16-Bit Vedic Multiplier Using Carry Skip Adder

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Abstract: **In modern digital signal processing and computing applications, high-speed and low-power multiplication units are crucial for efficient performance. This paper presents the design and implementation of a 16-bit Vedic multiplier using a Carry-Skip Adder (CSA) to boost computational speed while maintaining efficient power. [1-5]The Vedic multiplier is based on ancient Indian Vedic mathematics, specifically the "Urdhva Tiryakbhayam (Vertically and Crosswise) Sutra", which enables parallel processing of partial products, reducing latency (delay) compared to traditional multipliers.[11-18] The incorporation of the Carry-Skip Adder further optimizes performance by minimizing carry propagation delay, directing to faster addition of partial products. Simulation results demonstrate significant improvements in speed and power consumption compared to traditional multipliers such as the Array Multiplier and Booth Multiplier [19-21]. This technique is suitable for high-performance computing applications, including DSP, cryptography, and image processing [7-14].**

Index Terms: **Vedic Multiplier, Carry Save Adder, Carry Skip Adder, Xilinx ISE 14.7 version**

I.INTRODUCTION

Multiplication is a key math operation used in many areas like image resizing, filtering, extracting features, digital signal processing, cryptography, and scientific calculations. The speed and efficiency of a computer rely heavily on the quality of its multiplier. So, designing fast and low-power multipliers is very important. Traditional multipliers such as Array and Booth Multipliers have problems like long delays and high-power use.These issues come from the time it takes to generate partial products and pass carries that slow down the process. To fix these problems, Vedic mathematics offers a useful way to create faster multipliers.

Vedic mathematics is an old Indian math system with many simple formulas called sutras. One of these, the "Urdhva Tiryakbhayam" or "Vertically and Crosswise" Sutra, is especially good for multiplication. This method allows multiple partial products to be made at the same time, which cuts down the total time needed. It is also suitable for building hardware. However, adding the partial products together can slow down the machine because carry passing takes time. To improve this, a Carry-Skip Adder (CSA) is added. The CSA speeds up addition by skipping over bits where no carry is needed, making the whole process faster.

II. DESIGN PROCEDURE

Vedic Multiplier uses the Urdhva Tiryagbhyam Sutra, which means "Vertically and Crosswise." This method works well for hardware because it can do many calculations at the same time, making multiplications faster.

1.write the numbers you want to multiply in binary form.

2.perform crosswise multiplication and vertical addition following the Urdhva Tiryagbhyam method.

3.If you are multiplying 16-bit numbers, repeat the process, shifting and adding the partial results to get the final answer.

4.At each step, handle carrying over numbers with an adder, such as CSKA or CSA.

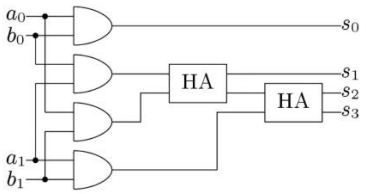

Fig: 1. 2x2 Vedic Multiplier

Carry Skip Adder (CSKA) speeds up binary addition. It skips over parts of the addition when possible, reducing delay caused by carry signals.

1.Break the bit string into smaller blocks, like 4 bits each.

2.Use a basic adder within each block to find the sum and create a carry-out.

3.Add skip logic that checks if all bits in the block are 1 and if the carry-in is 1. If yes, the carry can jump past the block.

4.If the conditions are met, carry skips to the end of the block; if not, carry moves normally.

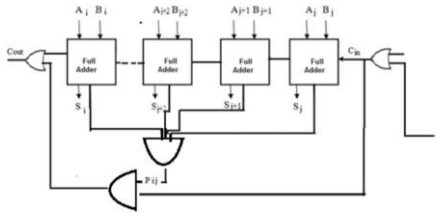

Fig:2 4-Bit Carry Skip Adder

Carry Select Adder (CSA) prepares two results for each block, one assuming carry-in is 0, the other assuming carry-in is 1.

1.Split input bits into blocks.

2.For each block, calculate sums and carries for both cases at the same time using duplicate adders.

3.At the end of the block, use a multiplexer controlled by the previous carry to pick the right sum and carry.

4.To implement these on a Xilinx ISE follow these steps:

5.Start by writing Verilog code for the multiplier, CSKA. Define modules for each part.

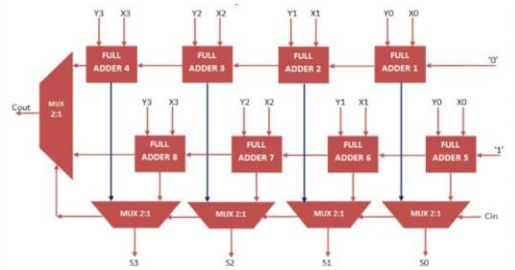

Fig:3 4-Bit Carry Save Adder

Test the final setup with real data or test patterns. Check how fast it works, how much space it takes on the chip, and how much power it uses.

Finally, analyze the results. Compare the performance of the Vedic multiplier with CSKA and CSA (which are taken before hand). Find out which one is better in speed, efficiency, and resource use.

III. IMPLEMENTED DESIGN

Vedic Multiplier using CSKA

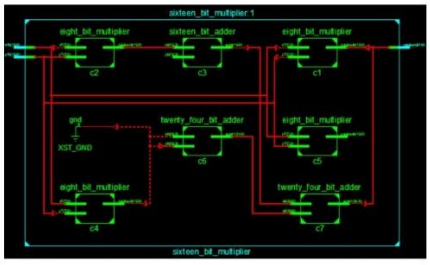

Fig: 4 Vedic Multiplier Using Carry Skip Adder

The schematic shows a 16-bit Vedic multiplier made with four 8-bit Vedic multiplier blocks. Each block takes two 8-bit parts of the inputs and produces 16-bit partial products. Two 32-bit Carry Skip Adders (CSKA_32) are used to add these partial products. The lower pair of multipliers connects to one adder, and the upper pair to the other. The outputs from the adders combine to give the final 32-bit product. Power and ground connections are shown for the circuit. The final output is a 32-bit number representing the product of two 16-bit inputs.

IV. RESULTS AND DISCUSSIONS

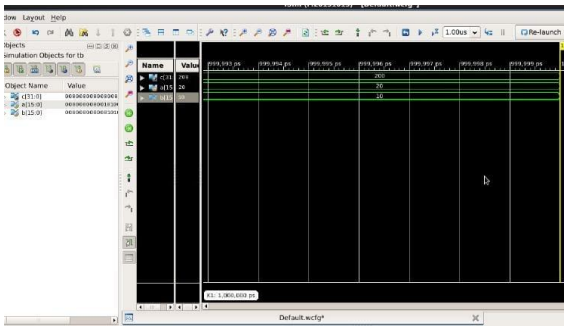

Fig: 5 Simulation Results

During the testing phase of the project, the 16-bit Vedic Multiplier combined with Carry Skip Adders (CSKA) was carefully tested to see how well it worked. A variety of test inputs were used to check all the possible paths in the circuit. The tests showed that the multiplier produced the correct results when multiplied. This confirmed that the design works properly and does what it is supposed to do.

Parameter	CSA	CSKA
Delay	7.85ns	8.30ns
Power	32.523mW	31.527mW
AND Gates used	1885	1034
OR Gates used	1365	386
Number of AND/OR logics used	30	28

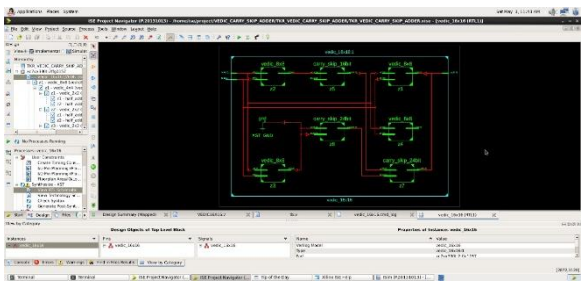

Fig:6 RTL View of 16_16 Vedic Multiplier Using Carry Skip Adder

V. FUTURE SCOPE

The future of the 16-bit Vedic multiplier using carry skip adder looks promising. It can become faster and more efficient with better designs. Combining it with modern low-power tech will lower energy use. Researchers might also improve the carry skip adder to make it more reliable. New materials or faster logic gates could boost overall speed. As chips get smaller, integrating this system into compact devices gets easier. It could replace older, slower multipliers in many applications. There's potential for it to be used in high-speed digital signal processing and computing. Improved algorithms could make the multiplier even more accurate with less power. The design might also adapt to support larger bit sizes or special computing tasks. Overall, this approach can help build faster, smaller, more efficient hardware in the future.

VI. ADVANTAGES

1.Audio Compression
2.Digital Image Processing
3.Compression of Videos
4.Speech Processing and Recognition
5.Digital Communication
6.Radio Detection

VII. CONCLUSION

This paper describes the design and build of a 16-bit Vedic multiplier that operates at high speed and is combined with a Carry Skip Adder (CSKA) for better arithmetic performance. The multiplier uses the Urdhva Tiryakbhayam sutra from Vedic math, which helps lower the number of partial products and makes calculations faster. The addition part of this system uses the CSKA, which reduces delays caused by carrying over digits. This makes addition faster and consumes less power. The combination improves the overall speed and efficient of the arithmetic operations.

VIII. ACKNOWLWDGEMENT

We Acknowledge G. Anitha Chowdhary for their patience checking in Manuscript and Result Validations.

REFERENCES

[1] Parameshwara, M.C., "Approximate full adders for energy efficient image processing applications" Journal of Circuits, Systems and Computers, vol. 30, issue 13, pp.1-17, Oct. 2021.

[2] P. Choppala, V. Gullipalli, M. Gudivada and B. Kandregula, "Design of Area Efficient, Low Power, High Speed and Full Swing Hybrid Multipliers," 2021 International Conference on Computing, Communication, and Intelligent Systems (ICCCIS), 2021, pp. 929-934.

[3] A. Jain, S. Bansal, S. Khan, S. Akhter and S. Chaturvedi, "Implementation of an Efficient N×N Multiplier Based on Vedic Mathematics and Booth-Wallace Tree Multiplier" 2019 International Conference on Power Electronics, Control and Automation (ICPECA), 2019, pp. 1-5.

[4] M. Munawar et al., "Low Power and High Speed Dadda Multiplier using Carry Select Adder with Binary to Excess-1 Converter," 2020 International Conference on Emerging Trends in Smart Technologies (ICETST), pp. 1-4, 2020.

[5] Parameshwara, M.C., Nagabushanam, M. "Novel low quantum cost reversible logic based full adders for DSP applications. " International Journal of Information Technology. 2021, vol. 13, pp.1755–1761.

[6] C.W.Tung and S.H. Huang, "A High-Performance Multiply- Accumulate Unit by Integrating Additions and Accumulations into Partial Product Reduction Process," in IEEE Access, vol. 8, pp. 87367-87377, 2020.

[7] K. B. Jaiswal, Nithish Kumar V, P. Seshadri and Lakshminarayanan G, "Low power Wallace tree multiplier using modified full adder," 2015 3rd International Conference on Signal Processing, Communication and Networking (ICSCN), pp. 1-4, 2015.

[8] Author(s): Mano, M. M. Project/Topic: Digital Logic and Computer Design Relevance: Provides fundamental knowledge of binary arithmetic, basic adder circuits (like half-adders and full-adders), and basic multiplier concepts.

[9] Author(s): Floyd, T. L. Project/Topic: Digital Fundamentals Relevance: Covers the basics of digital circuits, including logic gates and how they are used to implement arithmetic operations.

[10] Author(s): Hayes, J. P. Project/Topic: Computer Architecture and Organization

Relevance: Introduces basic computer arithmetic algorithms, including simpler multiplication methods.

[11] Author(s): Stallings, W. Project/Topic: Computer Organization and Architecture Relevance: Provides an overview of how arithmetic operations are performed within a computer, including basic multiplier structures.

[12] Author(s): Koren, I. Project/Topic: Computer Arithmetic Algorithms Relevance: While comprehensive, it starts with fundamental arithmetic algorithms, including basic multiplication techniques that predate more advanced methods like Vedic multiplication in digital hardware.

[13] Author(s): Savithri, T. N., & Mallikarjuna, P. Project/Topic: "Design of a Simple 4-bit Vedic Multiplier Using Urdhva Tiryakbhyam Sutra" Relevance: Focuses on a smaller bit-width Vedic multiplier, illustrating the basic application of the Sutra in hardware.

[14] Author(s): Sumathi, S., & Surekha, K. Project/Topic: "Implementation of a 2x2 Vedic Multiplier Using Basic Logic Gates" Relevance: Shows the very fundamental implementation of Vedic multiplication at a very small scale.

[15] Author(s): Lewis, E. L. Project/Topic: "Understanding Basic Adder Circuits" (e.g., an online tutorial or a chapter in a basic digital electronics book) Relevance: Explains the operation of ripple carry adders, which are simpler than carry skip adders and provide a foundation for understanding carry propagation.

[16] Author(s): Various educational websites (e.g., All About Circuits, Electronics Tutorials) Project/Topic: Articles explaining the function and implementation of half-adders, full-adders, and basic parallel adders. Relevance: These resources offer introductory explanations of the building blocks of addition circuits.

[17] Author(s): A textbook on VHDL or Verilog for beginners (e.g., Bhaskar, J. - A VHDL Primer) Project/Topic: Early chapters often include examples of implementing basic logic gates and simple arithmetic circuits like adders and basic multipliers in hardware description languages. Relevance: Shows how these fundamental circuits are described for hardware implementation.

[18] Author(s): A lab manual for a basic digital electronics course Project/Topic: Experiments involving the design and testing of basic adder and multiplier circuits using logic gates or small-scale integrated circuits. Relevance: Provides hands-on experience with the fundamental building blocks.

[19] Author(s): Singh, S., & Meena, K. L. Project/Topic: "Design and Simulation of a Low Power 4-bit Multiplier Using CMOS Technology" Relevance: Focuses on a smaller bit-width multiplier and basic CMOS implementation, which is a fundamental technology for digital circuits.

[20] Author(s): Karnik, T., & Borkar, S. Project/Topic: "Low-Power Digital Design" (early chapters) Relevance: Introduces basic concepts of power dissipation in digital circuits, relevant even for simpler designs.

[21] Author(s): A basic tutorial on how a shift-and-add multiplier works (widely available online). Project/Topic: Explains one of the fundamental algorithms for binary multiplication. Relevance: Provides a basic understanding of how multiplication is performed at the hardware level before introducing more optimized techniques.