To Design of Low Power Wide Rangevoltage Level Shifter Using Cmos Technology

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***Abstract*—The Paper introduces an ultra-low leakage, high-speed level shifter capable of wide-range voltage and frequency conversion. It uses leakage shutoff transistors to eliminate static current during standby, significantly reducing power consumption. A low-threshold transistor in the pull-down path enables faster falling edges, while voltage hysteresis transistors enhance the pull-up network for quick and complete charging of internal nodes, solving swing issues and improving performance. Designed using the Mentor Tanner 16 nm process, the level shifter demonstrates efficient operation with ultra-low power consumption when converting voltages from 0.3 V input to over 1.2 V output. It achieves minimal propagation delay and low energy per transition, supporting a broad conversion range from 0.13 V to above 1.2 V. Overall, the design ensures energy efficiency and high-speed operation across varying voltage levels.**

***Index Terms*—Level Shifter, Ultra-Low Leakage Voltage Conversion, Fast Transition, Low-Threshold Transistor, Power Efficiency, Wide Voltage Range**

I.INTRODUCTION

The rapid advancement of portable electronic devices such as smartphones, tablets, and laptops has heightened the demand for energy-efficient digital circuits. A common strategy to reduce power consumption is lowering the supply voltage, but this often compromises system performance. To maintain both power efficiency and speed, multi-voltage designs are employed, allowing different circuit blocks to function at varying voltage levels. This creates the need for level shifters (LSs) to

ensure proper communication between modules operating at different supply voltages.

Propagation delay and power dissipation are crucial parameters in LS performance. With the rising complexity of System-on-Chip (SoC) designs, energy-efficient and high-speed LSs are essential for modern low-power applications. Conventional LS designs like the differential cascade voltage switch level shifter (DCVSLS) and the current mirror level shifter (CMLS) face limitations. DCVSLS suffers from contention between pull-up and pull-down paths, especially at low voltages. CMLS reduces contention but often results in high static current due to incomplete transistor shutdown.

Advanced designs such as the Wilson current mirror LS (WCMLS), reduced-swing buffers, and auxiliary bias circuits aim to improve efficiency but still face issues like limited voltage swing, increased transition time, and leakage during switching. Designs incorporating error detection or logic-mismatch control also encounter trade-offs between complexity and power loss.

This brief proposes a new LS architecture that integrates a current mirror structure, a voltage hysteresis transistor, and mixed-threshold devices to optimize performance. The voltage hysteresis helps reduce internal node swing, while mixed-threshold transistors balance pull-up and pull-down strength. Additionally, a leakage shut-off transistor is used to cut off the pull-down path during standby, minimizing static current.

Simulation results using the Mentor Tanner 16 nm process confirm that the proposed LS achieves ultra-low leakage and fast voltage conversion from 0.3 V to

over 1.2 V, with a wide conversion range of 0.13 V to 1.2 V.

II.METHODOLOGY

i EXISTING METHODOLOGY:

In conventional current mirror–based level shifters, when the input voltage falls near or below the transistor threshold, the pull-down transistors MN1 and MN2 cannot fully discharge the intermediate node N1. As a result, the current mirror's ability to charge node N2 diminishes, preventing it from reaching high logic level. This reduced output swing at N2 causes the subsequent buffer stage inputs to linger at intermediate voltages, simultaneously activating both its pull-up and pull-down networks. The resulting contention increases static current consumption, undermining the level shifter's efficiency. This issue is particularly severe in sub-threshold operation, where device drive currents are limited.

i. PROPOSED METHODOLOGY:

The design and validation of a low-power, wide-range voltage level shifter are essential for modern digital CMOS systems that operate across multiple voltage domains. With the rapid advancement of energy-efficient electronics such as wearables, smartphones, and IoT devices, there's a growing demand for level shifters that can effectively convert signals between low and high voltage levels without compromising speed or increasing power consumption. Traditional level shifters, like differential cascade voltage switches (DCVS) or current mirror (CM) based designs, often suffer from drawbacks such as contention currents, static power dissipation, or reduced output swing—especially under near-threshold or sub-threshold conditions. These issues lead to performance degradation and excess energy consumption.

The proposed level shifter introduces a novel architecture that incorporates leakage shut-off transistors to eliminate static current during standby, low-threshold transistors for rapid transitions, and voltage hysteresis elements to enhance pull-up strength. This combination ensures full voltage swing and fast, reliable conversions across a wide range of voltages. Validated through simulations using the Tanner EDA 16nm CMOS technology, the design demonstrates ultra-low leakage and minimal delay, efficiently converting signals from as low as 0.13 V to over 1.2 V.

III.IMPLEMENTED DESIGN

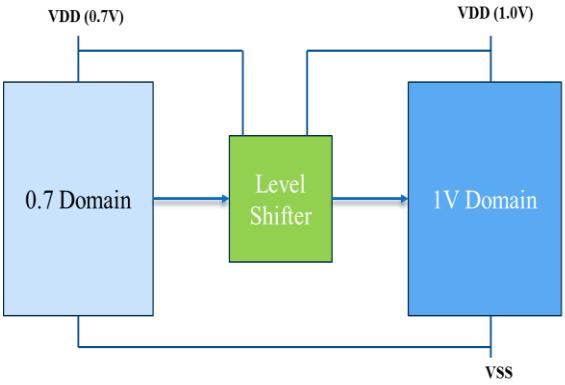


Fig1: Block Diagram

The block diagram shows how data is passed between two circuits that operate at different voltages, using a level shifter in between. On the left, we have a circuit running at 0.7 volts, called the 0.7V Domain. On the right, there's another circuit that operates at 1 volt, called the 1V Domain. These two blocks cannot directly talk to each other because they use different voltage levels. If they try to send signals directly, it could lead to incorrect data or even damage.

To solve this, a Level Shifter is used. This block sits between the two domains. It takes signals from the 0.7V Domain and converts them to the voltage level used by the 1V Domain. In simple terms, it boosts the voltage of the signals without changing the data being sent. The arrows in the diagram show the direction in which the signals travel — from the lower voltage side to the higher voltage side. The dark blue lines at the top and bottom represent power connections. Each domain is powered by its own voltage supply. This ensures both parts of the system operate correctly and safely.

In summary, the level shifter allows two parts of an electronic system with different voltage requirements to communicate with each other effectively, avoiding any electrical mismatch and maintaining signal integrity.

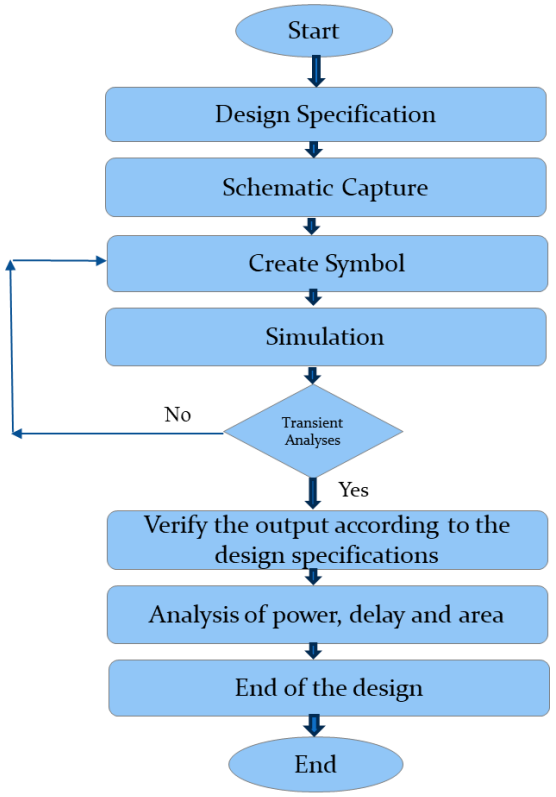


Fig2: Flow Chart

The flowchart illustrates the step-by-step process involved in designing an electronic circuit in a simple and structured manner. It begins with the Start of the design phase, followed by the Design Specification stage where the requirements and functionality of the circuit are clearly defined. These specifications include factors like voltage, speed, and expected performance. Once the goals are established, the next step is Schematic Capture, where the circuit is drawn using electronic components to show how they will be connected.

After capturing the schematic, a Symbol is created for the circuit. This helps in using the design as a block in more complex circuits. The design then moves to the Simulation stage, where the behaviour of the circuit is virtually tested. If the simulation passes, a Transient Analysis is conducted to evaluate how the circuit performs over time, particularly during changes in input or conditions. If problems are detected, the process may loop back to earlier steps to make corrections.

Once the simulation and analysis are successful, the output is Verified against the original design requirements to ensure everything works as planned. This is followed by an Analysis of Power, Delay, and Area, where the design is evaluated based on energy usage, speed, and space efficiency. If all results are satisfactory, it leads to the End of the Design, and finally, the project reaches its End.

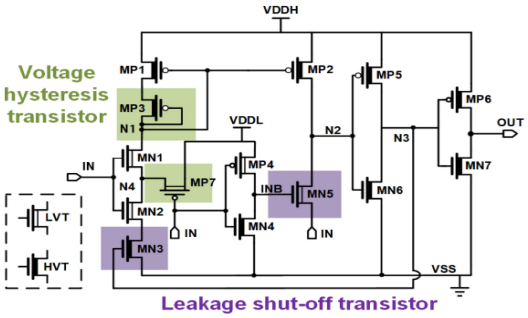


Fig3: Schematic Diagram

This schematic shows a low-power level shifter circuit, which is used to safely convert signals from one voltage level to another—typically from a lower voltage to a higher one—while minimizing power loss. The circuit mainly consists of PMOS (MP1 to MP7) and NMOS (MN1 to MN7) transistors. Two special types of transistors are highlighted in the diagram: the voltage hysteresis transistors (green area) and leakage shut-off transistors (purple area).

The voltage hysteresis transistors (MP3, MN1) help improve noise immunity. They create a small voltage gap between when the output switches from low to high and from high to low. This makes the circuit more stable and less sensitive to small voltage changes at the input.

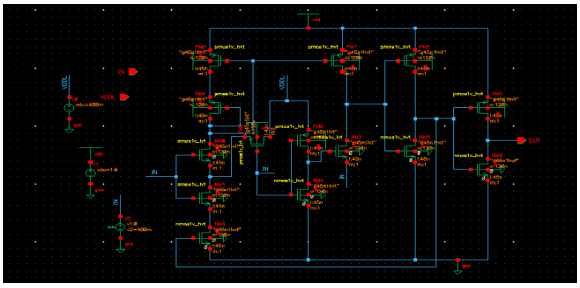
The leakage shut-off transistors (MN3, MN5) are used to reduce power leakage when the circuit is idle. These transistors cut off unwanted paths where current might flow unnecessarily, helping to conserve power.

The level shifter works by taking a low-voltage input signal (IN) and generating a higher-voltage output signal (OUT) that other parts of the chip can understand. The output stage (MP6, MP7, MN6, MN7) drives the output signal to either a high or low state depending on the input.

Overall, this circuit is designed to ensure reliable signal conversion between voltage domains while reducing power consumption and enhancing signal stability.

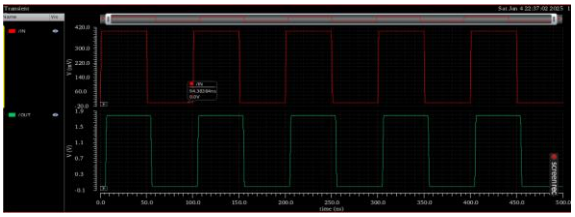
IV.RESULT

The expected results for a project titled "Design of Low Power Wide Range Voltage Level Shifter Using CMOS Technology", based on typical simulation outcomes and goals in such designs. These can be tailored or extended depending on the specific CMOS technology node (e.g., 65nm, 45nm), tools used (like Cadence, Synopsys), and simulation setup.



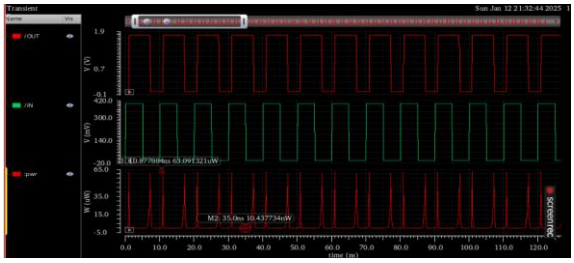
Schematic Of Proposed Method

When the input changes from low (VSS) to high (VDDL), as shown in Fig. 5.1. As the MN1 and MN2 are optimized with low-threshold transistors to strengthen the pull-down network, the MN1 and MN2 are turned on, and the current mirror charges the internal node N2 through the MP2 quickly. However, when the input voltage of the conventional current mirror LS is near/sub-threshold, the pull-down network MN1 and MN2 are too weak to discharge the N1, which will decrease the current mirror charging time for the N2 and lead to the reduced swing problem which causes the high static current in the next stage buffer.



Simulation Results of Proposed Method

The N1 maintains a lower voltage for the MP2 to have a faster speed to charge the node N2 fully, the current from MP2 to charge the node N2 is shown in Fig. 5.2. Meanwhile, the source of MN5 is equally connected to VDDL, which makes the MN5 completely cut off and prevents current leakage.



Power analysis of proposed method

The design could achieve a complete cut-off for the leakage current. Fig. 5.2 shows the comparison between the proposed LS and the others about the voltage of node N2. With the employment of MP3, the reduced swing problem is significantly improved. Besides, to save energy, a leakage shut-off transistor MN3 is inserted, when the N2 is high, and the N3 changes to low, the MN3 is closed, and the current mirror is closed completely.

V. CONCLUSION

The work introduces an innovative and energy-efficient voltage level shifter (LS) capable of converting signals from a deep subthreshold voltage of 400 mV up to a standard 1.8 V. The design integrates a reduced-swing buffer to minimize leakage currents and incorporates pass transistors to enhance the falling edge transition, thereby boosting speed.

This combination significantly reduces static power while improving overall conversion performance. The level shifter was successfully implemented and tested using 16nm Tanner EDA tools, confirming its efficiency in low-power applications. The results demonstrate that this design effectively balances speed and power, making it ideal for modern digital circuits operating across multiple voltage domains.

Its ability to handle wide voltage ranges with minimal energy loss makes it highly suitable for advanced systems-on-chip (SoCs), wearable devices, and battery-operated electronics, where power efficiency is critical. The proposed LS is a practical solution for future low-voltage, high-efficiency circuit designs in advanced CMOS technologies.

VI. FUTURE SCOPE

The future scope of designing a low power wide range voltage level shifter using CMOS technology is highly promising. With the growing demand for energy-efficient and compact devices, especially in IoT, wearable electronics, and multi-voltage SoCs, advanced level shifters are essential. Future work can explore further reduction in leakage using advanced transistor architectures like Fin FETs or gate-all-around FETs. Integration with adaptive body biasing and sleep-mode features can enhance performance and power savings. Additionally, expanding voltage compatibility for emerging ultra-low voltage systems and high-speed applications will make the design more robust and scalable for next-generation semiconductor technologies**.**

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