Enhanced Five-Level Inverter Design with Lower Leakage Current for Photovoltaic Applications

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***Abstract*—There's a noticeable rise happening in the utilization of renewable energy sources, and the usage of photovoltaic cells to capture solar radiation and convert it into electrical power is growing.Since photovoltaic cells generate DC voltage, an inverter is required to connect them to the AC power grid, either directly or through a transformer. Transformerless inverters are widely preferred due to their reduced cost, lower power losses, and lightweight construction. However, one of the primary challenges associated with these inverters is the presence of leakage currents, which need to be effectively mitigated. In this study, a novel dual-connection topology is introduced to stabilize the common-mode voltage and significantly reduce leakage current. The proposed inverter generates a five-level output voltage, which contributes to lower harmonic distortion in the output current when compared to conventional two-level or three-level inverters. The operational principles and output characteristics of the new topology are thoroughly analyzed. Simulation of the inverter circuit was conducted using MATLAB/Simulink, and its performance was evaluated against several established inverter designs.**

I. INTRODUCTION

Solar energy is emerging as one of the most rapidly expanding sectors in the renewable energy landscape. Over the last few decades, phenomenal growth trends have been observed in the production and application of photovoltaic (PV) systems in an endeavor to harness clean energy from solar radiation. Compared to fossil fuels, sources of renewable energy such as solar energy do not lead to environmental pollution during their production and utilization.

Voltage source inverters in PV systems synchronize with the grid to facilitate more efficient energy transmission by converting DC power from solar panels into AC power. [2, 3]. With or without a transformer, the inverters can be connected to the grid.

Due to their efficiency, portability, and affordability when compared to transformers, grid- connected transformer-less inverters have become increasingly popular in recent years. The solar panel's galvanic coupling to the ground is the problem with transformerless inverters. Leakage current results from this [7]. Since grounding cells are essential for reducing leakage current, issues like them still need to be resolved even with the new inverters' generally acceptable efficiency. There are parasitic capacitors between the ground and the cells in transformer-less inverters because the ground of the cell is not isolated from the ground of the grid. This capacitor's presence causes a leakage current to flow through the system. This can pass through a human body and can cause very dangerous threats if beyond a certain value. Moreover, leakage current can reduce system efficiency, introduce unwanted harmonics, and increase the total harmonic distortion (THD) in the grid current. Figure 1 illustrates the overall structure of the PV system, including the inverter, output inductor, and the grid connection.

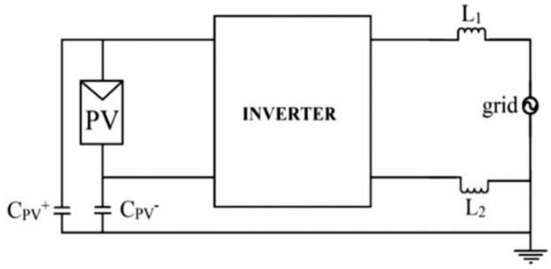


Fig. 1 Grid-Tied Solar Power Systems

The literature proposes a number of topologies to reduce leakage current. The most well-known topologies include HERIC [12], H5 structure [9], H6 [10, 11], and full-bridge structure with bipolar switching method, among others. Because of its constant common mode voltage, a full-bridge structure using the bipolar switching method exhibits extremely low leakage current. However, the two-level output voltage increases losses and necessitates the use of large output filters. Low inductance current ripple, superior differential characteristics, and increased efficiency are the advantages of a full-bridge inverter using a unipolar switching technique. However, the drawbacks include excessive leakage current and unsuitable common mode characteristics [13].

Isolating the AC side from the DC side while in freewheeling mode is the alternative technique. To reduce the leakage current, the structure proposed in [14] connects the solar cell's negative terminal to the grid's neutral point. Despite being simple to use, this structure requires additional devices, even though its input voltage is the same as that of the full bridge structure. This structure uses a single inductor and removes one of the output inductors. As a result, the full-bridge structure and unipolar modulation were used to create the H5, H6, and HERIC structures. Because the filter inductor cores must be isolated, the cost and weight of the filters in this type of inverter are increased.

These topologies have been used in the design of many structures. For instance, the midpoint of the two input-side capacitors is connected to the inverter's output to create a sequence of inverters with the HERIC topology. This allows them to further reduce leakage current by keeping the common mode voltage constant in the freewheeling mode [15–18]. A topology featuring two diodes and six switches is proposed in [19], where two extra switches are added between the legs of the full-bridge structure. This configuration enables a freewheeling mode that short-circuits the output, effectively reducing leakage current by suppressing large fluctuations in common-mode voltage. Additionally, [20] presents a cascaded HERIC-based topology using a 9-level inverter, designed to accommodate multiple PV cells.

This topology has the advantage of being multilevel and able to isolate the grid from PV cells during freewheeling mode, which reduces leakage current. However, the costs are high because this structure uses a lot of switches. Conduction losses are also increased by the additional switches that are in the current's path while it is operating.

A high-performance five-level inverter with dual structural solutions for leakage current reduction is introduced in this study. By connecting the inverter outputs to the DC bus's midpoint when it is freewheeling, these two structures reduce leakage current and common-mode voltage oscillationThe proposed topologies are designed to produce a five-level output voltage from the inverter, which enhances the quality of the output current and significantly reduces harmonic distortion. The performance of the proposed design is compared with that of the M-NPC MOSFET structure discussed in [16] and the HERIC topology referenced in [15–18]. This study highlights several key advantages of the proposed inverter, including better stabilization of common-mode voltage, reduced leakage current, improved multilevel output, lower total harmonic distortion (THD), and higher efficiency. Section 1 provides a comprehensive literature review, followed by an explanation of leakage current in HERIC inverters in Section 2. The new topology is introduced and explained in Section 3 using two connection models. Simulation results are presented in Section 4, and conclusions are drawn in Section 5.

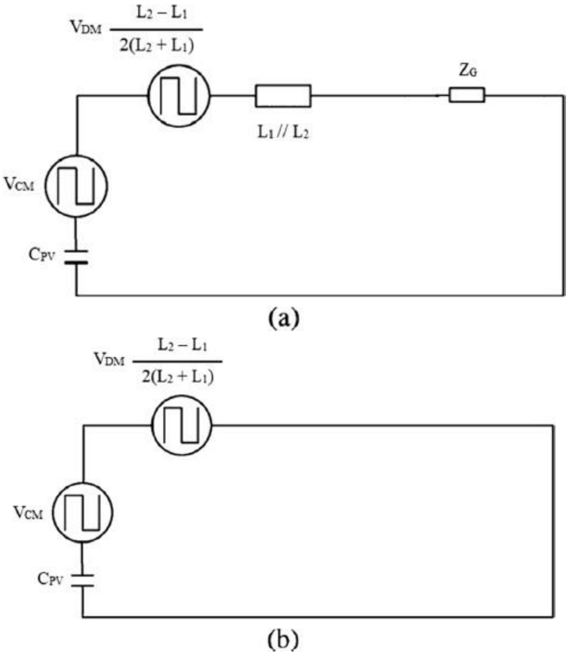


Fig. 2 Common-mode model

II. LEAKAGE CURRENT IN INVERTERS

As shown in Fig. 2, leakage current in transformerless inverters flows through the ground impedance (ZG), output inductors (L1, L2), and parasitic capacitors (between the ground and the PV panel (CPV)). Regardless of ZG, the simplified model is shown in Fig. 2b, while the detailed model of the common-mode noise is shown in Fig. 2a. Its parasitic capacitance value, which has historically been estimated to be between 50 and 150 nF/kW, is highly dependent on a number of factors, including the solar array's surface, the surrounding environment, the distance between the ground and the plate, humidity, and dirt [8]. Full-bridge inverters switch unipolarly but have a high leakage current. It is not recommended to increase the common mode voltage by creating a freewheeling path between DC and AC using the AC separation method. Here, a short circuit in the inverter output causes freewheeling. Figure 3 describes the HERIC inverter, one of the most common AC separation configurations. It usually applies to confirming the behaviour of leakage currents. The equivalent common-mode voltage (VECM), differential and common mode voltages, and leakage currents are calculated using the definitions in [28] as a guide:

$$V_{ECM} = V_{CM} + \frac{V_{DM}}{2}\frac{L_1 - L_2}{L_1 + L_2} \quad (1)$$

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (2)$$

$$V_{DM} = V_{AN} - V_{BN} \quad (3)$$

$$I_{Leakage} = C_{PV}\frac{dV_{CM}}{dt} \quad (4)$$

In reference to the PV array's negative terminal (denoted as point N in Figure 3), VAN and VBN represent the voltage differences between points A and N, and B and N, respectively. If inductors L1 and L2 are equal, the second term in equation (1) is eliminated. The leakage current depends on changes in the common-mode voltage, as described in equation (4). To manage the common-mode voltage during freewheeling mode, two additional switches (S5 and S6) are introduced on the AC side of the HERIC inverter. This control is achieved by utilizing the parallel diodes of S5 and S6: during the positive half-cycle, the diode of S5 conducts, while during the negative half-cycle, the diode of S6 takes over. In this mode, all other switches remain turned off.

In this study, the HERIC inverter is compared not only with its own structure but also with other proposed topologies, including the MOSFET-based Neutral-Point-Clamped (M-NPC) inverter described in [16]. The M-NPC structure consists of seven switches and four diodes and operates with two freewheeling modes. During the positive freewheeling cycle, D1, D2, S2, and S5 are turned ON, while in the negative freewheeling cycle, D1, D3, D4, and S7 are ON. This topology exhibits asymmetrical behavior during positive and negative conduction cycles: in the positive half-cycle, switches S1, S2, S5, and S6 conduct, whereas in the negative half-cycle, only S3 and S4 are active.

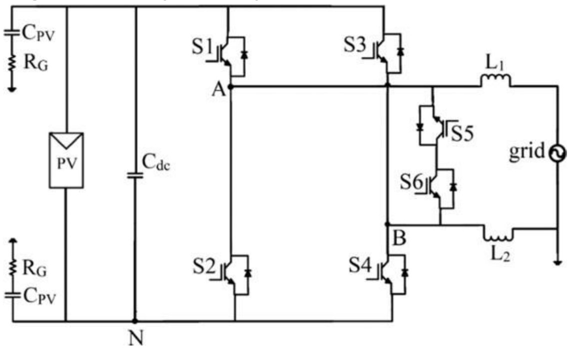


Fig. 3 The HERIC topology

III. THE PROPOSED TOPOLOGY

This provides a new five-level topology with eleven switches. It can reduce leakage current. Two structures are introduced in this topology. The way the inverters and PV panels are connected is the main difference between them. Depending on the solar panels that are available, there are multiple ways to connect the inverter to them, and each option has unique features. While the second design has less leakage current of each panel (not grid leakage current) than the first, the first design has a smaller THD of the output current. This improves panel usage safety.

A The Topology with the First Structure

Figure 5 illustrates the first proposed topology, where the voltage of PV1 is twice that of PV2 (i.e., VPV1 = 2VPV2). By placing capacitors (Cdc) in parallel with the PV panels, voltage division is achieved, resulting in multiple voltage levels at the input side relative to point N. For pulse-width modulation, the Sinusoidal PWM (SPWM) method is used due to its simplicity and effective performance in multilevel inverter applications. Specifically, this study employs the Level-Shifted Carrier PWM (LSC-PWM) technique, which uses two high-frequency carrier signals that share the same phase, amplitude, and frequency.

In this method, the amplitude of each carrier wave is set to 1 divided by the number of carriers—resulting in an amplitude of 0.5 in this study, where two carriers are used. The switching operation is based on comparing these two high-frequency triangular carrier waves with a low-frequency sinusoidal modulation signal representing the grid voltage, as illustrated in Figures 5 and 6. The carrier wave frequency is set to 16 kHz.

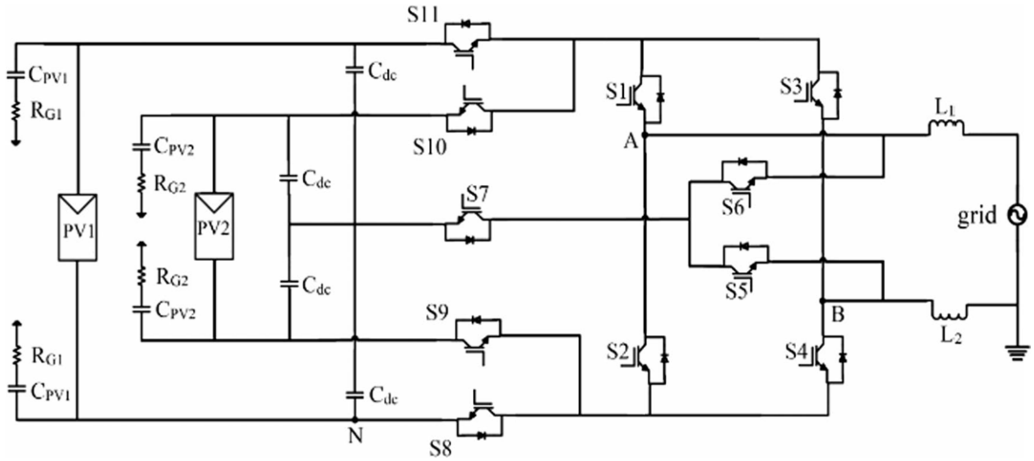


Fig.4 configuration of the proposed topology

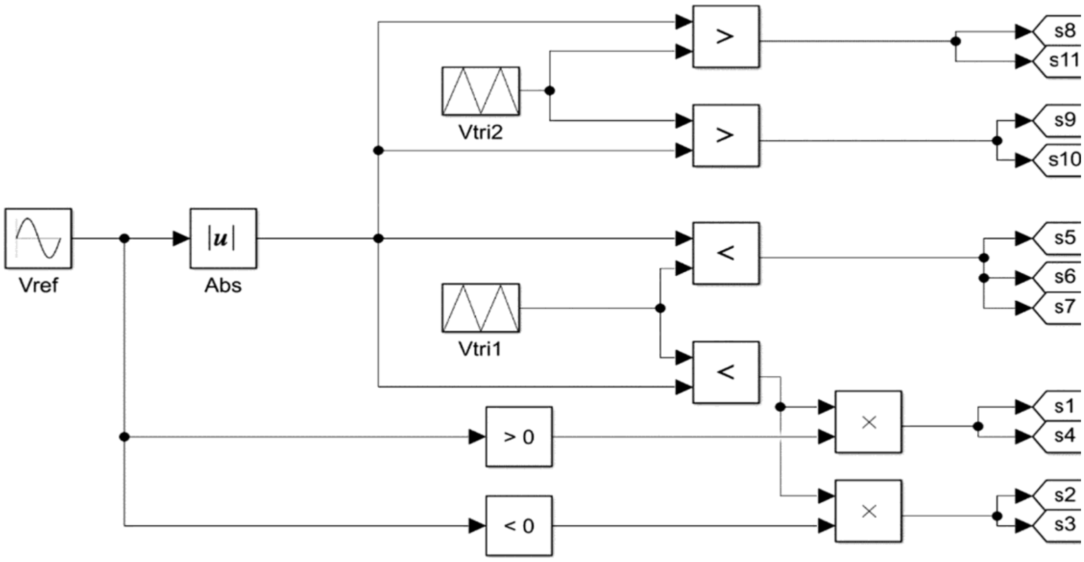


Fig. 5 Gate signals generated by the proposed switching algorithm

The controlling rules are defined as follows:

If (Vcontrol) > Vtri1 then S1, S4 are ON (5)
If (−Vcontrol) > Vtri1 then S2, S3 are ON (6)
If (|Vcontrol |) < Vtri1 then S5, S6, S7 are ON (7)
If (|Vcontrol |) > Vtri2 then S8, S11 are ON (8)
If (|Vcontrol |) < Vtri2 then S9, S10 are ON

The suggested inverter has five operating modes: two operating in the positive cycle (Modes 1 and 2), two operating in the negative cycle (Modes 3 and 4), and one operating in the freewheeling cycle. In the positive or negative cycle, four switches are on, while three are in the freewheeling mode. The circuit schematic for the switch status with various operating modes is displayed in Fig. 7.

Mode 1: Others are OFF, while S1, S4, S9, and S10 are ON. In this case, points A and B are linked to PV2's positive and negative terminals. The circuit diagram and switch status are shown in Figure 7a. The common mode and differential (output voltage) voltages are computed as

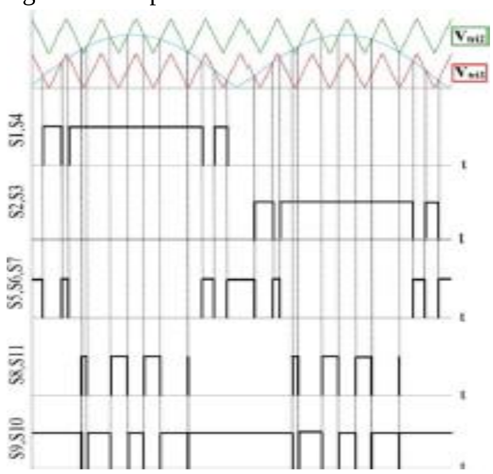


Fig. 6 Switching pattern

$$V_{AN}=\frac{3}{4}V_{PV1},\quad V_{BN}=\frac{1}{4}V_{PV1} \tag{10}$$

$$V_{AB}=V_{AN}-V_{BN}=\frac{1}{2}V_{PV1} \tag{11}$$

$$V_{CM}=\frac{V_{AN}+V_{BN}}{2}=\frac{1}{2}V_{PV1} \tag{12}$$

Mode 2: While the others are in the OFF state, S1, S4, S8, and S11 are in the ON state. The PV1's A and B terminals are shorted to points A and B, respectively, in this mode (Fig. 7b). The common mode voltage and differential (output voltage) are calculated as follows:

$$V_{AN}=V_{PV1},\quad V_{BN}=0 \tag{13}$$

$$V_{AB}=V_{AN}-V_{BN}=V_{PV1} \tag{14}$$

$$V_{CM}=\frac{V_{AN}+V_{BN}}{2}=\frac{1}{2}V_{PV1} \tag{15}$$

Mode 3: S2, S3, S9, and S10 are ON, while negative switches are OFF. In this mode, as shown in Fig. 7c, the PV2's positive and negative terminals are connected to points B and A, respectively, and the voltages are computed as:

$$V_{AN}=\frac{1}{4}V_{PV1},\quad V_{BN}=\frac{3}{4}V_{PV1} \tag{16}$$

$$V_{AB}=V_{AN}-V_{BN}=-\frac{1}{2}V_{PV1} \tag{17}$$

$$V_{CM}=\frac{V_{AN}+V_{BN}}{2}=\frac{1}{2}V_{PV1} \tag{18}$$

Mode 4: The other switches are off, but S2, S3, S8, and S11 are on. As shown in Fig. 7d, the positive and negative terminals of PV1 are connected to points B and A, respectively, in this mode, and the voltages are known as:

$$V_{AN}=0,\quad V_{BN}=V_{PV1} \tag{19}$$

$$V_{AB}=V_{AN}-V_{BN}=-V_{PV1} \tag{20}$$

$$V_{CM}=\frac{V_{AN}+V_{BN}}{2}=\frac{1}{2}V_{PV1} \tag{21}$$

Mode 5: Since this is the freewheeling mode, S5, S6, and S7 are turned on, and points A and B (shown in Fig. 7e) represent the midpoint of the PV panels. The voltages in this case are as follows:

$$V_{AN}=V_{BN}=\frac{1}{2}V_{PV1}=V_{PV2} \tag{22}$$

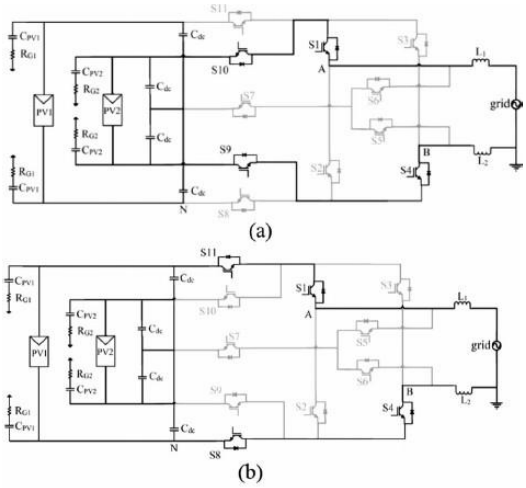
$$V_{AB}=0 \tag{23}$$

$$V_{CM}=\frac{V_{AN}+V_{BN}}{2}=\frac{1}{2}V_{PV1} \tag{24}$$

Table 1 lists the voltages in the common and differential modes for each of the operation modes. The voltages in points A and B are relative to the reference point (N). As can be seen, the common mode voltages in each of the operating modes are constant and equal to VPV1/2. By stabilizing the common mode voltage across all modes to VPV1/2, this structure lowers the leakage current. There are five output voltage levels, which are higher than those of other structures like HERIC: - 1/2VPV1, 0, +1/2VPV1, +VPV1, and −VPV1.

Table I Differential (output) and common mode voltage values in different operation modes for the first structure

Mode	V_{AN}	V_{BN}	V_{DM}
1	$\frac{3}{4}V_{PV1}$	$\frac{1}{4}V_{PV1}$	$\frac{1}{2}V_{PV1}$
2	V_{PV1}	0	V_{PV1}
3	$\frac{1}{4}V_{PV1}$	$\frac{3}{4}V_{PV1}$	$-\frac{1}{2}V_{PV1}$
4	0	V_{PV1}	$-V_{PV1}$
5	$\frac{1}{2}V_{PV1}$	$\frac{1}{2}V_{PV1}$	0



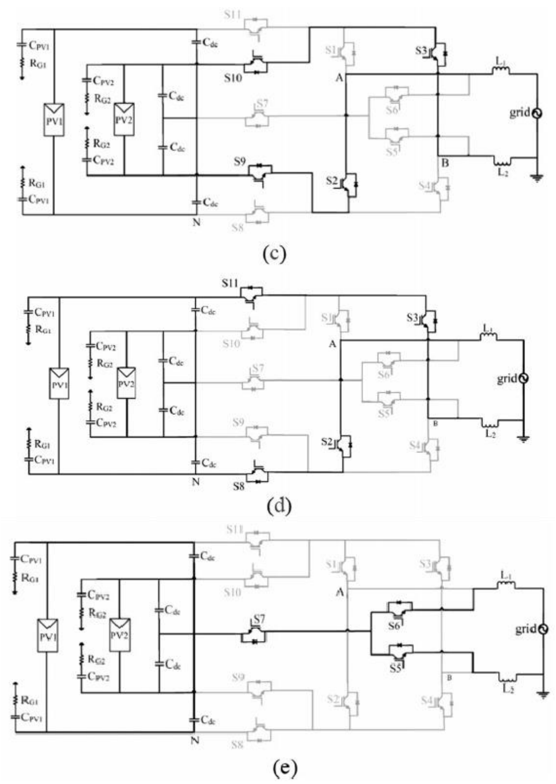


Fig. 7 Circuit diagram for the first structure of the proposed topology in different operation modes: a) Mode 1, b) Mode 2, c) Mode 3, d) Mode 4, and e) Mode 5

IV. RESULTS AND DISCUSSIONS

MATLAB/Simulink simulations are used to evaluate the suggested topology's performance. Two distinct structures' worth of data are acquired for the suggested topology.

In the proposed topology, multiple PV panels with varying power ratings are used. As a result, the leakage capacitance for each panel is set in proportion to its power, based on a ratio of 100 nF per kilowatt. The simulations are conducted with a switching frequency of 16 kHz and a system power of 2 kW. Only the steady-state behavior of the system is shown; the transient response is not considered. According to the simulation results, both structures exhibit similar performance. For comparison with conventional topologies, the first structure is used.

V. CONCLUSION

In order to reduce leakage current, a novel inverter has been introduced in this paper. The impact of M-NPC and HERIC inverters on reducing leakage current is described and contrasted with the suggested topology. The output voltage of the suggested topology has five levels in addition to minimizing leakage current. In terms of reducing the output current THD, this is more effective than HERIC. Despite the slight structural and switching complexity of the new topology, the new inverter's main benefits are:

- Leakage current reduction and common mode voltage stabilization
- Multilevel output with reduced THD
- Greater efficiency than the other contending topologies

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