Design And Implementation of 6T SRAM Using Cadence

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***Abstract*—This project presents the design and implementation of a Static Random-Access Memory (SRAM) system using the Cadence Virtuoso. SRAM is a key component in modern digital systems, particularly in cache memory, due to its high speed, low latency, and low static power consumption. The 6T SRAM cell is composed of two cross-coupled CMOS inverters forming a bistable latch and two access transistors that enable read and write operations through word and bit lines. In addition to the SRAM cell, essential peripheral circuits such as the sense amplifier and the pre-charge and equalizer circuits were also designed to ensure proper read and write operations.**

The design flow includes schematic design and functional verification using DC and transient analysis to evaluate the performance and stability of the circuits. The project successfully demonstrates the key aspects of SRAM design at the schematic level, highlighting the role of supporting circuits in enhancing memory reliability and operations.

***Index Terms*—SRAM, CMOS, WL, BL, BLbar, Q, Qb**

I. INTRODUCTION

Memory plays a fundamental role in digital electronics, serving as a temporary or permanent storage medium for data. Among various types of memories, Static Random Access Memory (SRAM), a type of volatile memory that is widely used in cache architectures and high-speed processors due to its fast access time, low power consumption, and ease of integration in system-on-chip (SoC) designs. The basic architecture of an SRAM includes bit cells, decoders, sense amplifiers, and pre-charge and equalizer circuits, each serving a specific function to enable reliable and efficient data storage and retrieval.

The primary component of this system is the 6-transistor (6T) SRAM cell, known for its balance between performance, area efficiency, and stability. The 6T SRAM cell is designed with careful consideration of cell ratio (CR) and pull-up ratio (PR) to ensure both read and write stability. Proper transistor sizing is essential to achieve high cell density while maintaining performance and reliability.

To support the operation of the SRAM cell, a sense amplifier is designed to detect small voltage differences between the bit lines during a read operation and amplify them to full logic levels. This significantly improves speed and accuracy. Additionally, pre-charge and equalizer circuits are implemented to equalize and pre-charge the bit lines to a known state (typically Vdd/2) before each read or write operation, ensuring correct differential operation and reducing errors.

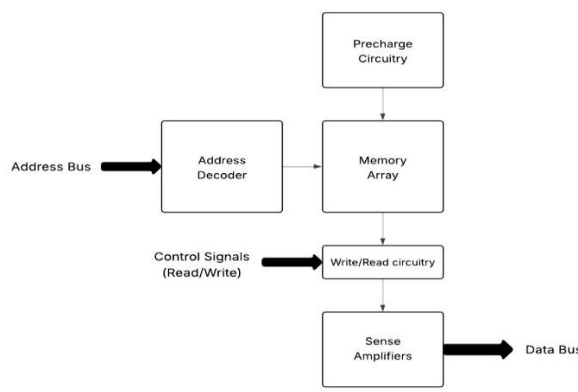

Fig. 1: Block diagram of SRAM

This work focuses on schematic-level design and simulation. The design is carried out at the transistor level using CMOS technology, emphasizing the practical aspects of memory circuit design. The functional simulations verify the correct behaviour of each block under ideal conditions. This project not only reinforces theoretical knowledge of VLSI design but also provides hands-on experience with industry-standard tools, illustrating the challenges and considerations involved in memory design.

II. EXISTING ARCHITECTURES

As per surveys, there exist many architectures of SRAM that use different numbers of transistors. Each circuit portrays unique outputs. But this system is uniquely designed to achieve better performance in terms of noise margin, read and write operations.

III. DESIGN METHODOLOGY

A. Requirement Analysis and Component Identification

This step involved understanding the basic structure and operation of an SRAM memory cell. A standard 6-transistor (6T) SRAM bit cell was chosen for its balance between speed, power, and area efficiency. Auxiliary circuits such as the sense amplifier and pre-charge and equalizer circuits were also identified as necessary components for proper memory operation.

B. Schematic Design in Cadence Virtuoso

Cadence Virtuoso is a powerful and widely adopted Electronic Design Automation (EDA) tool developed by Cadence Design Systems for the custom design of integrated circuits (ICs). It provides a comprehensive environment for the design, simulation, layout, and verification of analog, digital, RF, and mixed-signal circuits.

Thus, each component was designed at the transistor level using the Virtuoso Schematic Editor:

- 6T SRAM Cell: Two cross-coupled inverters form the bistable latch, with two NMOS access transistors controlled by the word line (WL).

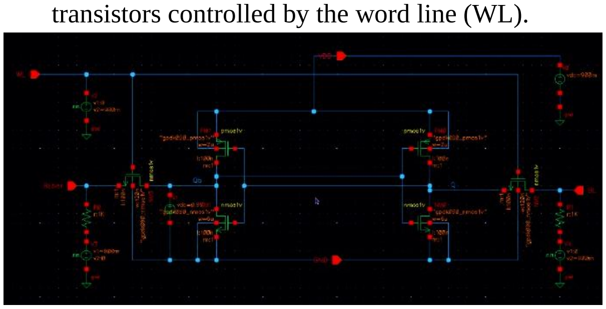

Fig. 2: Schematic of 1-bit SRAM cell

- Sense Amplifier: In memory circuits, the voltage across bit lines determines the stored bit. However, the presence of numerous cells connected to a single column makes it challenging to detect this voltage accurately. To address this, sense amplifiers are employed to enhance stability and reliability by detecting small voltage differences and amplifying them. This amplification increases the bit line voltage swing, improves fan-out, accelerates transitions, and ultimately reduces read access delay.

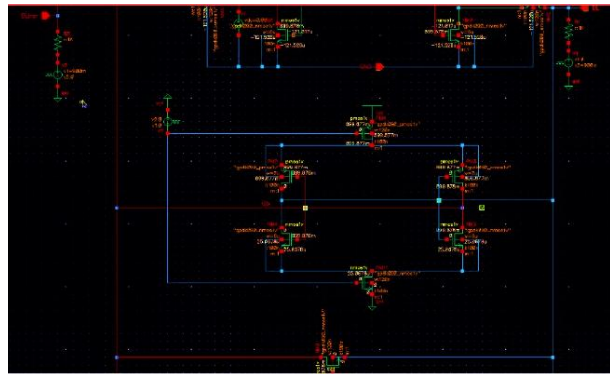

Fig. 3: Schematic of sense amplifier

- Pre-charge and Equalizer Circuit: Designed to pre-charge both bit lines to a known voltage (typically Vdd or Vdd/2) and equalize them before each read/write cycle.

Fig. 4: Schematic of pre-charge and equalizer circuit

C. Transistor Sizing and Design Optimization

Proper transistor sizing and cell ratio is crucial for ensuring stability during read and write operations as well as for the analysis of static noise margin (SNM). The cell ratio (CR) is defined as the ratio of the pull-down NMOS to access NMOS transistor.

D. Simulation and Functional Verification

Using Cadence Analog Design Environment (ADE), DC analysis and transient analysis was performed, to verify the following aspects:

- The correct operation of the SRAM cell during write and read cycles.
- Voltage levels and transitions at the outputs of the sense amplifier.
- Proper pre-charging and equalizing of bit lines before operations. Test benches were created to apply the required signals (WL, BL, BLbar, data_in, data_out, etc.) and observe responses across time.

E. Integration of Components

The final step involved connecting the SRAM cell with its supporting circuitry. A single-bit memory setup was first verified, followed by the planning of extension toward a small array. Signals such as write enable, sense enable, and pre-charge control were synchronized to mimic real-world timing.

IV. IMPLEMENTATION

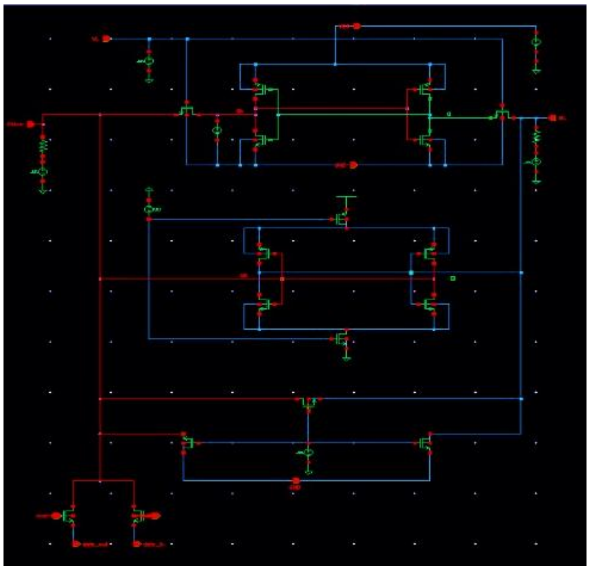

Fig.5: Schematic of 1 bit SRAM

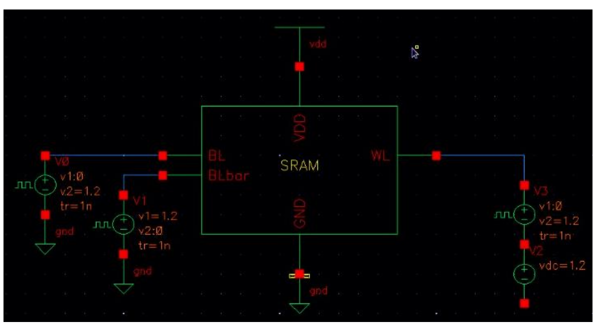

Fig. 6: Testbench of 1 bit SRAM

V. SIMULATION AND OUTPUT WAVEFORMS

A. Static Noise Margin

In SRAM analysis, the "butterfly curve" is a graphical technique used to determine the Static Noise Margin (SNM), which indicates the cell's stability against noise. It's obtained by plotting the voltage transfer characteristics (VTC) of the two inverters in a 6T SRAM cell, and the SNM is the side length of the largest square that can fit within the lobes of the resulting curve.

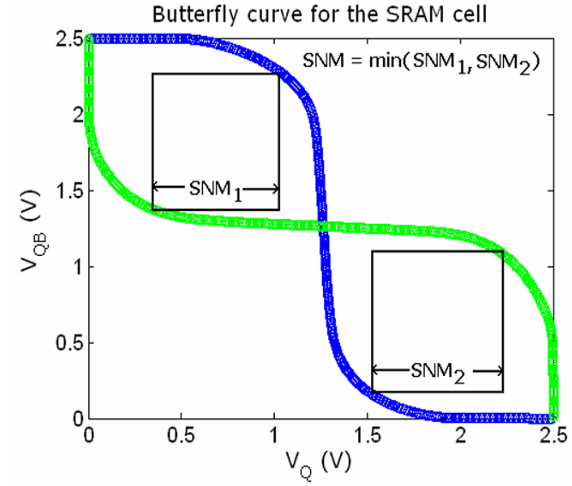

Fig. 7: Graph explaining the determination of SNM

Fig. 8: Analysis of SNM

CALCULATION OF SNM:

	V_H	V_L
SNM_1	0.25	0.15
SNM_2	0.95	0.5

Table 1: Values of SNM

SNM = min (SNM1, SNM2)

SNM1 = 0.25 - 0.10 =0.15

SNM2 = 0.95 - 0.5 = 0.45

SNM = min (0.15, 0.45) = 0.15

B. Read and Write Operation

Fig. 9: Graph of various parameters

The read and write operations in a memory cell involve a sequence of controlled signal activations to ensure reliable data storage and retrieval.

Before a write operation, the pre-charge and equalizer circuitry is enabled to prepare the bit lines. For writing a '1', a high data-in signal is applied, followed by activation of the sense amplifier and write enable. Once signals stabilize, the word line is activated to store the bit.

For reading, the pre-charge circuit is again enabled, and the read enable, sense amplifier, and word line are activated simultaneously, resulting in a high data-out. A similar procedure is followed to write a '0', with a low data-in signal, and during the read operation, the data-out goes low, reflecting the stored '0'.

SUMMARY TABLE OF READ AND WRITE OPERATIONS

Time (ns)	WL	Operation Type	Behavior
~10 ns	HIGH	Write	BL driven, Q and Qb flip
~20 ns	HIGH	Read	BL and BLbar drift, Q and Qb stable
~30 ns	HIGH	Write	New data written (Q and Qb change)
~40 ns	HIGH	Read	Bitlines drift slightly, Q and Qb hold
~50 ns	HIGH	Write	Another writes, Q and Qb change
~60 ns	HIGH	Read	Bitlines drift again, stable data

Table 2: Summary of read and write operations

VI. CONCLUSION

The project successfully demonstrates the design and functional verification of a 6T SRAM cell using the Cadence Virtuoso platform. Key components including the SRAM cell, sense amplifier, and pre-charge and equalizer circuits were implemented and tested through schematic design and transient analysis. The simulations confirmed the proper functionality of the memory operations, showcasing stable read/write behaviors. The butterfly curve analysis revealed a satisfactory Static Noise Margin (SNM), indicating reliable performance of the designed cell.

VII. FUTURE SCOPE

- Array Extension: Expanding the design to implement multi-bit or full memory arrays, including row and column decoders.
- Post-Layout Simulation: Incorporating parasitic extraction (PEX) and running post-layout simulations for more accurate performance metrics.
- Low-Power Enhancements: Exploring power gating or alternative SRAM topologies (like 8T or 10T) to improve performance under low-voltage conditions.
- Physical Verification: Further, this circuit simulation can be extended by creating the layout of this SRAM and integrating layout versus schematic (LVS) checks and tape-out level verification for fabrication readiness.
- Technology Scaling: Porting the design to advanced nodes (e.g., 65nm or below) to study scaling challenges and benefits.

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