DOUBLE NODE UPSET RHBD 12T SRAM CELL

Muthuraman S[1], Dr P Deepa [2]
[1]*PG Scholar, Department of Electronics and Communication Engineering, Government College of Technology, Coimbatore.*
[2]*Associate Professor, Department of Electronics and Communication Engineering, Government College of Technology, Coimbatore.*

Abstract **- Radiation-hardened SRAM is a crucial memory technology developed for reliable operation in harsh, high-radiation environments like space and nuclear power plants, as traditional SRAM is susceptible to radiation-induced data corruption from single-event upsets (SEUs) and double-node upsets (DNUs). To address these challenges, the Radiation- Hardened by Design (RHBD) 12T SRAM cell is proposed in this paper to offer a robust solution. This architecture incorporates two interconnected latch circuits configured in a self-recovering feedback mechanism to mitigate the risk of data corruption. The feedback mechanism restores disrupted storage nodes to their original state, ensuring data integrity even under DNUs. The RHBD 12T SRAM cell, balances redundancy and isolation for enhanced resilience. RHBT 12T SRAM cell is simulated for write, read, and hold operations to evaluate its robustness against radiation-induced faults. Simulation in the Cadence analog design at 45nm technology validates its performance. The RHBD 12T SRAM cell demonstrates improved fault tolerance, minimal transistor count, and efficient power consumption, making it a reliable choice for applications in radiation-prone environments like space.**

Index Terms - Double node upset (DNU), Static Noise Margin (SNM), Monto carlo Analysis, Dynamic Power, Static Power, Corner Analysis.

I. INTRODUCTION

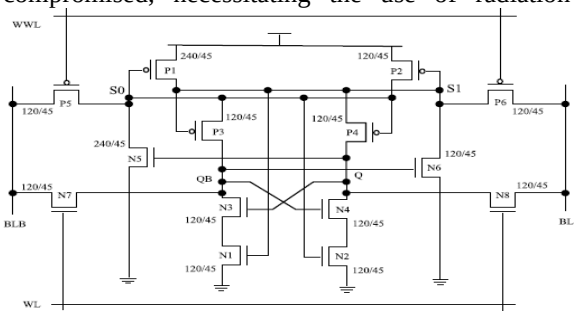
In modern electronic systems, the increasing demand for high-performance and reliable memory solutions is driven by advancements in technology [1]. Static Random Access Memory (SRAM) plays a vital role by offering high-speed data access and storage. Conventional SRAM designs face significant challenges when exposed to high levels of ionizing radiation, such as outer space, nuclear reactors, aerospace systems. Radiation- induced phenomena, including Single Event Upsets (SEUs) and Double Node Upsets (DNUs), threaten data integrity, compromise reliability, and pose risks of catastrophic failure in mission-critical applications [2].

The above challenges underscore the necessity of radiation-hardened by design (RHBD SRAM) to ensure resilience, maintain functionality, and extend the operational lifespan of memory cells in radiation-rich conditions. The SRAM cell is more sensitive to soft error such as single node upset (SNUs) and double node upset (DNUs) [3]. DNUs can leads to data corruption and mitigation them required robust error correction code (ECC) and the radiation hardened design. Radiation- induced errors can corrupt the data stored in the normal SRAM Cells.

In critical applications, such as aerospace or space missions, data integrity is of utmost importance, and any corruption can have severe consequences [4]. A DNU in SRAM occurs when two memory cells or nodes are simultaneously altered, due to external radiation or electromagnetic interference [6]. The primary issue with conventional Static Random Access Memory in environments with high levels of ionizing radiation, such as outer space or areas near nuclear reactors, lies in its vulnerability to radiation-induced errors.

Ionizing radiation, which includes high- energy particles such as protons, neutrons, or heavy ions, can interact with the electronic components of SRAM in several ways. These interactions often result in single-event effects as bit flips or soft errors, where the stored data in memory cells is corrupted. Additionally, prolonged exposure to radiation can cause permanent damage to the memory cells, leading to device degradation and failure. This susceptibility arises because SRAM relies on delicate semiconductor components that are highly sensitive to the energetic disturbances caused by ionizing radiation. in such environments, the reliability of sram can be severely

compromised, necessitating the use of radiation-



hardened or error- correcting memory solutions to ensure stable operation and data integrity [7].

The fault-tolerant mechanisms such as redundancy, isolation, and advanced error-mitigation techniques to safeguards the data integrity even under simultaneous disturbances.[8]. This susceptibility can lead to SEU and latch-up events, both of which can compromise the integrity and functionality of the memory.[9]. The DNU is mainly caused by cosmic neutrons and β paticles when hit the node [10]. It is important to note that the generated current may lead to Double Event Upsets (DEUs) in electronic circuits causing temporary or permanent changes in the state of memory cells or other electronic components [11]. The proposed 12T SRAM cell improves the speed, reduced delay, and low power consumption and achieves a balance between performance and efficiency. Comprehensive simulations and parametric analyses, including evaluations of Static Noise Margin (SNM), dynamic power, static power, and corner performance under Process, Voltage, and Temperature (PVT) variations, validate the robustness of the design [12].

II. EXISTING METHOD OF DOUBLE NODE UPSET 14T RHBD SRAM CELL

The deep sub-micron memory devices play a crucial role in space electronic applications due to their susceptibility to single-event upset and double-node upset. When a charged particle from space hit a scaled memory circuit, the critical charge of sensitive storage nodes drops, and a node upset happens across the storage nodes. The soft error immune RHBD-14T SRAM cell (SEI- 14T) for space and satellite applications is shown fig1.The SEI-14T memory cell consists of two latch circuits coupled for self-recovering and state-restoring feedback manner. In addition, SEI-14T memory cell mitigate single event upset (SEU) in all sensitive nodes and a portion of double node upset. The problems associated with the double node upset in a 14T SRAM cell is the area overhead and the increased delay of the circuit.

Fig. 1 DOUBLE NODE UPSET RHBD 14T SRAM CELL

A. BASIC WORKING OF DNU 14T SRAM CELL

The write operation of memory cell uses both bit lines as input to write the data that has been stored inside. As shown in fig 1, connect BL and BLB to GND and supply voltage, respectively, to write the stored data to logic 0 from 1. As a result, QB charges via P5 and N7 transistors and Q discharges via N8 and P6 transistors at the storage node. Additionally, Q writes data to logic 0 and N2 and N4 transistors are turned on and read operation of both bit lines (BL, BLB) are used as output lines to read data from the storage nodes during the reading process. During the connection of the bit lines to the precharge network, the word line needs to be connected to the supply voltage. In the event that a memory cell contains logic 1, the N1, N3, and N5 transistors are activated. Through the transistors N1, N3, N7, P5, and N5, the BLB value is discharged. The N2 and N4 transistors will not turn off until this process is finished. When the sensing amplifier detects a voltage difference between the bit lines of at least 50 mV, it activates and provides the necessary information of the hold operation of both the WWL (write word line) and WL word lines are turned off while the hold operation is in progress. Access transistors are therefore disabled. In addition, bitlines are connected to the supply voltage (VDD) to shorten the wakeup time of transistors. Transistors N1, N3, N5, P1, and P4 are therefore ON, and the others are OFF. Therefore, the initial data is stored in memory.

B. PROBLEM IN CONVENTIONAL SRAM

This issue is especially common in advanced SRAM technologies with smaller geometries, where densely packed nodes are more vulnerable to simultaneous disturbances. Prolonged exposure to ionizing radiation can greatly

diminish the lifespan of standard SRAM in such settings. The accumulated effects of radiation-induced problems can lead to early memory cell failures. For a 14T SRAM cell, double node upsets pose challenges such as substantial area overhead and increased circuit delays.

III. PROPOSED DOUBLE NODE UPSET 12T RHBD SRAM CELL

The proposed 12T Double Node Upset (DNU) SRAM cell is a robust memory design aimed at enhancing resilience against simultaneous upsets in two nodes, commonly caused by radiation or noise in critical applications and is shown fig 2. This proposed 12T SRAM cell incorporating redundancy and isolation mechanisms protect data integrity. Compared to traditional SRAM cells, the 12T design offers improved fault tolerance with minimal area overhead, making it suitable for environments like space. Key performance metrics include delay, power consumption, and robustness, which are analyzed under varying supply voltages and process variations. Monte Carlo simulations are used to evaluate the impact of these variations on delay, power, and noise margins, ensuring reliability. With its balance of resilience, efficiency, and compactness, the 12T SRAM cell is a valuable solution for high-reliability systems. In a double- node upset radiation hardened 12T SRAM Cell N1 and N2 function as cross-coupled inverters, while transistors P1 and P2 are connected to VDD to provide power stability. Additionally, N5 and N6 are linked through word line 1, and P5 and P6 are connected through Word line 0, enabling control of the BL and BLB data. When radiation affects the nodes Qb and Sb, causing Qb to flip and the system ensures data retention through specific transistors. The data at node Qb is retained using transistors N4, N6, P2, and P3, while the data at node Sb is preserved by transistors P1 and N5. This design effectively mitigates the impact of radiation- induced upsets, ensuring reliable data stability.

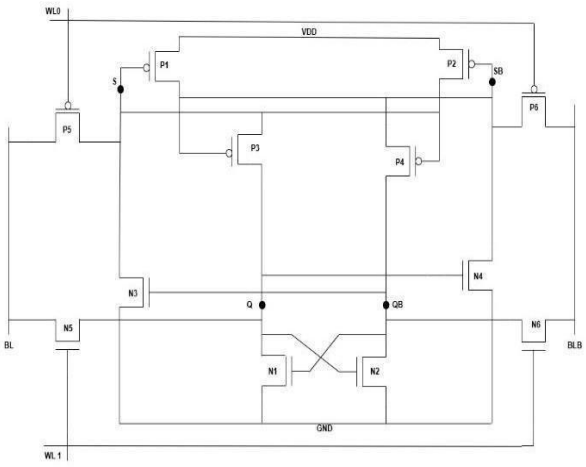


Fig. 2 PROPOSED DOUBLE NODE UPSET RHBD 12T SRAM CELL

A. BASIC WORKING OF DNU 12T SRAM CELL

The Write operation of memory cell uses both bit lines as input to write the data that has been stored inside. The stored data must be connected to GND and supply voltage for BL and BLB respectively to write logic 0 from 1.Thus Q discharges via N5 and P5 transistors and QB charges via P6 and N6 transistors Q writes data to logic 0 while the N2 transistors are active, and during the read operation, both bit lines (BL and BLB) serve as output lines to retrieve data from the storage nodes. During the connection of the bit lines to the precharge network, the word line needs to be at supply voltage. In the event that a memory cell contains logic 1, the N1 and N3 transistors are activated. Through the transistors N1, N5, P5, and N3, the BLB value was discharged. The N2 transistors will not turn off until this process is finished. When the bit lines show a voltage differential of at least 50 mV, the sense amplifier kicks in and provides the pertinent information. During hold operation both of the word lines (WL and WWL) are turned off. Consequently, the access transistors are disabled. In order to shorten the transistor wakeup time, bitlines are also connected to the supply voltage (VDD). Therefore, transistors N1, N3, P1, and P4 are turned on, and the other transistors are turned off memory therefore stores its basic data.

IV. RESULT AND DISCUSSION

The existing and proposed RHBD SRAM Cell is simulated in Cadence 45nm Technology for

double node upset (DNUs) and analyzed the performance on power, delay and stability.

A. SIMULATION OF PROPOSED 12T RHBD SRAM CELL

Fig 3 showns, the simulation of write operation where bitline 1 and bitline bar represent the data inputs. When both wl1 and wl2 are activated, the data is written to the internal nodes Q, QB, S, and SB.

Fig.3 WRITE OPERATION

B. TEST CIRCUIT OF READ OPERATION

The test circuit for the read operation in a 12T SRAM cell is designed to assess the functionality, reliability, and performance of the memory cell under various operating conditions is shown is fig 4. The circuit includes several critical components, like SRAM cell word line (WL), bit lines (BL and BLB), a precharge circuit, and a sense amplifier. During the read operation, the precharge circuit initially charges the bit lines to a predefined voltage level, ensuring balanced conditions for accurate sensing. When the word line is activated, it connects the storage nodes of the SRAM cell to the bit lines via access transistors. Depending on the stored data, a small voltage difference develops between the bit lines, which is subsequently amplified by the sense amplifier to determine the stored value.

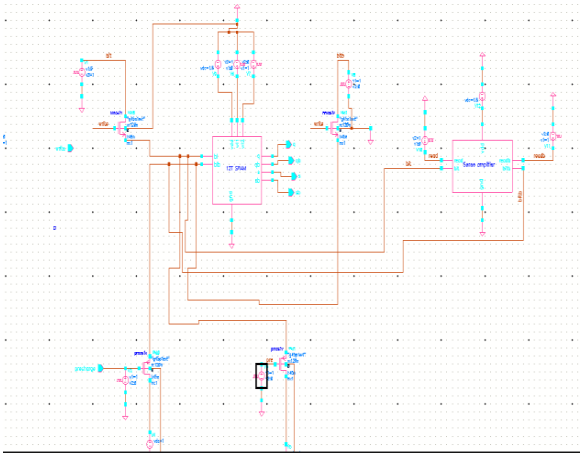


Fig. 4 TEST CIRCUIT OF READ OPERATION

C. SIMULATION OF READ OPERATION

In Fig 5 showns the read operating of 12T RHBD SRAM Cell when WL1 and WL2 are activated, they separate the read and write operations. When the write line is active, data is written to the internal nodes. When the write line is deactivated, the read line is activated to read data from the internal nodes.

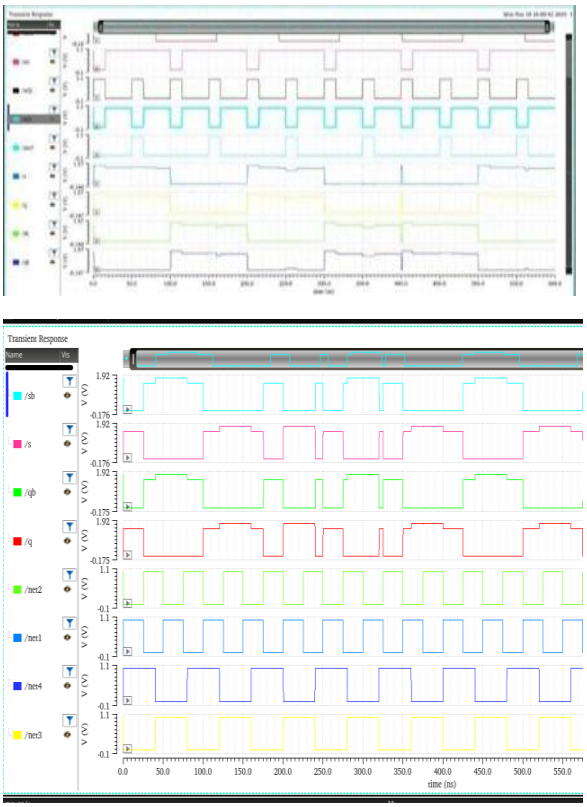


Fig 5 READ OPERATION

D. RADIATION HARDENED 12T SRAM CELL

A 12T SRAM cell is implemented with a supply voltage (VDD) of 1.8V is shown in fig 6. The input signals are configured as follows: Wordline1 transitions from 0V to 1V with a pulse width of 50 ns and a period of 25 ns, while Wordline2 transits from 1V to 0V with the same pulse width and period. Input data is provided through the bitline as a signal transitioning from 0V to 1V with a pulse width of 40 ns and a period of 20 ns. Complementary data is supplied through the bitline-bar, transitioning from 1V to 0V with the same pulse width and period. The output is observed at four pins: Q, QB, S, and SB. For the radiation- hardened SRAM, when a node is affected by a current pulse, a capacitor is connected in series with the affected node. For the affected node QB, the input pulses are a current pulse I1 of 0 µA and a current pulse I2 of 10 µA, with a capacitance value of 50 F. Similarly, for the affected node SB, the input pulses are a current pulse I1 of 10 µA and a current pulse I2 of 0 µA, with a capacitance value of 50 F. The simulation time for the radiation-hardened SRAM is

800 ns.

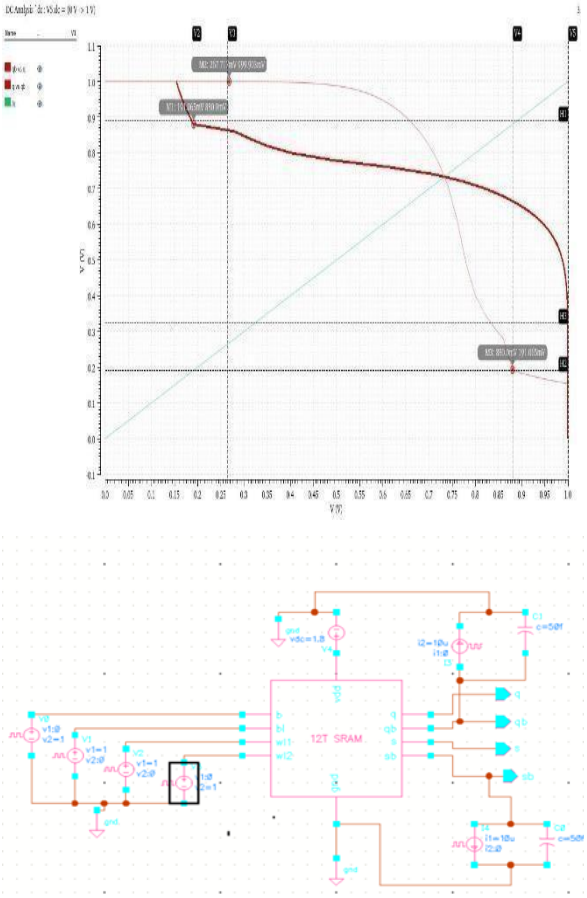


Fig. 6 RHBD 12T SRAM CELL

E. SIMULATION OF RHBD 12T SRAM CELL

The high-energy particle strikes node pair QB and S1, then QB (S1) temporarily alters stored data from 0 to 1 (1 to 0) is shown in fig 7. As a consequence, N4, N6, P2, and P3 are temporarily turned ON. This causes storage nodes Q, QB and S temporarily change the state. However, as mentioned in the SEU at QB and SEU at SB, due to the stronger transistors P1 and N5 makes SB and QB recover the flip data.

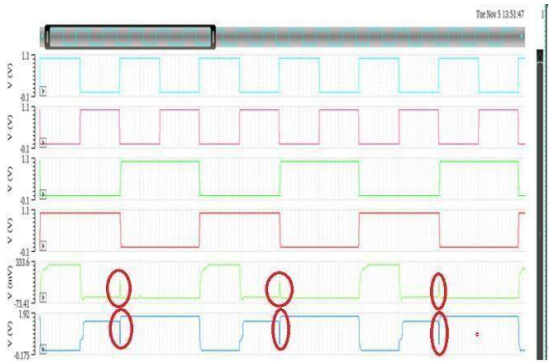


Fig 7 RADIATION HARDENED 12T SRAM CELL

V. ANALYSIS OF THE PROPOSED RHBD 12T SRAM CELL

The proposed RHBD 12T SRAM Cell is analyzed for SNM, Dynamic Power, Static Power, Corner analysis and Delay.

A. STATIC NOISE MARGIN(SNM)

As access Transistors are in the OFF state the Cell is isolated from BL and BLB Therefore there is no possibility of the state getting changed, as there will be fewer chances of Noise interference. As there is no Noise getting added, the Inverters are working with a perfect VTC as shown in above fig 8. The Hold state Static Noise Margin (SNM) is expected to be Maximum.

Fig 8 STATIC NOISE MARGIN

B. DYNAMIC POWER

The dynamic power is the power consumed by a circuit during its active operation, primarily when there is a switching of states (from 0 to 1 or 1 to 0) is shown on fig 9. It is a significant component the total power consumption of the double node upset RHBD 12T sram is 38.91pW.

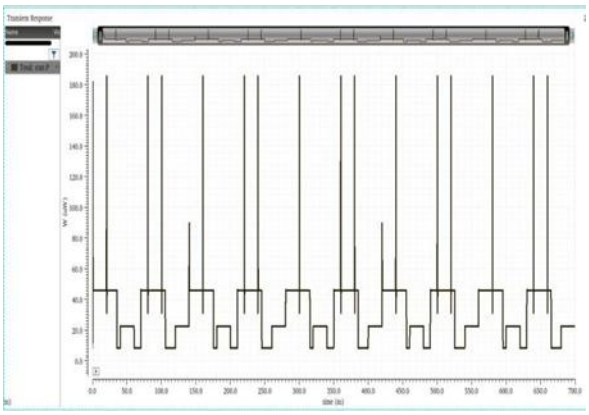


Fig 9 DYNAMIC POWER

C. STATIC POWER

The static power is the power consumed by a circuit when it is not actively switching, the circuit is in a steady state either 0 or 1 is shown in fig 10 and fig 11. It is primarily caused by leakage currents in transistors, even when no operation is being performed. In the 12T RHBD SRAM designed to mitigate Double Node Upsets (DNUs), the first node of Q, QB leakage power is 26.84pA and the second node of S, SB leakage power is 25.65pA.

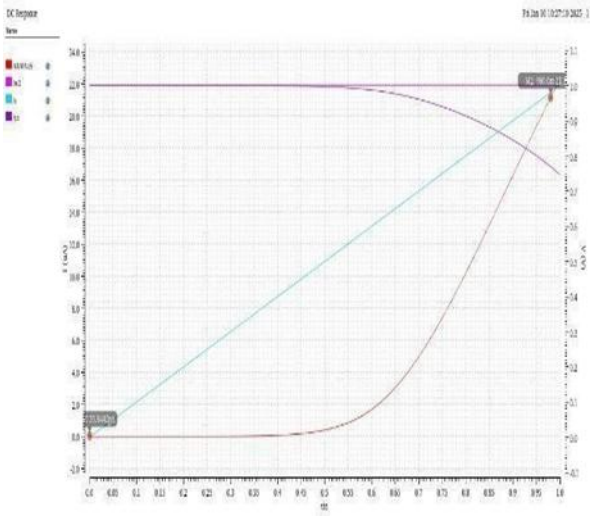


Fig 10 STATIC POWER PRIMARY NODE

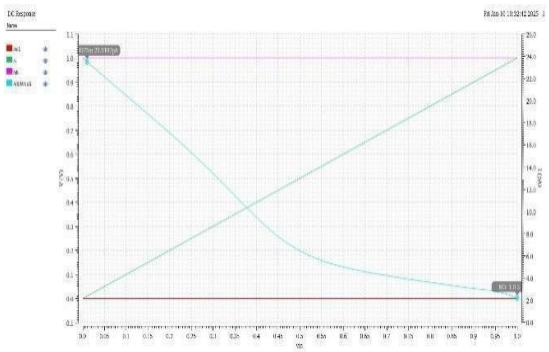


Fig 11 STATIC POWER SECONDARY NODE

D. CORNER ANALYSIS

The Corner analysis for a 12T SRAM cell involves evaluating its performance by varying the supply voltage from 1.8V to 1.0V is shown in fig in 12. This analysis is essential because, in real-world scenarios, voltage fluctuations occur in the SRAM cell. By varying the voltage within this range, the behavior of the Double Node Upset radiation-hardened SRAM cell under different conditions can be thoroughly asses.

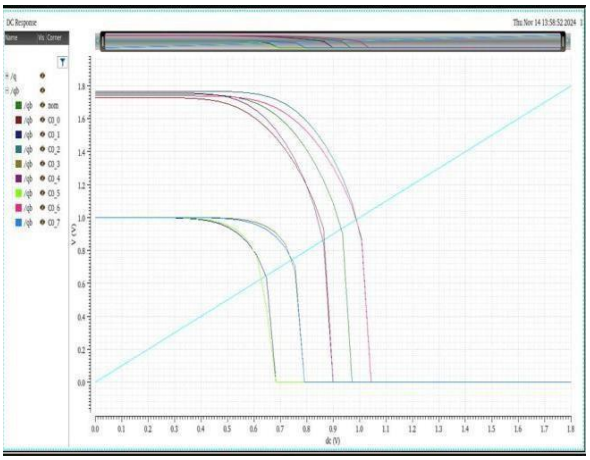


FIG 12 CORNER ANALYSIS

E. MONTO CARLO SIMULATION

The analyse Monto Carlo simulations is shown in fig13.A collection of n samples is taken to evaluate the delay, including the rising-to-falling and falling-to-rising transitions table1, as well as the total propagation delay of the double-node radiation-hardened SRAM.

TABLE 1 MONTO CARLO SIMULATION

DELAY	VALUES
Propagation delay of falling edge	20.21n
Propagation delay of rising edge	20.47n

Total Propagation delay	20.34n

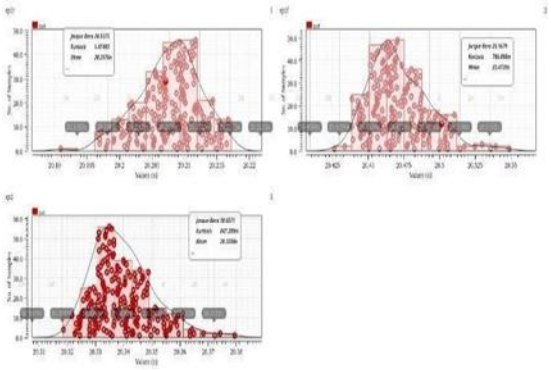


Fig 13 MONTO CARLO SIMULATION

F. COMPARISON ANALYSIS

The comparison of the Double Node Upset (DNU) radiation-hardened SRAM cells with 14T and 12T designs table2. Key parameters, including area, dynamic power consumption, and static power consumption (for Q and QB, as well as S and SB nodes), are analyzed to evaluate the performance and efficiency of both designs. The comparison highlights the trade-offs between the two architectures, offering insights into their suitability for various applications.

ANALYSIS	14T SRAM CELL	12T SRAM CELL
AREA	14T	12T
DYNAMIC POWER	51.52×10^{-9}	38.91×10^{-9}
STATIC POWER Q AND QB	26.85×10^{-9} 23.45×10^{-9}	$23.84.7 \times 10^{-9}$ 21.16×10^{-9}
STATIC POWER S AND SB	$25.65.7 \times 10^{9}$ 2.455×10^{-9}	23.54×10^{-9} 2.13×10^{-9}

TABLE 2 COMPARISON ANALYSIS

CONCLUSION

The proposed RHBD 12T SRAM cell addresses the limitations of conventional SRAM cell in high-radiation environments. The radiation hardened design, incorporating redundancy and error mitigation, ensures resilience against radiation- induced errors like DNUs. Compared to 14T designs, RHBD 12T SRAM cell offers superior fault tolerance with reduced transistor count, power and delay. Key metrics like SNM, dynamic/static power, and corner performance were evaluated and makes it suitable for critical applications. This RHBD 12T SRAM cell ensures reliable data storage and processing even in harsh environments, providing a promising solution for dependable electronic systems operating under challenging conditions and advancing the development of specialized memory for critical and emerging applications.

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