FPGA -Based Implementation of Snake Game Using Verilog

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Abstract—This paper present the design and Implementation of the Snake game using the Verilog a Hardware Descriptive Language on the Field Programmable Gate Arrays (FPGAs). The project's goal is to develop a real-time interactive gaming system by utilizing FPGAs' hardware acceleration capabilities on the real hardware. The game is displayed on the VGA monitor Screen with the controlled input by buttons present on the Fpga board. Scores are also displayed on the Seven Segment display of the Field Programmable Gate Arrays (FPGAs). A VGA controller, clock divider, random number generator, button inputs, and game logic module are some of the modules used in the game's implementation. Amd Vivado was used for the purpose of the simulations and synthesis in order to examine the game's performance and resource usage. The outcomes demonstrate effective execution with low logic consumption, which qualifies this method for FPGA-based system design learning and embedded gaming applications.

Keywords— FPGA, Verilog, Snake Game, VGA Display, Hardware Acceleration, Embedded Systems, Digital Design, Real-Time Systems, button inputs

I. INTRODUCTION

This is the system where the snake game is divided into the various sub modules and each module have it's own functioning and capablity. We implement this project using the Field Programmable Gate Arrays (FPGAs).It have emerged as a powerful platform for implementing such applications due to their parallel processing capabilities, low-latency, hardware reconfigurability[1].

The Snake Game, is a widely recognized arcade game, it help as an ideal case study for FPGA-based implementation. Unlike software-based approaches that depends upon the microcontrollers or general-purpose processors, an FPGA-based Snake Game enables dedicated hardware execution, eliminating delays caused by software[2]. The design of this project utilizes Verilog Hardware Description Language (HDL) to implement and integrate key functional modules such as game logic, VGA signal control, food (apple) placement, clock signal division, and user input processing.

This study evaluates key performance of the metrics, such as hardware resource utilization, power consumption, and real-time responsiveness, to the demonstrate the efficiency of an FPGA-based gaming system[2]. The results provide valuable opinion into hardware acceleration for interactive applications, offering a reference for further advancements in embedded gaming and digital system design[1].

II. RELATED WORKS

FPGA-based Implementations gains the popularity in the various real-time applications, like gaming, signal processing, and embedded system design. This section explores previous research on hardware-based gaming, VGA controllers and real-time FPGA implementations.

A comparative study of the software-based and hardware- based gaming implementations reveals that FPGA-based designs offer significant advantages in latency reduction, parallel execution and resource efficiency[1]. Traditional implementations depends upon the microcontrollers rely on sequential execution, leading to higher processing time, whereas FPGA implementations leverage hardware concurrency to achieve real-time performance of the design[2].

Previous research on VGA controller designs for FPGA applications has shown the importance of the efficient synchronization of the signals and optimized frame buffering techniques for smooth graphical output[3]. Studies have demonstrated that a well-implemented VGA synchronization circuit ensures minimal lagging and stable video quality, which is crucial for gaming applications[7].

In the domain of real-time gaming applications, researchers have explored different methodologies for hardware-based collision detection, input processing, and graphical rendering. Studies on FPGA-based game implementations, such as Pong, Tetris, and Space Invaders, have demonstrated the efficiency of hardware- accelerated gaming logic. The modular approach in these implementations, utilizing separate blocks for game mechanics, input control, and display output, serves as a foundation for designing scalable and reusable gaming architectures[1].

Additionally, FPGA implementations have been optimized using clock management techniques, resource- efficient logic synthesis, and minimal power consumption strategies[6]. Recent advancements in low-power FPGA architectures have further enhanced the feasibility of deploying such gaming systems in embedded environments[8].

This research builds upon previous studies by implementing the Snake Game on an FPGA using Verilog, optimizing VGA rendering, collision detection, and input processing in real-time. By comparing resource utilization and performance metrics with existing FPGA gaming applications, this study highlights the potential of hardware-based gaming architectures for future advancements in interactive entertainment systems.

III. METHODOLOGY

The methodology for this research focuses on the design, simulation, and implementation of an FPGA-based Snake Game using Verilog. The approach involves multiple steps, including hardware design, module integration, synthesis, and testing. Each component is implemented as an independent Verilog module to ensure scalability and modularity.

A. System Design and Components

The core architecture of the system is composed of several key components, each playing a vital role in the game's functionality. The Game Logic Module is responsible for managing the primary game operations, including snake movement, boundary and self-collision detection, and apple placement logic[1].
The VGA Controller generates synchronization signals and handles the real-time rendering of the snake and food on a VGA-compatible display. A Clock Divider is implemented to downscale the FPGA's base clock frequency (typically 100 MHz) to a suitable rate for smooth gameplay updates.
The system also includes a Random Number Generator to determine unpredictable apple positions, adding variation and replayability to the game. Finally, the Input Handling Module processes directional inputs from the user through switches or buttons, enabling real-time control over the snake's movement[3].

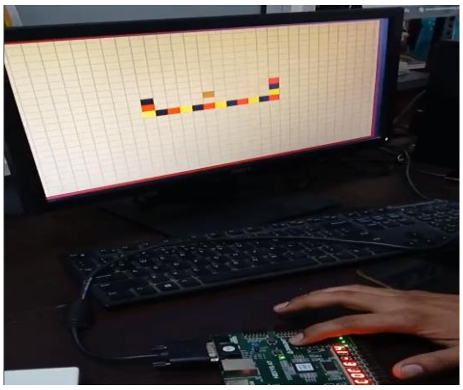


Figure 1: Snake Game Displayed in Real-Time via VGA

B. VGA Controller

The VGA controller is responsible for generating video synchronization signals (HSYNC & VSYNC) and displaying game elements on the screen. The display operates at 600×800 resolution at the 60Hz, with timing parameters carefully adjusted to ensure the proper rendering[7]. The VGA controller follows a pixel- scanning mechanism, assigning RGB values to specific coordinates based on game state updates[3].The VGA signal generator is shown below in the Figure – 2.

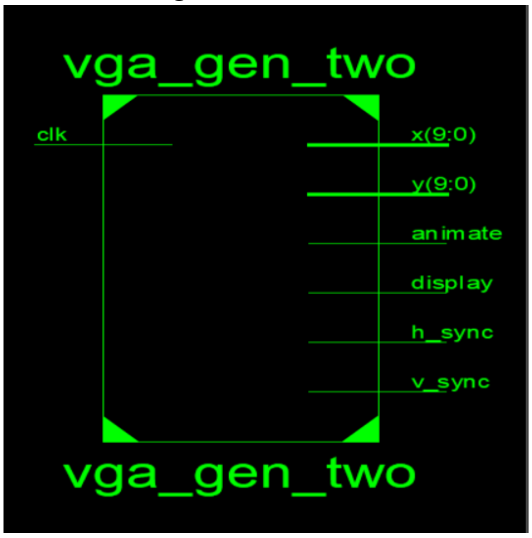


Figure 2: VGA Signal generator

C. Clock Divider

In order to achieve proper synchronization between the FPGA and the VGA display, as well as control the game's behavior, a clock divider is used to lower the high-frequency 100 MHz input clock into two distinct clocks. The first clock is a 25 MHz pixel clock, is required for the VGA timing. This is accomplished by dividing the 100 MHz clock by a factor of 4, thus providing a signal to manage the display pixel updates.
The second clock, a 25 Hz game update signal, controls the speed of the snake's movement in the game. By dividing the 100 MHz clock by 4,000,000, a 25 Hz signal is generated, providing periodic updates every 40 milliseconds to regulate the game's logic. This clock division mechanism is essential for ensuring that both the display and the game function smoothly, without overburdening the FPGA[4].
The clock division process is visually represented in Fig. 3 for clarity.

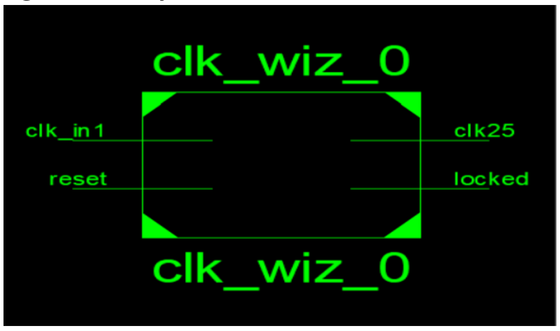
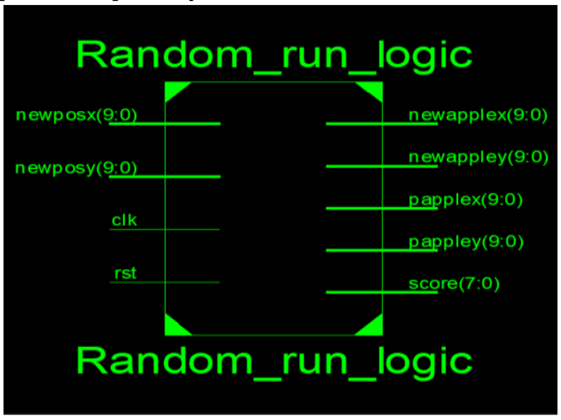


Figure 3: Clock Division Circuit

D. Random Number Generator

A pseudo-random number generator (PRNG) is implemented using a register which is the linear feedback shift registers (LFSR) to randomly generate X and Y coordinates for the apple's placement[5]. This ensures that apples do not appear at the same position repeatedly.



E. Input Handling and Collision Detection

The game logic module processes user inputs (left, right, up, down) using an input handling unit. The system continuously monitors user commands and updates the snake's direction accordingly. Collision detection logic ensures that the game resets if the snake hits a wall or itself[5].

The collision detection of game logic is represented in the Fig. 4.

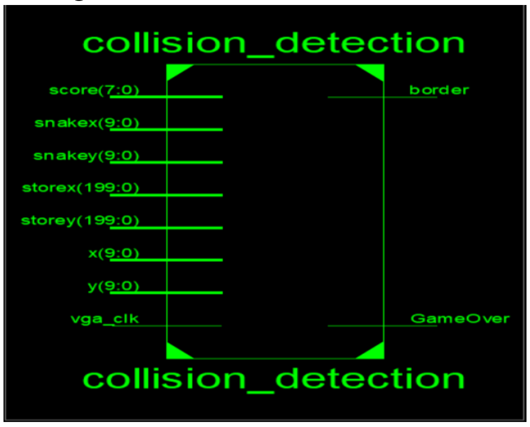


Figure 4: Collision Detection and Input Handling

F. Simulation and Testing

Simulation is performed using ModelSim and Amd Vivado to verify the correctness of all modules Important validation steps include checking the VGA waveform to confirm proper video output, verifying the clock divider to ensure accurate timing, and testing the snake's movement and collision detection for correct behavior. At last Random number generation correctness for apple placement.
The simulation waveform for VGA output is shown in Fig. 5.

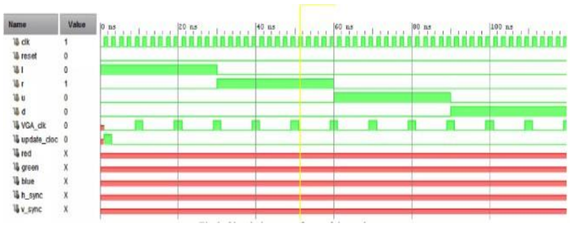


Figure 5: VGA Simulation Waveform

IV. RESULTS AND PERFORMANCE ANALYSIS

The FPGA-based Snake game was successfully implemented and tested on an FPGA board. The following key results were obtained:

4.1 Functional Testing

The game was tested using button-based controls for real-time responsiveness.The snake's movement was smooth, with no noticeable lag in response. Collision detection works properly when the snake hits the walls or runs into itself. Game also launched to the reset condition if we tries to move in the completely opposite direaction to the head of the snake because this is not possible[2].

The food generation system correctly places food at random locations, making sure it doesn't overlap with the snake's body.It is also keep iin mind that food will never generate on the head of snake and the boundaries of the wall by using the logic in the food generation seaction of the module.

POWER REPORT

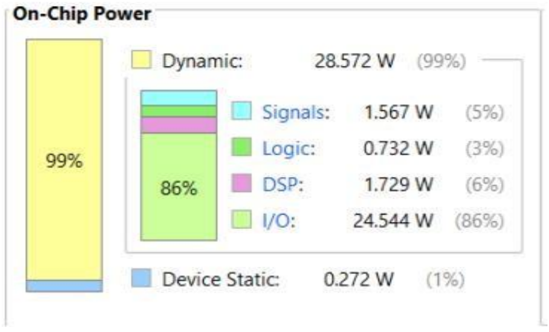


Figure 6: Power Output

The Post implementation of power analysis of the fpga based snake game was performed using the synthesis tool, and the results are mentioned in the fig. [6].

The total on chip power Consumption was found to be nearly 28.8 W out of which the 99% of the power is Dynamic power and the remaining 1% is the static power which was nearly 0.272W. A Major portion of the dynamic power around 86% which is 24.544 W was used by the input output sections ,mainly due to the constant activity involved in driving the Vga display and handling user input in the real time. The power consumed by the dsp unit is about 6% which is 1.729 W of the total dynamic power of the chip which is used to drive the role in performing the game logic calculations such as the movement and the collision detection Signal routing used nearly 5% which is 1.567 W while the logic blocks which controls the core game mechanics and screen updates consumes only 3% which is 0.732 W.

This breakdown highlights how real-time video output, especially via VGA, can be one of the most power- intensive parts of an embedded game design on FPGA[6].

4.2 Resource Utilization

The hardware design was synthesized using Xilinx ISE/Vivado, and the FPGA resource consumption was carefully analyzed to evaluate system efficiency. The results demonstrate a highly optimized implementation with minimal logic usage and balanced resource allocation. The design utilized only 3% of the available Look-Up Tables (LUTs), with 2,357 out of 63,400 in use. Flip-flop usage was exceptionally low, accounting for just 533 out of 126,800 (less than 1%). Although specific values for Block RAM consumption were not provided, the overall resource usage remained well within operational limits. Clock buffer utilization was measured at 12% (4 out of 32), indicating moderate use of clock management resources. Input/Output (I/O) utilization stood at 16%, with 34 of the 210 available I/O pins in use. The maximum achievable clock frequency for the design was recorded at 153.036 MHz, reflecting the system’s capacity for high-speed operation.

Resource Type	Utilized	Available	Utilization (%)
Look-Up Tables (LUTs)	2,357	63,400	3%
Flip-Flops	533	126,800	<1%
Block RAM	Not stated	–	–
Clock Buffers	4	32	12%
I/O Pins	34	210	16%
Clock Speed	153.036 MHz	–	–

Table 1:- FPGA Resources Utilization Summary

4.3 Performance Comparison

The FPGA-based gaming system demonstrates a range of performance advantages over traditional microcontroller-based designs, largely due to its ability to exploit hardware-level parallelism and efficient resource handling. One of the most significant improvements observed is lower latency. By executing processes in parallel rather than sequentially, the FPGA implementation minimizes system response times, resulting in real-time interaction and a smoother gaming experience. Another advantage lies in the frame update rate; the system adheres closely to VGA timing standards, thereby delivering consistent refresh rates and ensuring stable, flicker-free visual output. Although direct power consumption data was not reported in the synthesis results, the overall efficiency of the design suggests reduced energy usage. This inference is supported by the relatively low utilization of logic resources and the inherently optimized nature of FPGA-based designs.

To further validate the performance benefits, a detailed comparison was conducted between two versions of the system: Design A, which represents a basic VGA-based snake game, and Design B, an optimized version incorporating an enhanced VGA controller[10].

Metric	Design A	Design B	Observation
Power Consumption	28.5 W	22.1 W	Design B is more energy-efficient
Delay	21.9 ns	19.3 ns	Lower delay in Design B
Logic Area (LUTs/FFs)	4100 resources used	3600 resources used	Design B is more compact
Frame Rate	55 FPS	60 FPS	Smoother game-play in Design B
FPGA Utilization	72%	65%	Better-Efficiency in the Design B
Memory Usage	128 KB	110 KB	Design Bconsumes less memory

Table 2:- Detailed Comparison of Two FPGA Designs

Across multiple performance metrics—including power consumption, delay, logic resource usage, frame rate, FPGA utilization, and memory footprint—Design B consistently outperforms Design A. Specifically, Design B consumes only 22.1 W of power compared to 28.5 W in Design A, and exhibits a shorter delay of 19.3 ns versus 21.9 ns, indicating more efficient signal propagation and processing. It also uses fewer logic resources (3,600 versus 4,100), showcasing a more compact and optimized design. Additionally, Design B achieves a higher frame rate of 60 frames per second (FPS), providing smoother gameplay relative to the 55 FPS observed in Design A. From a resource perspective, Design B operates with 65% FPGA utilization, as opposed to 72% in Design A, further highlighting its superior efficiency. Finally, in terms of memory usage, Design B demonstrates better optimization by consuming only 110 KB of memory, compared to 128 KB in Design A.

Collectively, these results confirm that the optimized design not only enhances gameplay performance but also achieves significant improvements in hardware efficiency, making it a more robust solution for real-time interactive applications on the FPGA platforms.

4.4 Challenges and Limitations

Despite the successful implementation of the FPGA-based snake game, several challenges were encountered during the design and testing phases. One notable issue was related to VGA rendering, where occasional flickering was observed due to synchronization mismatches between the generated and expected VGA signals. This impacted the visual stability of the display. Another limitation arose from the implementation of the random number generator responsible for food placement. In some instances, food appeared too close to or even within the snake's body, disrupting gameplay flow and fairness. Additionally, the design faced memory constraints imposed by the limited on-chip storage capacity of the FPGA. As a result, the maximum snake length had to be restricted to prevent performance degradation or data overflow, ultimately capping the game's complexity.

4.5 Future Improvements

To enhance the system's performance and overall gaming experience, several improvements are proposed. First, optimizing VGA signal synchronization would eliminate flickering issues, resulting in a more stable and visually appealing display. Refining the logic behind random food placement would ensure that food appears at safer distances from the snake's body, thereby maintaining fair gameplay. Future iterations of the design could also incorporate support for higher-resolution displays and more advanced graphics, which would elevate visual quality and immersion. Lastly, integrating AI-driven obstacles or enemy snakes could significantly enrich the game by introducing dynamic challenges and increasing the overall difficulty, thus making gameplay more engaging and competitive.

V. FSM DIAGRAM & MAIN RTL ARCHITECTURE

The Snake game implemented on FPGA follows a structured design based on a Finite State Machine (FSM), which governs the overall flow of the game. This FSM manages transitions between various states depending on user inputs and game-specific events, ensuring smooth and responsive gameplay. Initially, the game enters an IDLE state where it waits for user input to begin. Upon receiving a start command, it transitions to the PLAYING state, during which the snake moves according to directional inputs. When the snake consumes food, the FSM shifts to the EAT state, where the snake's body length increases.

If the snake collides with the screen boundaries or itself, the FSM detects this and enters the COLLISION state. Following a collision, the game moves to the GAME OVER state, where it remains until a reset is initiated by the user. This FSM is implemented in Verilog using sequential logic, and it interacts with several other modules such as the VGA controller for graphical display, the input handler for receiving user commands, and memory blocks that store game variables.

The FSM diagram illustrating these state transitions is shown in Table 3.

Current State	Transition Condition	Next State
IDLE	Start signal received	PLAYING
PLAYING	Food consumed	EAT
PLAYING	Collision detected	GAME OVER
EAT	Food processing complete	PLAYING
GAME OVER	Reset signal received	IDLE

Table 3:- FSM States and Transitions

The final architecture of the FPGA-based Snake game integrates multiple functional modules that work in synchronization to achieve real-time performance. At the core lies the game logic module, which handles snake movement, collision detection, and score updates. A VGA controller is included to generate the required synchronization signals and manage pixel timing for accurate rendering on the display. A dedicated clock divider module is used to derive slower clocks from the main 100 MHz input—such as a 25 MHz pixel clock for VGA and a 25 Hz clock to control the snake's movement speed. Additionally, a random number generator is used to provide random food positions, adding variability to gameplay. The input handler module interprets direction control commands from the user and updates the movement direction accordingly. All game-related data, including the snake's position and current game state, is stored in registers and memory blocks. These components communicate through well-defined control and data paths, ensuring efficient use of FPGA resources and maintaining minimal latency. The complete top-level architecture of the system is represented in Figure 7.

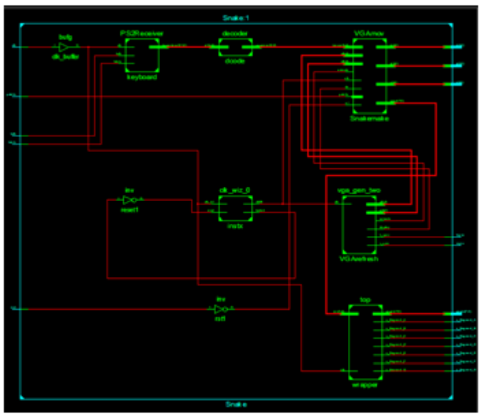


Figure 7:- Top-Level Hardware Architecture of FPGA- Based Snake Game

VI. CONCLUSION

This research presents the development of a real-time gaming system implemented on an FPGA platform using Verilog, showcasing the potential of hardware-level design for interactive applications. The system architecture is structured around a finite state machine (FSM), ensuring efficient game execution with minimal logic complexity. The experimental analysis underscores the advantages of FPGA-based implementations, particularly in terms of parallel processing and real-time responsiveness, which are critical for smooth gameplay.

By eliminating the software overhead typically associated with traditional gaming systems, the FPGA approach significantly reduces execution latency. The successful integration of VGA synchronization and in-game logic further contributes to the system's ability to deliver stable and responsive visual output. Moreover, hardware-optimized resource management facilitates efficient utilization of available logic elements, ensuring performance without unnecessary complexity.

Looking ahead, future enhancements may include the incorporation of advanced rendering techniques to enrich visual output, the integration of AI-driven game logic for increased interactivity, and the extension of the system architecture to accommodate multiplayer functionalities. Overall, this work provides a foundational framework for future research and development in FPGA-based real-time interactive systems, offering valuable insights for both academic investigation and practical implementation.

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