Single Input Single Output SEPIC converter for BLDC drive

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Abstract- **A novel converter topology is introduced for driving permanent magnet brushless DC (BLDC) motors with unipolar currents. This design features a front-end single-ended primary inductance converter (SEPIC) and a series switch for each motor phase. By grounding all switches, the topology simplifies gate drive circuits. The input voltage can be boosted, providing enhanced current regulation, which is particularly beneficial for low-voltage applications. When operating with an AC supply, the SEPIC converter functions in discontinuous conduction mode (DCM). In this mode, it acts as a voltage follower, allowing the line current to approximate the line voltage waveform. This approach reduces low-order harmonics and improves the power factor without requiring any voltage or current sensors. The simplicity, along with a reduced component count, makes this topology an attractive, low-cost solution for various variable-speed drive applications.**

I. INTRODUCTION

The simplest converter is the buck converter. Its name reflects its function, as it always steps down, or "bucks," the input voltage. The converter's output is determined by the following equation:

$$V_O = DV_g$$

By interchanging the input and output of the buck converter, is the boost converter. True to its name, the boost converter always steps up the voltage, ensuring the output voltage is higher than the input voltage. This output voltage is determined by the following equation:

$$V_O = \frac{1}{D'}V_g$$

For applications requiring the ability to step up or step down the voltage depending on the input and output levels, a solution is to use two cascaded converters—a buck and a boost. However, this approach requires separate controllers and switches for each converter. Despite this complexity, it is an effective solution in many scenarios.

The buck-boost converter has the desired step up and step down functions:

$$V_O = \frac{-D}{D'}V_g$$

The output of the converter is inverted. A flyback converter, which is an isolated version of the buck-boost converter, uses a transformer instead of a simple inductor, increasing the complexity of its design and development.

The SEPIC (Single-Ended Primary Inductor Converter) is a versatile converter that provides the required input-to-output gain. As shown in Fig. 1, the SEPIC converter has gained popularity in recent years, particularly in battery-powered systems where stepping up or down is necessary depending on the battery's charge level.
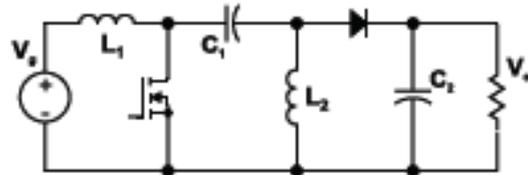

Figure 1. Sepic converter

Fig. 2 shows the circuit when the power switch is turned on. The first inductor, L1, is charged from the input voltage source during this time. The second inductor takes energy from the first capacitor, and the output capacitor is left to provide the load current. When the switch is turned ON, the input inductor is charged from the source, and the second inductor is charged from the first capacitor. No energy is supplied to the load capacitor during this time. Inductor current and capacitor voltage polarities are marked in this figure.
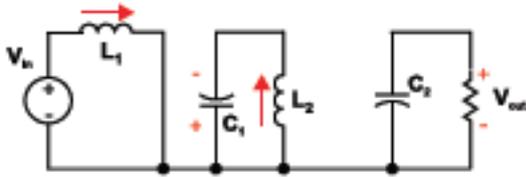
Figure 2. When the switch is turned ON

When the power switch is turned off, the first inductor charges the capacitor C1 and also provides current to the load, as shown in Fig. 3. The second inductor is also connected to the load during this time. Both inductors provide current to the load capacitor

The output capacitor sees a pulse of current during the off time, making it inherently noisier than a buck converter
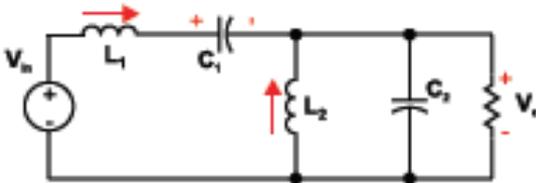

Figure 3. With the switch off

This paper makes use of the desirable properties of the single ended primary inductance converter (SEPIC) operating in the discontinuous conduction mode (DCM). At constant duty cycle, the average input current automatically tracks to some extent the sinusoidal shape of the input voltage. This is realized without the need of sensing and controlling the input current, thus simplifying the control circuit. Such a feature can be used to integrate the PFC stage with the output voltage regulation or inverter stage, which can lead to considerable cost reduction.

II. PROPOSED CONVERTER TOPOLOGY

The proposed converter with four controlled switches and diodes is shown in Fig. 4. The front-end consists of a SEPIC dc/dc converter comprised of inductors L_1 and L_2, switch S_1, intermediate capacitor C_1, diode D_1 and output capacitor C_2. The modification from the usual SEPIC configuration is that the diode D_1 is placed in the return path instead of in the positive ail. This is to block the flow of current through the phases during the periods of negative back-emf. A, B, and C are the three machine windings, and the currents through them are controlled by turn-on and turn-off of the switches S_a, S_b, and S_c, respectively. Since there is only one switch per phase, the currents through them are unidirectional. The diodes D_a, D_b

and D_c serve to freewheel the winding currents when the switches are turned off during current regulation and phase commutation. The output of the converter is used to energize the three phases of the motor, and the voltage of capacitor C1 is used to demagnetize the phases during turn-off and for current control.
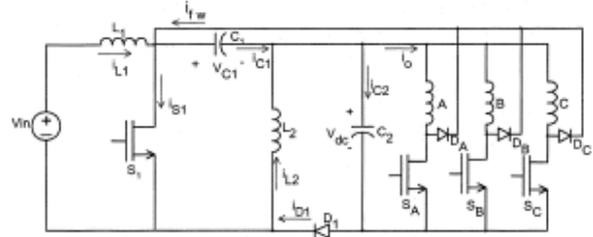

Fig. 4. Schematic of SEPIC converter-based BLDC motor drive.

Each phase is energized by turning on the corresponding switch in series with it. The equivalent circuit of phase A when switch Sa is turned on is shown in Fig.5(a). To regulate the current, Sa is turned off, which forces the turn-on of diode Da , and the flow of current through C1 as shown in the equivalent circuit of Fig. 5(b). This applies a voltage of $-V_{C1}$ across the machine winding, enabling a fast decay of the phase current.
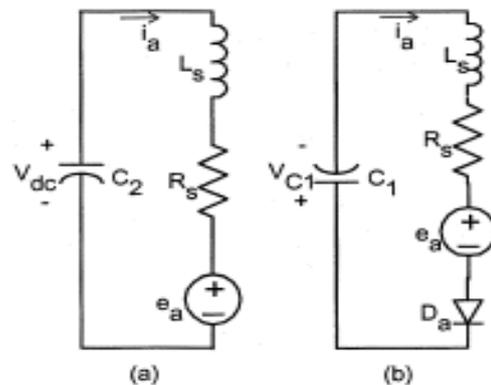

(a)   (b)

Fig. 5. Equivalent circuits of each machine phase when (a) the switch is on and (b) when the diode is conducting.

For proper demagnetization of the phase after each conduction interval and to prevent conduction during periods of negative back-emf, the instantaneous value of V_{C1} should be greater than the peak value of the back-emf E, or

$$V_{C1} > E$$

By applying Kirchoff's voltage law to the SEPIC front-end, we obtain

$$V_{in} > V_{L1} + V_{C1} + V_{L2}$$

Since the average voltages in the two inductors are zero, we get

$$V_{in} = V_{C1}$$

We obtain the peak back-emf at the maximum speed of the motor, which is given by, $E_{max}=V_{in}$ assuming that the ripple in the intermediate capacitor voltage is negligible. The maximum operating speed is then given by $w_{max}=V_{in}/K_c$

where K_c is the phase back-emf constant of the motor. If the motor is operated beyond this speed, it would result in negative torque spikes because of conduction during periods of negative back-emf.

The minimum voltage V_{dc} required is $V_{dc}=E+IR_e+L_s(dI/dt)$ where R_s and L_s are the phase resistance and inductance, and I is the phase current. At low speeds, when the back-emf is low, the switching frequency of the phase switches increases in order to regulate the phase current. The switching frequency and hence the losses at low speeds can be minimized by bucking the input voltage to lower levels at the output V_{dc}. At higher speeds, the current regulator loses its ability to force current into the phases especially during turn-on because of the high back-emf voltage. The ability of the SEPIC front-end to boost the available input voltage makes it possible to maintain current-regulated operation of the drive at higher speeds. This feature makes the proposed topology particularly suitable for low voltage dc applications such as automotive circuits.

The front-end SEPIC converter can be designed for operation either in the continuous conduction mode (CCM) or in the discontinuous conduction mode (DCM). In CCM, its voltage conversion ratio is given by

$$m = \frac{V_{dc}}{V_{in}} = \frac{D}{1-D}$$

where D is the duty cycle of the switch S_1.

In DCM, its voltage conversion ratio is given by

$$m_d = \frac{V_{dc}}{V_{in}} = \frac{D}{\sqrt{K}}$$

where, $K = 2L_1L_2/RT(L_1 + L_2)$, R being the equivalent load resistance and T the time period of switch S_1. The boundary value of K between continuous and discontinuous conduction modes, K_{crit} can be calculated $m=m_d$

$$K_{crit}=(1-D)^2$$

The converter operates in CCM when $K> K_{crit}$ and in DCM when $K< K_{crit}$. In both modes of operation, V_{dc} can be regulated at a value higher (Boost operation) or lower (Buck operation) than the input voltage V_{in}. From the controls viewpoint, it is advantageous to have the converter operating in the same mode under all load conditions. In addition, the size of the inductors and hence the overall converter can be reduced if it is operated in DCM. Hence it is proposed that the converter be designed for operation in the critical conduction mode at maximum load, so that it operates in DCM at rated load and all values less than rated load.

III. AC SUPPLY OPERATION

For applications requiring operation from an ac supply, it is desired to obtain improved power factor by using the proposed topology as shown in Fig. 6. By operating the SEPIC front-end in DCM, the following desirable characteristics are obtained
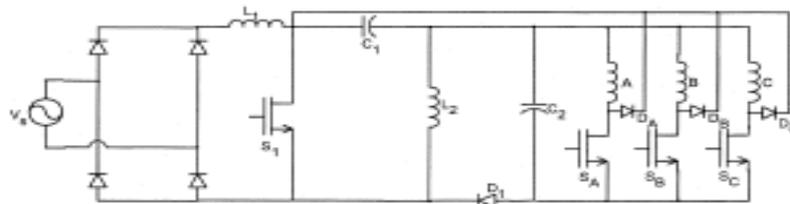

Fig. 6. Schematic of the proposed converter operating from an ac supply.

The converter works as a voltage follower, meaning that the input current naturally follows the input voltage profile (No current loop is needed), and the theoretical power factor is unity. For ideal voltage follower operation, the intermediate capacitor voltage should follow the half-sinusoidal input voltage, and goes to zero in each half-cycle. This is illustrated for the case of a resistive load in Fig. 7. However, with a unipolar BLDC motor load, the intermediate capacitor voltage has to be greater than the phase back-emf for proper demagnetization of the phases. This causes a distortion of the input current waveform around his zero-crossings of the input voltage. This is acceptable because the input current shaping is achieved at no cost to the drive, and as will be seen, the resulting power factor is better than with the conventional circuit configuration. There is a practical limit to the power level up to which dc/dc converters can be operated in DCM. This limit is reached around 300W. The use of unipolar excitation for BLDC motors beyond this power rating is also not recommended, as bipolar excitation would better utilize the machine windings. Hence, the proposed topology is well-suited to low-power, low-performance applications where cost is a major consideration.
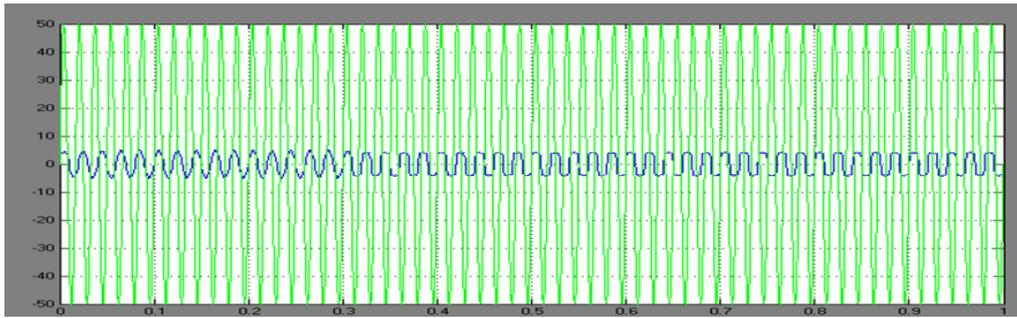
Fig. 7   Operation with resistive load: (a) input voltage and current

IV. SIMULATION AND EXPERIMENTAL RESULTS

The operation of the proposed topology has been verified by simulation is shown in Fig. 8. The rotor position is sensed by means of three hall sensors, and the position information is used to determine the phase winding to be excited. The motor speed is derived from the position inputs and is compared with the speed reference to generate the current references.

A BLDC motor with a phase back-emf constant of 12 V/Krpm is used in the design example. Because of the low back-emf constant, the input voltage is chosen to be 50 V peak. A drive with a power rating of 100 W is designed. The following equations are used for the design.

$$L_1 = \frac{V_1 dT_s}{I_{rip}}$$

$$L_2 = \frac{L_1 L_{eq}}{(L_1 - L_{eq})}$$

$$C_1 = \frac{1}{(w^2(L_1 + L_2))}$$

The actual value of C1 should be higher to minimize the voltage ripple caused by the freewheeling phase currents and is determined by simulation to be $10\mu F$.
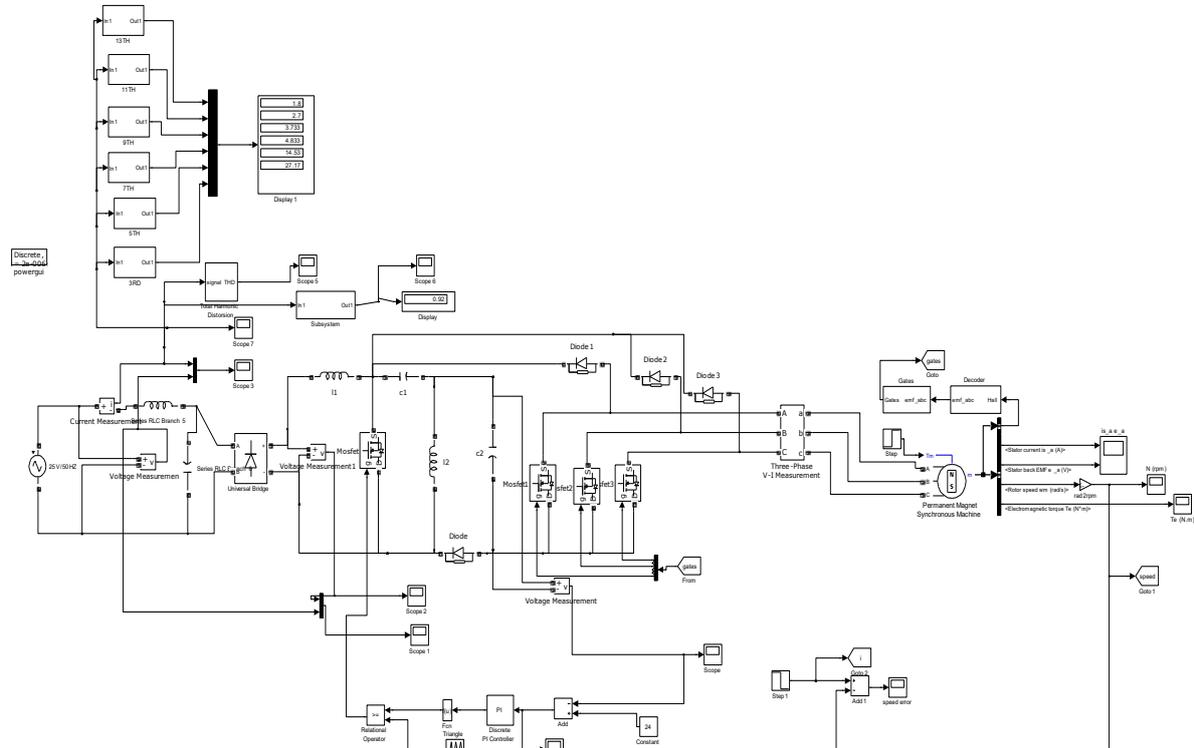

Fig 8. Proposed Converter

A PI controller is used to compare the reference and actual speed and generate the current reference. The resulting speed response is shown in Fig. 9, and the speed response to a step change in load torque in Fig. 10. The input current plotted in Fig. 11(a) is seen to follow the input voltage waveform. Fig. 11(b) shows

the intermediate capacitor voltage waveform. In an ideal PFP, this would go to zero in each half-cycle of the input voltage, but in this case, its minimum value is limited to the peak phase back-emf. This results in some distortion of the input current around the zero-crossing of the input voltage.
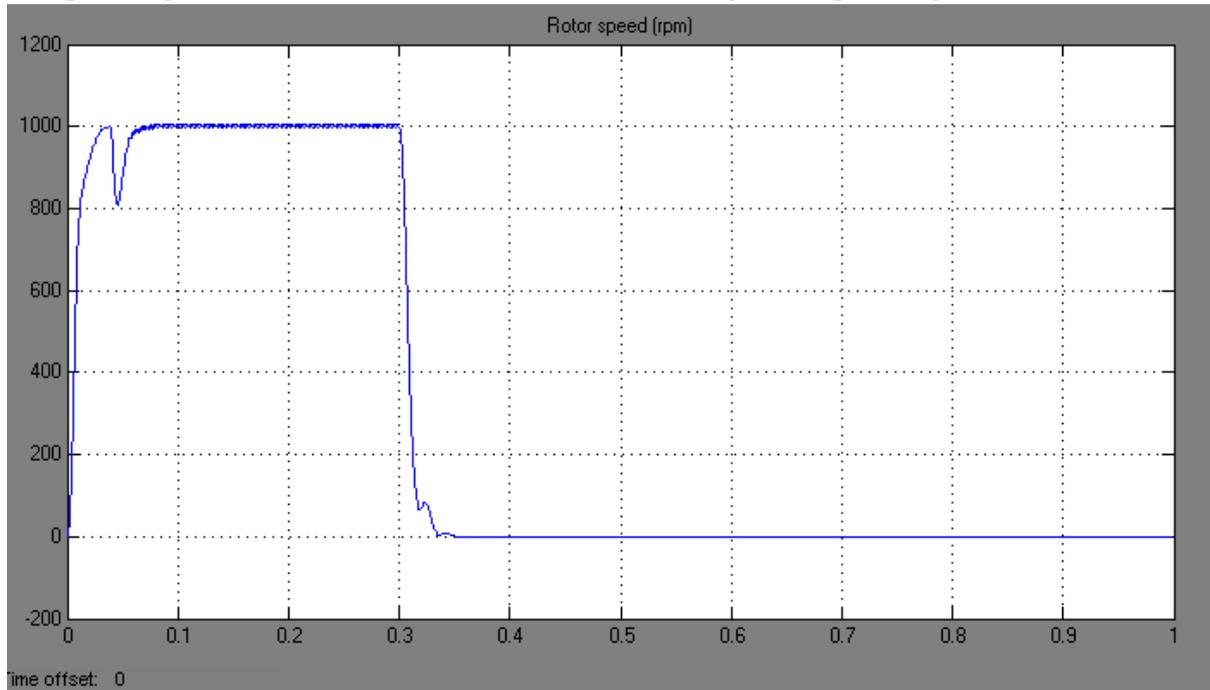

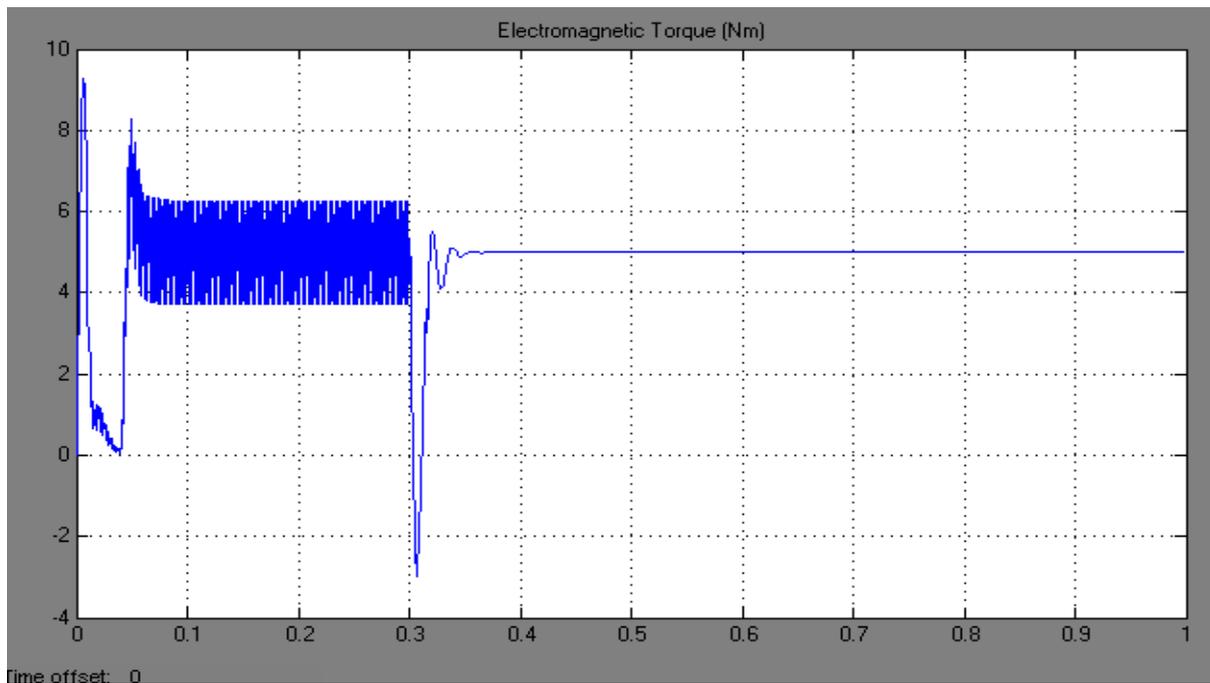Fig. 9. Speed reference and speed (rpm).

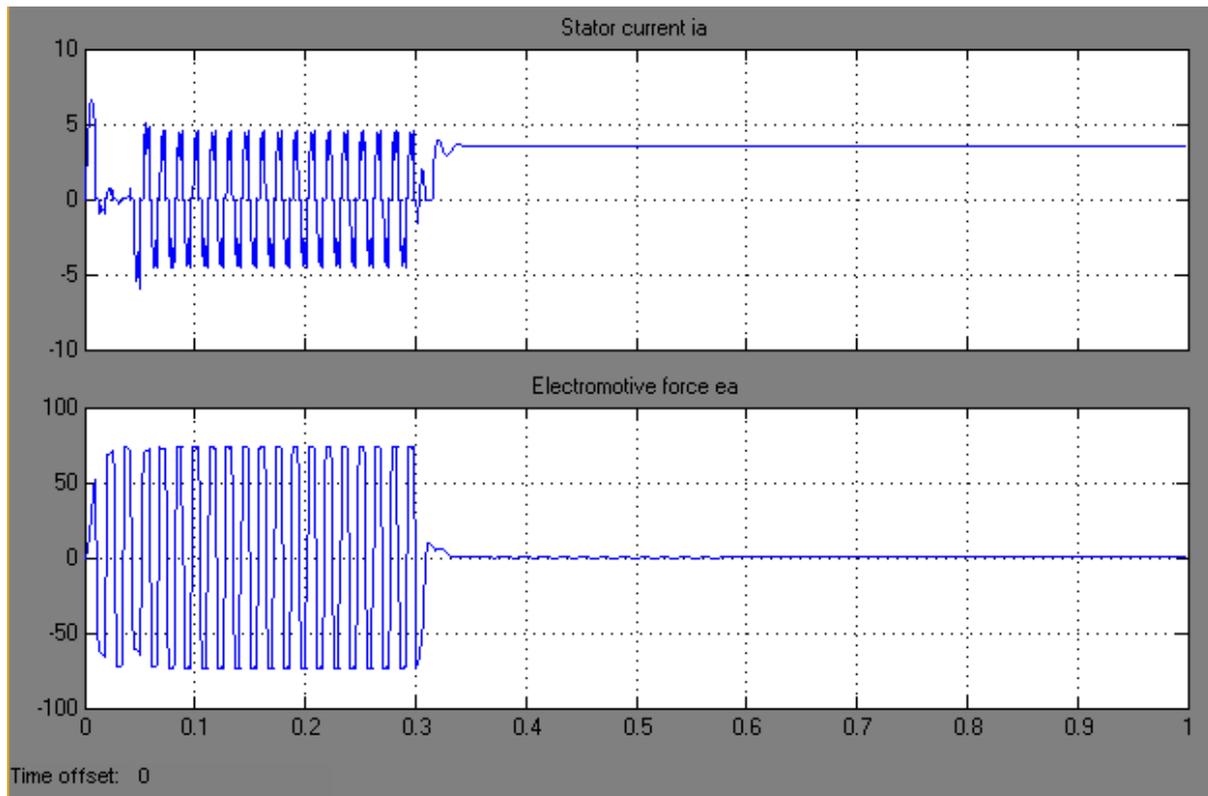Fig. 10. Speed response to step change in load torque at 0.3 s.

Fig. 11. Current and Capacitor Voltage waveforms

The performance improvement is achieved by using the proposed topology and a high power factor is also achieved over the entire speed range.

V. CONCLUSION

The proposed SEPIC converter uses only four controlled switches, all of which are referenced to ground. This considerably simplifies their gate drive circuitry and results in low cost and compact packaging. It is capable of bucking or boosting the available input dc voltage to maximize the current-regulated operation of the drive. The input current naturally follows the input voltage to a certain extent, reducing the amount of low-order harmonics and resulting in a high power factor.

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