Area, Speed and Power Comparison of Carry Adders

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Abstract - Adders are an almost necessary part of any modern integrated circuit. The requirement for the adder is that it be principally fast and tributary well organized in terms of power consumption and chip area. In this work, the applicable supervisor for adder type selection is presented, considering the relationship between delay, power consumption and area. The adders used in this work are ripple-carry adders, carry-skip adders and carry-lookahead adders. The functionality of the module and performance aspects such as area, power dissipation and propagation delay are analyzed in 0.18 µm metal layer CMOS technology using simulations and synthesized using Xilinx 8.1i. Therefore, it is suitable for applications where system speed, power and area size of the system are the main concerns. This paper also presents various adder designs that are suitable for implementing high-throughput signal processing while consuming low power. All operation of the adder chip is at 120 MHz using a 1.8 V power supply. Using 0.18 µm CMOS technology, the proposed adder unit comparison consumes only 0.0115 mW per MHz of signal encoding applications.

Keywords: Ripple Carry Adder, Carry Save Adder and Carry Look-Ahead Adder

1. INTRODUCTION

Cell-based strategy approaches such as standard cells and FPGAs, combined with general-purpose hardware synthesis, are essential for high efficiency in ASIC design. In the majority of digital signal processing applications (DSP), the dangerous operations are addition, multiplication, and accumulation. Addition is a fundamental operation for any digit system, digital signal processing or control system. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. Adders are also a very important component in digital systems since they are also used for other basic digital operations such as subtraction, multiplication, and division [1]. Therefore, improving the performance of the digital adder would go a long way in advancing the process of binary operations within a circuit composed of such blocks. Over the past few decades, many different adder architectures have been considered and planned for fast binary addition. In cell-based design techniques, they can be well considered in terms of circuit area and speed as well as correctness for logic optimization and synthesis [2].

In this paper, the design of an 8-bit adder with three types of adders is presented: Ripple carry adder, carry save adder and carry lookahead adder. The functionality and performance analysis are performed using Xilinx 8.1i. Since the circuit synthesis and design software is integrated, it provides simulation and testing tools. Two types of simulations are used to study a design: Functional simulation and timing simulation. Functional simulation is used to verify the logic of a design. It strongly integrates mixed-signal operation with digital design, implementation, circuit simulation, transistor-level extraction, and operation verification. Performance aspects such as area, power dissipation and propagation delay are analyzed for all adders in 0.18-µm metal layer CMOS technology using Xilinx 8.1i.

2. RIPPLE CARRY ADDER (RCA)

The ripple-carry adder is constructed from series-connected full adders (FA). In each stage of the ripple-carry adder, one full adder is responsible for adding two binary bit digits. The carry of one stage is passed directly to the next carry stage. Although it is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient for large bit numbers. One of the major weaknesses of this adder is that the delay increases linearly with the bitlength. The worst-case delay of the RCA is when a carry signal is exchanged through all stages of the adder bit series from least significant bit to most significant bit [3]. The delay of the RCA is directly proportional to n, the number of bits, so the arrangement of the RCA is limited as n becomes larger. The advantages of the RCA are lower power consumption and a compressed layout with an open, smaller chip area.

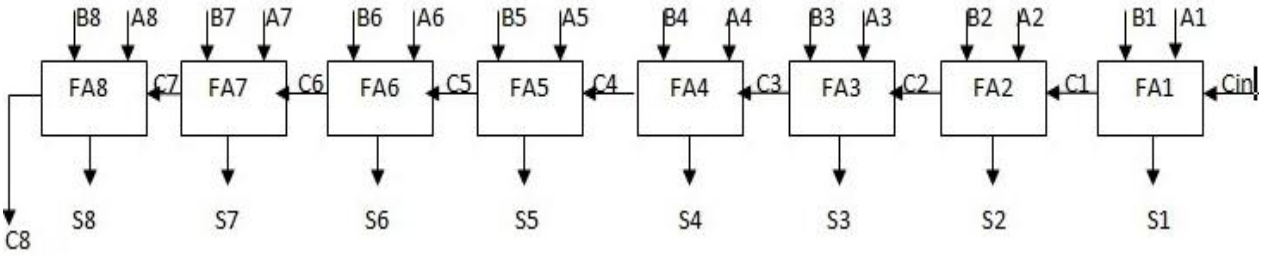


Figure 1: 8-bit Ripple Carry Adder

3. CARRY SAVE ADDER (CSA)

The carry-save adder reduces the summation of 3 numbers to the summation of 2 numbers. The propagation delay is 3 gates despite of the number of bits. The carry save adder contains n full adders, computing a single sum and a carry bit based mainly on the respective bits of the three input numbers. The entire sum can be calculated by shifting the carry sequence left by one place to the left and appending a 0 to the front most significant bit of the bounded sum order, and summing this arrangement with RCA gives the resulting value bit n + 1. This process can be persistently continued, summing one input for each stage of full adders, with no intermediate carry propagation. These stages can be arranged in a binary tree structure, with the delay increasing logarithmically with the number of inputs to be added and regularly with the number of bits per input. The main application of the carry-save algorithm is the multiplier style used for competent CMOS implementation of a much wider range of processes for high-speed digital signal processing [4]. CSA is applied in the limited product line of array multipliers to speed up the carry spreads in the array.

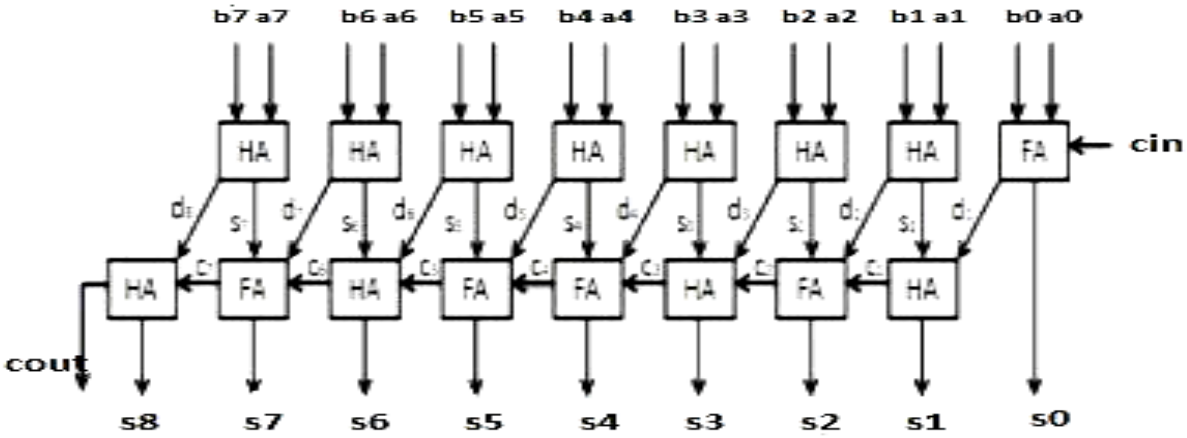


Figure 2: 8-bit Carry Save Adder

4. CARRY LOOK-AHEAD ADDER (CLA)

A carry look-ahead adder is planned to overcome the delay caused by the rippling effect of the carry bits. The propagation delay that occurs with parallel adders can be eliminated by the carry look-ahead adder. This adder is shaped to look ahead to the lower order bits of the organized and operand when a higher order carry is generated. This adder reduces the carry delay by reducing the number of gates used through which a carry signal must circulate. Carry look ahead depends on two things: a. Calculating, for each digit position, whether that position is going to propagate a carry if one comes in from the right. b. Combining these calculated values to be able to deduce quickly whether, for each group of digits, that group is going to propagate a carry that comes in from the right. The net bit effect is that carries initially propagate gradually through each group of four bits, just as in a ripple carry system, but then are carried four times faster, passing

from one look-ahead carry to the next. Within each group that accepts a carry, the carry gradually propagates within the digits of that group. This adder consists of three steps: a propagation block, a sum generator, and a carry generator.

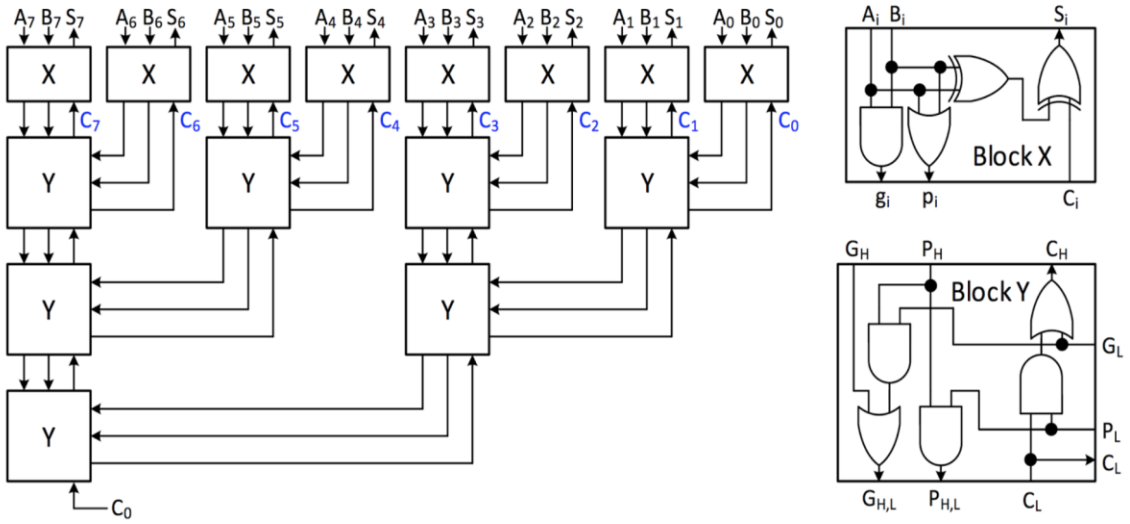


Figure 3: 8-bit Carry Look-Ahead Adder

5. RESULTS

The adder structures discussed in this paper were developed in 0.18-µm CMOS technology using Xilinx 8.1i. It highly integrates mixed-signal operations with digital design, implementation, circuit simulation, transistor-level extraction, and operation verification. Performance aspects such as area, power dissipation, and propagation delay for all adders are analyzed in 0.18-µm metal layer CMOS technology using Xilinx 8.1i. In VLSI system design, the low area, delay and power design form the main systems.

Table1: Comparison of Adders

Parameters	RCA	CSA	CLA
Supply Voltage	1.8 V	1.8 V	1.8 V
Power consumption	0.0072mW	0.0072mW	0.0072mW
Delay	0.431ns	0.339ns	0.408ns
Speed	2.320GHz	2.949GHz	2.450GHz
Power Delay	3.103fj	2.440fj	2.937fj
IC process	180nm CMOS	180nm CMOS	180nm CMOS
Area Efficient	6%	9%	5%
Gate Count	302	560	264

5.1 Power Consumption

The total power consumption using CMOS technology 0.18um is about 0.0072mW for the adder unit. The delay time is obtained from the time difference between the rising edges of the clock signal input and the rising edge of the output waveform. It also shows the tabulated result of delay values for all types of adders with CMOS 0.18um. The delay for RCA, CSA and CLA adder is 0.431 ns, 0.339 ns and 0.408 ns respectively as shown in the figures. The design speed is calculated from the reciprocal of the delay, which means that 1/delay time is equal to the speed. The total speed for the adder unit with CMOS 0.18um is 2.320 GHz, 2.949 GHz, and 2.450 GHz, respectively (see table).

RCA Project Status			
Project File:	RCA.ise	Current State:	Programming File Generated
Module Name:		• Errors:	
Target Device:	xc2s100e-7tq144	• Warnings:	
Product Version:	ISE 8.1i	• Updated:	Fri 9. Jul 10:34:01 2021

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Total Number Slice Registers	46	2,400	1%	
Number used as Flip Flops	38			
Number used as Latches	8			
Number of 4 input LUTs	64	2,400	2%	
Logic Distribution				
Number of occupied Slices	77	1,200	6%	
Number of Slices containing only related logic	77	77	100%	
Number of Slices containing unrelated logic	0	77	0%	
Total Number of 4 input LUTs	64	2,400	2%	
Number of bonded IOBs	35	98	35%	
IOB Flip Flops	2			
Number of GCLKs	1	4	25%	
Number of GCLKIOBs	1	4	25%	
Total equivalent gate count for design	802			
Additional JTAG gate count for IOBs	1,752			

Performance Summary			
Final Timing Score:	0	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Failing Constraints
All Constraints Were Met

Clock Report					
Clock Net	Resource	Locked	Fanout	Net Skew(ns)	Max Delay(ns)
clk_BUFGP	GCLKBUF1	No	40	0.128	0.431
p27/_n0003	Local		2	0.000	3.345
p23/_n0003	Local		2	0.000	3.142
p25/_n0003	Local		2	0.089	3.231
p21/_n0003	Local		1	0.000	0.619

Figure 4: Summary Report and Delay Report of RCA

CSA Project Status			
Project File:	CSA.ise	Current State:	Programming File Generated
Module Name:		• Errors:	
Target Device:	xc2s100e-7tq144	• Warnings:	
Product Version:	ISE 8.1i	• Updated:	Fri 9. Jul 11:02:02 2021

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Total Number Slice Registers	45	2,400	1%	
Number used as Flip Flops	38			
Number used as Latches	8			
Number of 4 input LUTs	64	2,400	2%	
Logic Distribution				
Number of occupied Slices	77	1,200	6%	
Number of Slices containing only related logic	77	77	100%	
Number of Slices containing unrelated logic	0	77	0%	
Total Number of 4 input LUTs	64	2,400	2%	
Number of bonded IOBs	35	98	35%	
IOB Flip Flops	2			
Number of GCLKs	1	4	25%	
Number of GCLKIOBs	1	4	25%	
Total equivalent gate count for design	560			
Additional JTAG gate count for IOBs	1,782			

Performance Summary			
Final Timing Score:	0	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Failing Constraints
All Constraints Were Met

Clock Report					
Clock Net	Resource	Locked	Fanout	Net Skew(ns)	Max Delay(ns)
clk_BUFGP	GCLKBUF1	No	40	0.112	0.339
p27/_n0003	Local		2	0.000	3.142
p23/_n0003	Local		2	0.000	3.345
p25/_n0003	Local		2	0.000	3.231
p21/_n0003	Local		1	0.000	0.619

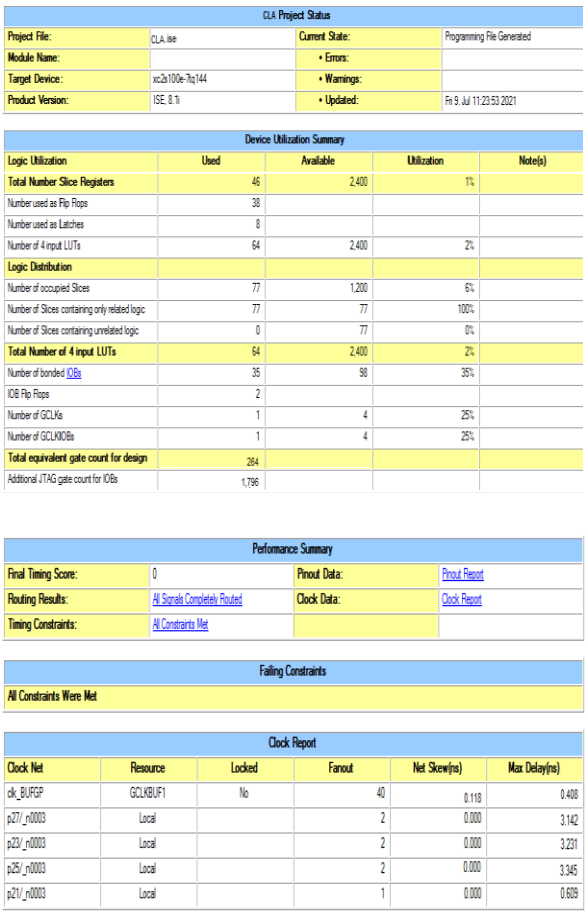
Figure 5: Summary Report and Delay Report of CSA

5.2 Power Delay Product

From the delay comparison, the maximum delay occurs for the ripple-carry adder. The minimum delay occurs with the carry look-ahead adder. The power delay product is simply the product of power consumption and time delay. The lower the value of the power delay product, the better the performance of the design, as shown in the table.

5.3 Efficient Area

As the accumulator length increases, the area size also increases. Therefore, to reduce the area, compression techniques are used. For each accumulator size, some cell area can be saved by changing the size of the efficiency and the system speed.



CLA Project Status

Project File:	CLA.ise	Current State:	Programming File Generated
Module Name:		• Errors:	
Target Device:	xc2s100e-7q144	• Warnings:	
Product Version:	ISE 8.1i	• Updated:	Fri 9 Jul 11:23:53 2021

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Total Number Slice Registers	46	2,400	1%	
Number used as Flip Flops	38			
Number used as Latches	8			
Number of 4 input LUTs	64	2,400	2%	
Logic Distribution				
Number of occupied Slices	77	1,200	6%	
Number of Slices containing only related logic	77	77	100%	
Number of Slices containing unrelated logic	0	77	0%	
Total Number of 4 input LUTs	64	2,400	2%	
Number of bonded IOBs	35	98	35%	
IOB Flip Flops	2			
Number of GCLKs	1	4	25%	
Number of GCLKIOBs	1	4	25%	
Total equivalent gate count for design	264			
Additional JTAG gate count for IOBs	1,796			

Performance Summary

Final Timing Score:	0	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Failing Constraints

All Constraints Were Met

Clock Report

Clock Net	Resource	Locked	Fanout	Net Skew(ns)	Max Delay(ns)
clk_BUFGP	GCLKBUF1	No	40	0.118	0.408
p27/_n0003	Local		2	0.000	3.142
p23/_n0003	Local		2	0.000	3.231
p25/_n0003	Local		2	0.000	3.345
p21/_n0003	Local		1	0.000	0.609

Figure 6: Summary Report and Delay Report of CLA

6. CONCLUSION

In this work, a comprehensive analysis of three types of adders in 0.18 µm CMOS technologies was performed. The performance analysis, simulation results and comparison are presented in a table and the figures above. According to the results presented, the carry look-ahead adder is the one of the three adder types that offers the best trade-off between area, speed, and power consumption, and they are suitable for circuits with high performance and low power consumption. The fastest adder is the carry-save adder, but it has a loss of area. The simplest adder suitable for low power applications is the ripple carry adder with the lowest gate count and the longest delay.

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