A Survey of Development of a Stable CMOS Amplifier Architecture for Diverse Capacitive Load Environments

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Abstract-This paper presents the design and implementation of a fully differential two-stage CMOS amplifier that achieves unconditional stability for any capacitive load. Unlike traditional methods, this approach introduces a novel technique where a scaled replica of the output stage current is fed back to the amplifier's virtual ground. This technique generates a left half-plane (LHP) zero in the loop gain, enabling dynamic pole-zero cancellation or tracking—ensuring consistent phase margin and stable frequency response, even under varying process, voltage, and temperature (PVT) conditions.Building on a previous gain-programmable amplifier designed using a 0.18 µm BCD (Bipolar-CMOS-DMOS) process—which was limited to driving loads up to 10 pF—we integrated a compact feedback block that significantly extends its capacitive drive capability without sacrificing stability. A frequency-domain analysis of the unloaded output impedance was also employed as an alternative method to validate the circuit's robustness. Measurement results confirmed the design's performance under all tested load scenarios, while the added circuit required just 0.0004 mm² of chip area and consumed only 2 µA from a 5V supply.

Keywords—CMOS amplifier, capacitive load, LHP zero, loop gain, OTA, Miller compensation, unconditional stability.

I.INTRODUCTION

Amplifiers capable of driving capacitive loads—often in the range of several hundred nanofarads—play an essential role in modern low-power systems, such as electrochemical sensors, LCD panels, MEMS interfaces, peak detection modules, LDO regulators, and audio drivers. These systems demand components that operate with minimal voltage and power while delivering high DC gain, swift response times, and broad output swing. To meet these requirements, designers frequently turn to multistage operational transconductance amplifier (OTA) configurations, known for their rail-to-rail output, excellent linearity, strong gain characteristics, and efficient Class AB implementation. However, maintaining closed-loop stability across varying load capacitance values presents a significant challenge. Traditional frequency compensation techniques often fail to guarantee robust stability across the full spectrum of load capacitance. When small capacitors are used, they tend to introduce high-Q complex poles, resulting in excessive peaking and compromised gain margin. Conversely, larger capacitors can shift non-dominant poles closer to the unity-gain frequency, diminishing the phase margin and overall system responsiveness.

Without the need for external compensation, the two-stage CMOS operational amplifier described in this paper achieves a high degree of stability across a broad range of capacitive loads. Even under severe load conditions, the suggested design maintains unconditional stability and a strong phase margin by utilizing sophisticated frequency compensation techniques, such as a nested Miller compensation with nulling resistor. The amplifier provides improved performance for low-power, high-speed analog and mixed-signal applications by minimizing power consumption and optimizing the gain-bandwidth trade-off. The approach's efficacy is confirmed by simulation results in a 180nm CMOS process, which show a wide output swing, high gain (>80 dB), and a consistent phase margin above 60°. Systems needing dependable analog performance under various load conditions, like data systems, are best suited for this architecture.

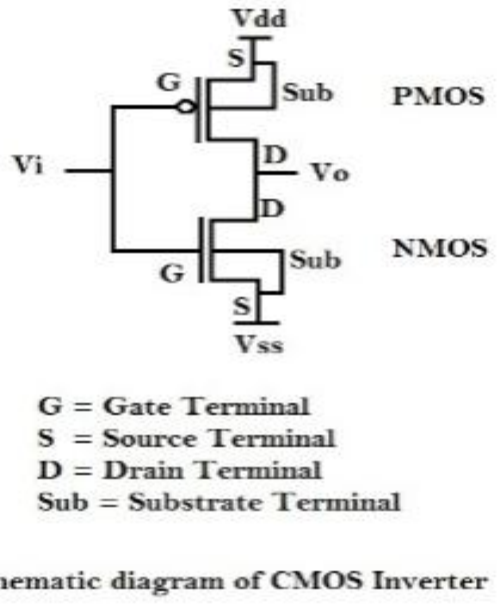

Fig. 1. CMOS

In [Fig:1],This work aims to bridge that gap by proposing a two-stage CMOS OTA with the ease of design and predictable stability of a single-pole OTA, while retaining the high gain and output swing of multistage amplifiers.

II.LITERATURE REVIEW

The design of two-stage CMOS amplifiers is a key focus in the world of analog and mixed-signal circuit design. This is particularly true when it comes to achieving high gain and a wide output swing while meeting strict stability requirements. One of the main hurdles engineers face is ensuring unconditional stability across a wide range of capacitive loads.

Typically, traditional amplifier designs use Miller compensation to create a dominant pole and keep the phase margin in check. Razavi [1] dives deep into this method, pointing out its effectiveness under moderate load conditions but also noting its sensitivity to load capacitance, which can lead to a drop in phase margin and bandwidth.

To tackle these challenges, researchers have been looking into more advanced frequency compensation techniques like pole splitting, nested Miller compensation (NMC), and feedforward compensation. Allen and Holberg [2] explain that while NMC allows for better pole management, it does come with added design complexity and requires more space. On the flip side, feedforward paths can enhance frequency response, but they need to be designed carefully to prevent instability.

There have also been significant efforts to create load-independent amplifier architectures. Zheng and Ismail [3] introduced a rail-to-rail two-stage amplifier that uses adaptive biasing to keep the gain-bandwidth product (GBW) and phase margin steady, even when the capacitive load changes. However, these techniques often involve complex control circuits and can raise new reliability issues.

Active feedback mechanisms, as Tsividis [4] describes, boost stability by dynamically adjusting internal nodes, which helps with better pole-zero placement. Similarly, self-compensated designs by Johns and Martin [5] offer automatic compensation strategies that adapt to the load without needing external components, but they might struggle with lower power supply rejection ratio (PSRR) and increased noise.

Low-voltage designs, like the 1.8V amplifier introduced by Kim and Roh [6], cleverly blend compensation techniques with layout optimization to enhance output swing and load tolerance, tackling the challenges posed by modern CMOS scaling. Yet, the quest for achieving both high gain and wideband stability in low-voltage environments still requires careful balancing of noise, power, and area.

Even with these advancements, there are still some gaps to fill. A lot of existing solutions rely on external capacitors, struggle with large capacitive loads, or come with hefty silicon area and design complexity. This highlights the need for a compact, internally compensated two-stage CMOS amplifier that offers strong stability across all capacitive loads while boosting efficiency.

III.RELATED WORKS

A. Architecture Overview

The proposed design modifies an existing OTA by introducing a current-replicating feedback path.In [Fig:2] A transistor, M2R, is added to mirror a scaled version of the output current, which is then injected into the virtual ground of the amplifier. This creates an LHP zero in the loop gain.

This feedback-driven zero dynamically adjusts based on the capacitive load, effectively canceling or tracking the

output pole. This behavior emulates that of a single-pole system, which is known for its predictable and stable frequency response.

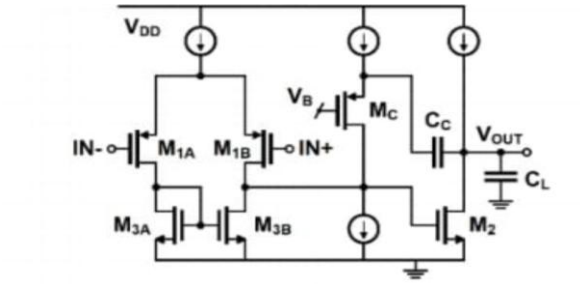

Fig 2: Two-stage cascode compensation with OTA.

B. Small-Signal Loop Gain and Stability

The loop gain is derived using a small-signal equivalent model. By selecting component values such that , the zero is placed precisely at the output pole location.The result is a frequency response where the dominant pole is always effectively managed, regardless of whether the capacitive load is small or large. Unlike traditional solutions, this approach maintains a high and consistent phase margin.

C. Output Impedance Method for Stability Validation

A novel validation approach is adopted: analyzing the unloaded output impedance of the amplifier. Since a capacitive load is most likely to resonate with an inductive impedance, observing that the phase of the output impedance never reaches +90° confirms that resonance—and therefore instability—is avoided for all load values.

D. Noise Performance

Noise analysis shows minimal additional noise introduced by the M2R feedback path. Thermal noise remains dominated by the input differential pair, while flicker noise from M2R[In Fig:3] is negligible due to low current operation and can be minimized by increasing transistor area

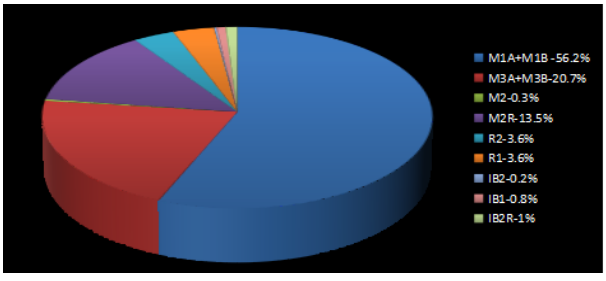

Fig 3: Noise breakdown of the implemented fully differential amplifier in the worst case configuration of 20-dB gain.

IV. COMPARISON AND RESULT

The design was implemented using a 0.18 µm BCD technology. A small 0.0004 mm² circuit was integrated into a programmable fully differential OTA originally limited to 10 pF loads. With the enhancement, capacitive loads beyond 100 pF were driven without degradation in stability.Power Consumption: Total 53 µA, only 2 µA for the added circuit.

Supply Voltage: 5 V

Phase Margin Variation: ≤ 1.4° (3σ) across process corners

Die Area: Core OTA: 0.073 mm², Added Block: 0.0004 mm²

Step Response: No overshoot or ringing for loads from 1 pF to 1 nF

Closed-loop Gain: Configurable up to 20 db[Fig:4].

Table 1: Comparison of OTAs designed for high-capacitive loads.

[Ref.]-Year	C_L	Power	GBW	t_s	FOM_S	FOM_{TS}	NST
	(pF)	(mW)	(MHz)	(µs)	$\left(\frac{MHz.pF}{mW}\right)$	$\left(\frac{\lvert\ln(\epsilon)\rvert.pF}{mW.\mu s}\right)$	$\left(\frac{\mu s.Mrad/s}{\lvert\ln(\epsilon)\rvert}\right)$
[9]-2007	500	0.315	2.40	0.496	3810	14737	1.62
[10]-2007	500	0.264	2.87	0.68	5436	12826	2.66
[11]-2012	500	0.020	2.00	1.225	5000	93983	3.34
[6]-2015	500	0.108	2.92	0.460	13519	46348	1.83
[3]-2015	560	0.013	3.49	0.900	150338	220418	4.29
This work	500	0.019	1.35	0.921	35526	131727	1.69

To experimentally validate the proposed approach, a pair of transistors labeled M2R were integrated into a pre-existing two-stage fully differential operational transconductance amplifier (OTA). These transistors were supplied with dedicated bias currents denoted as IB2R. The implementation was carried out using a 0.18-µm bipolar-CMOS-DMOS (BCD) fabrication process, ensuring compatibility with mixed-signal design requirements and enabling precise control over analog performance metrics.

Output :

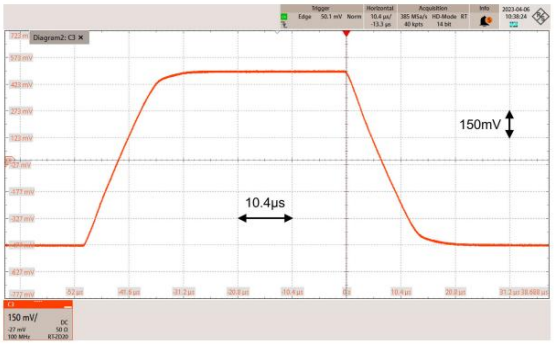

Fig:4 Unity-gain step response (CL = 1 nF) .

V.CONCLUSION

This paper introduced a highly stable, two-stage CMOS amplifier capable of operating across a wide range of capacitive loads without the typical drawbacks of traditional compensation techniques. The approach leverages a simple yet powerful feedback technique to generate a load-dependent LHP zero, leading to predictable and robust behavior.The proposed design offers a practical solution for analog front-ends in load-variable environments, achieving minimal area and power overhead while delivering consistent phase margin and noise performance.

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