Synthetic Data Generation for Text Spotting and Testing of Printed Circuit Board Using Image Processing

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***Abstract*—Chip surface defect inspection is a critical process to manufacture semiconductors with excellent performance and stable integrated circuits. In this paper, we present a cutting-edge YOLOv11-based defect inspection model, which can support real-time processing and high-precision detection. The model can detect and classify three typical chip surface defects, i.e., cracks, ink marks, and broken areas, with high precision. Innovative additions like the C3K2 block, SPFF module, and C2PSA attention mechanism improve defect localization and classification to a large extent. The model is 0.99 accurate when IoU threshold is 0.5, and it surpasses state-of-the-art algorithms. This paper verifies the feasibility of deep learning-based defect inspection in industrial control and quality control.**

***Index Terms*—Chip Surface fault, YOLOv11, Defect Detection**

I. INTRODUCTION

A. General Overview

Surface defects in semiconductor chips play a critical role in the reliability and performance of electronic devices. Detection of these defects is critical in maintaining manufacturing qual- ity. Traditional methods of inspection are manual visual ex- amination or traditional image processing, which are typically inefficient and inaccurate [1]. Deep learning, in the context of convolutional neural networks (CNNs), has been shown to be an effective replacement with high-precision automated defect inspection [2].

This work integrates the cutting-edge advancements of YOLOv11 into chip surface defect detection and presents its implementation in industrial automation. The key con- tributions of this work are, YOLOv11-based model design optimization for chip defect inspection.Innovative architectural enhancement implementation for improved feature extraction and localization.Achievement of high mean average precision (mAP) Comparison with the state-of-the-art approaches with enhanced performance [3], [5].

B. Scope Of The Project

This research covers developing and implementing a YOLOv11-based surface defect-detection automatic system to augment quality control in semiconductor manufactur- ing. Traditional defect inspection strategies that are mainly from classical image processing depend largely upon manual inspection and have many downsides, such as inefficiency and being prone to errors [7].so this study gets to deploy state-of-the-art deep learning object detection that accurately spots and classifies high-impact defects like cracks, ink and broken regions. The model is real-time, so it's very suit- able for being integrated with AOI systems when high-speed production environments are involved [9]. Additionally, the research explores transformer-based enhancements for small- defect detection and delves into semi-supervised learning to lessen the reliance on a large annotated dataset. Future work aims to optimize the model for edge deployment; that is, it will be made suitable for on-the-spot detection of defects in industrial settings. By providing the link between AI- driven defect detection and semiconductor manufacturing, this research therefore contributes toward higher production effi- ciency, less operational expenditure, and enhanced reliability in chip fabrication processes [11], [12], [13].

II. RELATED WORK

Recently scientists have used deep learning approaches to perform defect inspections. Research groups have dedicated effort to developing CNN-based models which perform auto- matic inspections of chip defects.

Cao et al. (2023) developed an auto chip package surface defect inspection framework based on deep learning which outperformed conventional inspection systems [1].The study led by Ma et al. (2022) developed an upgraded Faster R-CNN model that brought forward improved industrial application efficiency [3].Wang et al. (2022) developed a deep learning model which focuses on attention mechanism features via deep learning [4].Ullah et al. (2024) applied CNNs for inverse fea- ture matching in industrial defective chip assessments [5].Zhou et al. (2024) developed an entire pipeline model for inspecting packaging defects on chips [7].

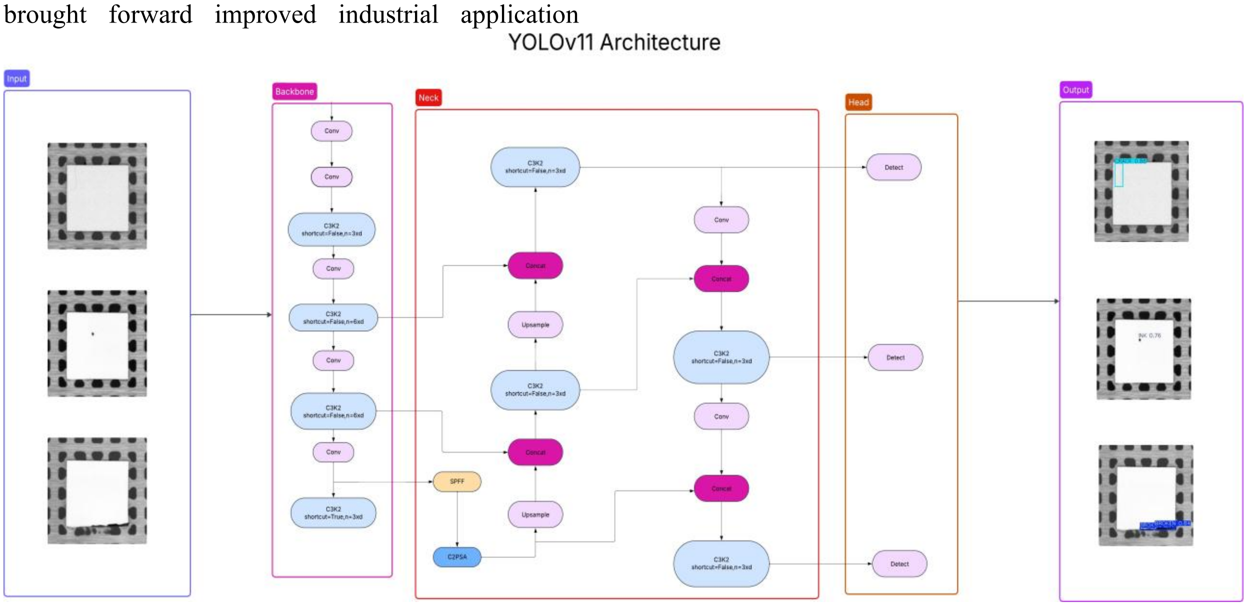

Fig. 1.

The present study advances existing models by imple- menting YOLOv11 for conducting fast and specific defect identification.

III. METHODOLOGY

There would be systematic operations in the methodology to be executed as follows:

A. System Methodology

1) Data Collection and Preprocessing:

- The collection of defect-labeled chip images included cracks and ink markings, and broken areas, with three of such types.
- There would be various data augmentations performed including rotation, flipping, and scaling, to have a robust model.
- The boxes in the YOLO annotation format indicate where the defects are situated.

B. Model Architecture

Backbone: Feature Extraction

- C3K2 Block allows CSP bottleneck computation to take place in the most efficient fashion. It enables a wider path to be concluded via convolution with the 3x3 kernel; thus, maintaining vital spatial information.
- Three-layer convolution kernels activated by SiLU com- bine to enhance the features extraction entrusted part in the model.
- The bottlenecks of residual forms permit information in the form of gradients to flow through the network pathways resembling the ResNet scaffolding.

Neck: Multi-Scale Feature Fusion

- SPFF enhances small defect identification for the network in max-pooling operations for feature gathering across varying regions.
- The head of detection gets the refined multi-scale feature maps which come out from combining layers making use of upsampling.

Attention Mechanism: C2PSA

- C2PSA enables the model to spot defect-prone areas through position-sensitive attention provided it gets a very good interpretability.
- Dual-Branch PSA Modules have two pathways of

atten- tion to optimize the spatial relevance performance while having no or little impact on computational resources.

Head: Multi-Scale Detection

- While offering the predictions at different scales, the detection head executes precise defect positioning irre- spective of their size in images.

C. Training Process

- The training process consisted of supervised learning at a learning rate of 0.001 and batch size as 16.
- The training model had basically three parts: a classifi- cation loss, a localization loss, and then confidence loss.
- The training procedure was based on transfer learning starting with the pre-trained weights from a YOLOv5 model.
- The work done on the development of the model was done in the PyTorch framework and trained on an NVIDIA RTX 3050 GPU.

IV. EXPERIMENTS PREPARATION

A. Introduction of the Data Set

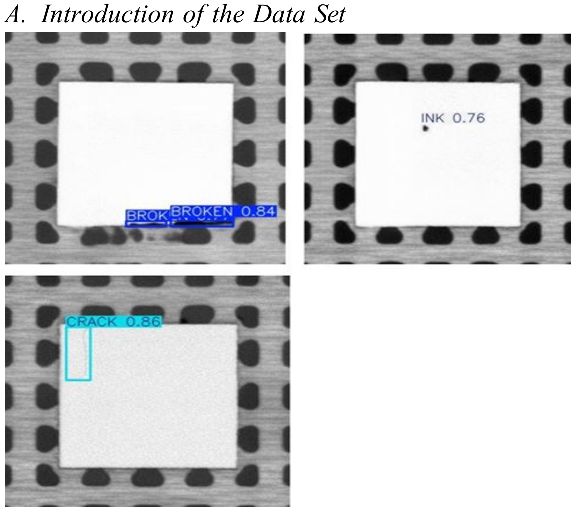

Fig. 2. Picture of the dataset

The used dataset in the research consists of 1729 high- quality scanned chip surface images, professionally labeled to designate three main categories of defects as cracks, ink marks, and broken areas. Images were sampled from semiconductor fab environments to vary the patterns of defects, light sources, and surface textures.Data augmentation processes like rotation, flip, scale, change of contrast, and injection of noise were utilized to increase the model's stability and generalization. The images were also YOLO annotated in which the rectangles marked the defect locations. Randomly the data was split into 80% train, 10% valid, and 10% test for fair representation of all defect classes

B. Model Evaluation Indicators

The evaluation metrics contain parameters such as AP, mAP, Precision, Recall, F1-Measure (F1), Parameters, and FLOPs.

1). Recall: Recall is defined as the number of true positive case detections as contrasted with the total number of true and false negative case detections. It lies within the parameters of the object's identification model evaluation, thus denoting the ability of the model to identify every object in an image.

$$Recall = \frac{TP}{TP + FP} \qquad (1)$$

2). Precision: The accuracy rate refers to the ratio of actual case detection to the sum of positive and false positives in case detection. Precision rate acts as a very important indicator used for the assessment of Accuracy in the algorithms.

$$Precision = \frac{TP}{TP + FP} \qquad (2)$$

3). F1: An F1 score is calculated by taking the average of Precision and Recall. This alone can tell how an object detection model performed based on Recall and Precision. The F1 score is a range between 0 to 1, where 1 shows that the model has performed perfectly.

$$F1 = 2 * \frac{Precision * Recall}{Precision + Recall} \qquad (3)$$

4). AP: The target detection precision model is evaluated using AP, which is the ratio of the true positive to true positive and false positive case detections.

$$Ap = \int_0^1 p(r) \qquad (4)$$

5). Mean Average Precision(mAP): mAP stands for mean Average Precision of all categories of targets detected, eval- uating the performance of the model over all detected target category classes. It is widely accepted as a benchmark against which competing target detection models are evaluated.

$$mAp = \frac{1}{n}\sum_{i=1}^{n} AP_i \tag{5}$$

V. RESULT AND ANALYSIS

The initial weight used by the model is the official weight YOLOv11.pt. The input image configuration parameters are as follows: 640 pixels by 640 pixels in size, 8 pixels in batch size, 200 iterations as the maximum, and 0.001 as the initial learning rate. From the fifty-first to the one hundred fifty iterations, the learning rate decreases gradually, with a weight attenuation coefficient of 0.0005. the optimizer used for training is SGD, learning rate is set to 0.001, and all the other parameters are kept the same. This setting allows for proper use of already available data and minimizes the time required for training. The results of training the model are as follows: mAP = 99.0 %, F1 = 0.97.

YOLOv11's performance is being compared with that of YOLOv5 and YOLOv8 in this paper. The process of experi- mental testing involved the use of the same test set where all the parameters for testing remained the same. The model was tested, compared, and analyzed to confirm improvements made on the upgraded model. The findings present YOLOv11 to be better compared to earlier models based on mAP, recall, and F1-score, which proves that it is more efficient and accurate.

TABLE I MODEL TEST RESULT TABLE

Model type	mAP	Precision	Recall	F1
YOLOv5	98.1%	100%	99%	0.95
YOLOv8	97.7%	100%	99%	0.95
YOLOv11	99.0%	100%	100%	0.97

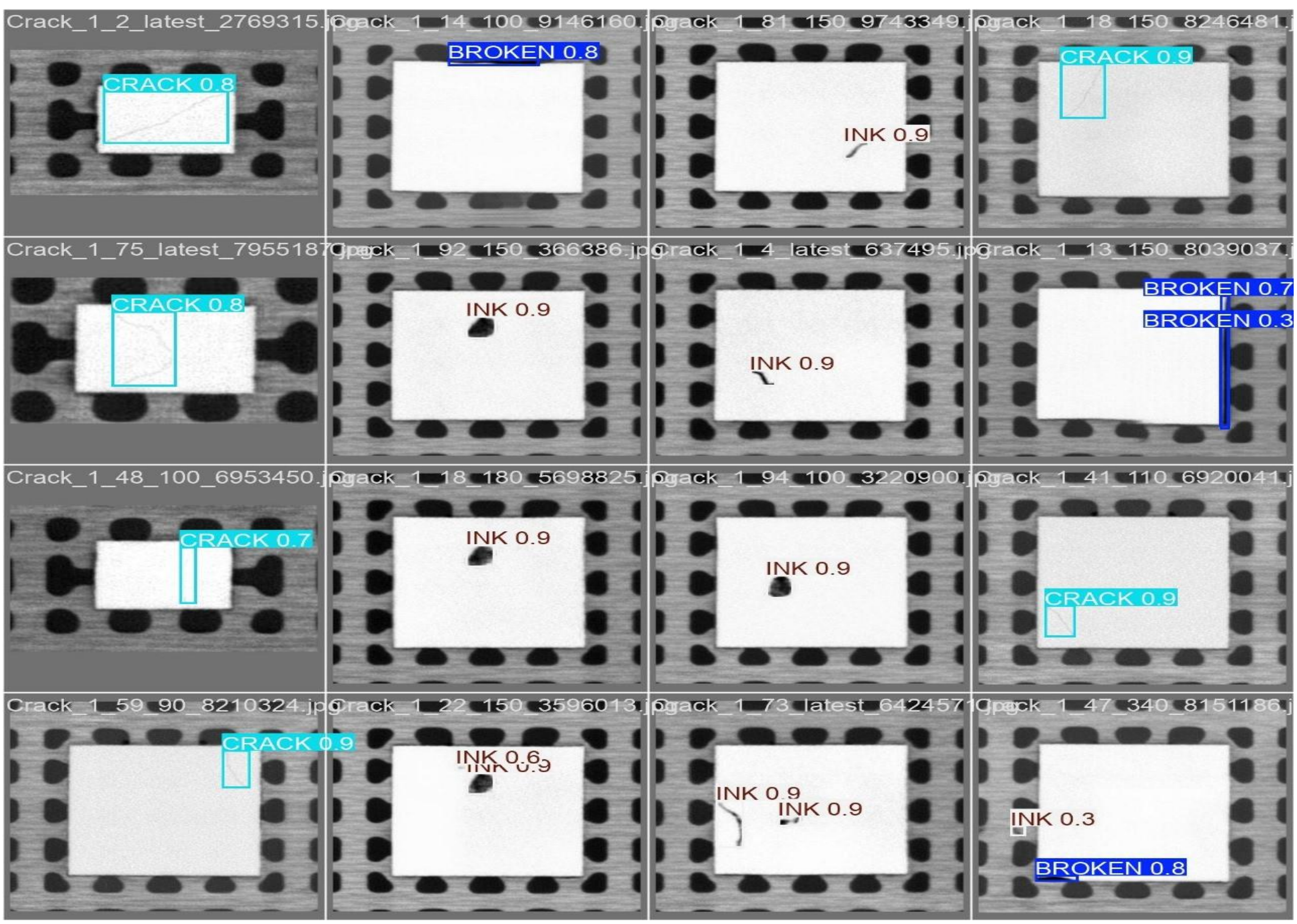

Fig. 3. Chip detection results

VI. CONCLUSION

The developed YOLOv11 model efficiently deals with var- ious obstacles when identifying defects on chips by managing defects with diverse dimensions and forms together with varying illumination conditions. The utilization of transformer- based component technology makes small and elusive defects more detectable than traditional inspection methods can han- dle. One major advantage of YOLOv11 emerges from its effective management between execution speed and identification precision. Real-time inference capacity of this model qualifies it for important industrial tasks that require immediate decision-making. The model maintains exceptional precision together with recall values which demonstrate its operational reliability. Even though the model provides attractive benefits it faces some restrictions in its function. Training YOLOv11 requires large annotated datasets that function as bottlenecks for the process. Large training computation needs and require- ments may hamper the adoption of this system for resource-limited facilities. The paper presents evidence that YOLOv11 produces superior chip defect detection that delivers high accuracy while being efficient for semiconductor manufac- turing needs. Research will evaluate additional deployment optimizations for edge computing applications due for coming examinations.

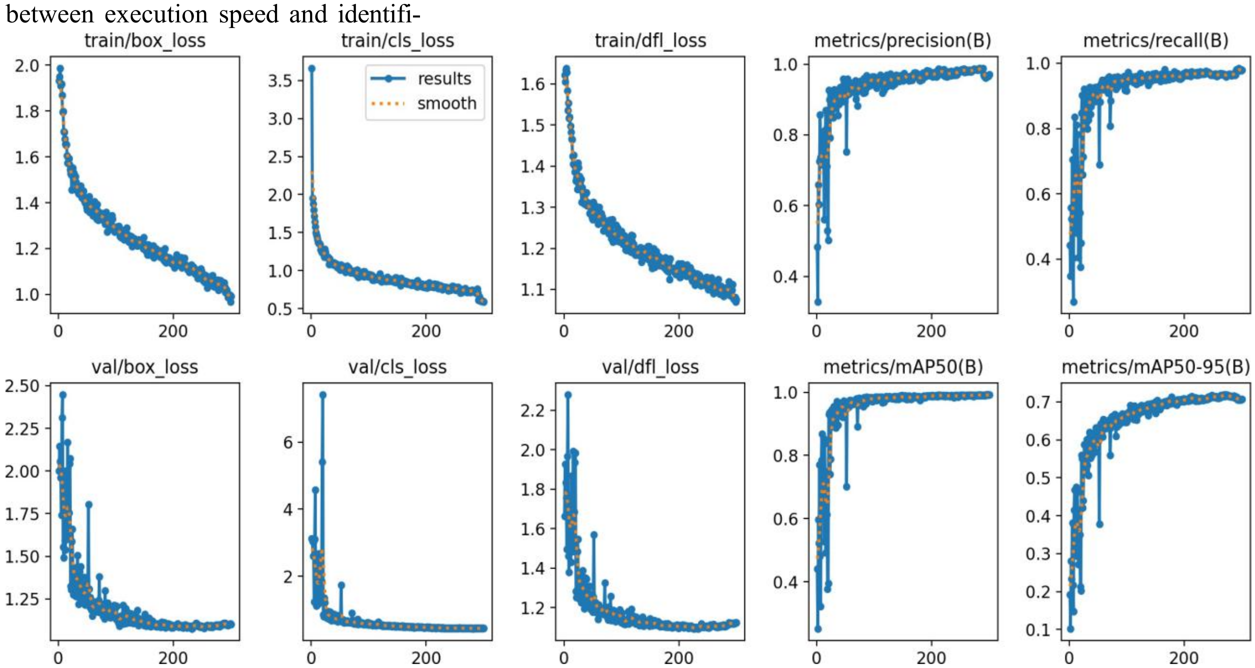

Fig. 4. Model Training Results

REFERENCES

[1] Cao, Y., Ni, Y., Zhou, Y., Li, H., Huang, Z., & Yao, E. (2023). An auto chip package surface defect detection based on deep learning. IEEE Transactions on Instrumentation and Measurement, 73, 1–15.

[2] Ruan, R., Zou, W., Li, Z., Qin, Z., Wu, Q., & Huang, S. (2024). U-Shape Network for Chip Surface Defect Detection. In 2024 IEEE International Conference on e-Business Engineering (ICEBE) (pp. 298–305).

[3] Ma, C., Chao, Y., Zhu, J., Wang, Y., Liu, W., & Han, Z. (2022). Chip Surface Defect Recognition based on Improved Faster R-CNN. 2021 27th International Conference on Mechatronics and Machine Vision in Practice (M2VIP), 1–6.

[4] Wang, S., Wang, H., Yang, F., Liu, F., & Zeng, L. (2022). Attention-based deep learning for chip-surface-defect detection. The International Journal of Advanced Manufacturing Technology, 121(3–4).

[5] Ullah, W., Khan, S. U., Kim, M. J., Hussain, A., Munsif, M., Lee, M. Y., Seo, D., & Baik, S. W. (2024). Industrial defective chips detection using deep convolutional neural network with

inverse feature matching mechanism. Journal of Computational Design and Engineering, 11(3), 326–336.
[6] Wang, X., Gao, S., Guo, J., Wang, C., Xiong, L., & Zou, Y. (2024). Deep Learning-Based Integrated Circuit Surface Defect Detection: Addressing information density imbalance for industrial application. International Journal of Computational Intelligence Systems, 17(1).
[7] Zhou, S., Yao, S., Shen, T., & Wang, Q. (2024). A novel End-to-End deep learning framework for chip packaging defect detection. Sensors, 24(17), 5837.
[8] Zhou, B., Yu, X., Zhang, Y., Chen, H., & Wang, A. (2023). Chip Surface Defect Detection Algorithm Based on Improved YOLOv3. 2023 the 5th International Conference on Video, Signal and Image Processing, 134–142
[9] Wang, J., Lin, B., Li, G., Zhou, Y., Zhong, L., Li, X.,& Zhang, X. (2023). YOLO-XRay: A bubble defect detection algorithm for chip x-ray images based on improved YOLOV5. Electronics, 12(14), 3060.
[10] Li, A., Hamzah, R., & Rahim, S. K. N. A. (2025). A chip X-ray image bubble defect detection model combined with Dual-Former attention mechanism. Measurement, 116871.
[11] Huang, H., Tang, X., Wen, F., & Jin, X. (2022). Small object detection method with shallow feature fusion network for chip surface defect detection. Scientific Reports, 12(1).
[12] Dahai, L., Zhihui, C., Xianqi, L., Qi, Z., & Nanxing, W. (2023). A lightweight convolutional neural network for recognition and classification for Si3N4 chip substrate surface defects. Ceramics International, 49(22), 35608–35616.
[13] Ren, H., Tian, M., Zhang, G., & Zhou, W. (2024). A multi-scale feature fusion network for chip surface defect detection. 2024 IEEE International Conference on Image Processing (ICIP), 957–962.
[14] Lin, Z., Ye, H., Zhan, B., & Huang, X. (2020). An efficient network for surface defect detection. Applied Sciences, 10(17), 6085.
[15] Wang, J., Zhou, X., & Wu, J. (2021). Chip appearance defect recognition based on convolutional neural network. Sensors, 21(21), 7076.