# A Seven Level Dual T Type Boost Active Neutral Point Clamped Inverter

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Abstract—This paper presents a seven-level dual T type boost active neutral point clamped inverter (ANPC) with two floating capacitors to have a voltage balance and a gain of 1.5v which will overcome the three-level active neutral point clamped inverter which requires high DC link voltage at least twice the peak of AC output voltage. So to reduce that a new topology is introduced with a voltage boosting gain of 1.5v.

*Index Terms*—Seven-Level, Boost ANPC, Multilevel Inverter, Voltage-Boosting.

#### I. INTRODUCTION

Multilevel inverters (MLIs) are considered among the most promising breed of power converters for energy conversion system and industrial applications. Numerous applications for MLIs such as renewable energy conversion systems, grid connected inverter, transportation, electrical vehicles (EV), aerospace, and other industrial systems. The MLIs produce staircase output voltage which provides amended harmonic content, reduced dv/dt, lower switching frequency and losses, higher efficiency, decreased electromagnetic interference (EMI) and fault tolerant capability. MLIs are classified into three major topologies which are the neutral point clamped (NPC), the flying capacitor (FC) and cascaded H bridge (CHB).

Many improvements have been made in developing ANPC inverters with more number of levels [3], but there was a problem of voltage balancing. So additional specially designed voltage balancing circuits are necessary to solve the problem [4-6], among which the hybrid configuration with other topologies such as flying capacitor and H-bridge inverters have been researched [7],[8], and a low voltage sub module that controls additional DC source is presented in [9], and a 3L-ANPC inverter which is widely used in industry for power conversion is presented in [1-2].

Some different ANPC inverters with switch count reduction, to increase efficiency instead of increasing the number of voltage levels is introduced, a novel 5L-ANPC inverter with compact configuration was demonstrated [10]. But the above said ANPC inverter have a problem of high DC link voltage requirement where the DC input voltage is twice the AC output voltage so a boost DC-DC converter is needed to meet the DC link voltage but these conversion from DC-AC and DC-DC structure reduces the efficiency of the system.

Research have been done on ANPC topology to eliminate boost DC-DC conversion [11], and to have a single stage DC-AC conversion based on the principle presented at [12], which reduces the DC link voltage and will have a voltage gain from half to unity.

The initiative of this letter is to give an alternative ANPC topology with voltage boosting gain and increased number of levels. Section II: Explains various previously carried out topologies on the Multilevel Inverter. Section III: Describes the proposed system and its circuit configurations, operation principles, as well as the self-voltage balance of capacitor in detail. In Section IV, a MATLAB simulation along with the Simulink model, the output voltage waveforms finally, the conclusions are presented in the last Section.

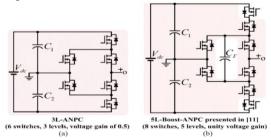


Fig.1. Active-neutral-point-clamped inverters: (a) conventional three-level ANPC topology and (b) a recent five-level ANPC topology with twofold voltage gain enhancement.

## II. RELATED WORK

Multilevel Converters: Fundamental Circuits and Systems This letter provides a chronological overview of the topology for multilevel converters, and discusses their different terminology usages and characteristics. The multilevel converters include three-level neutral-point-clamped (NPC) and neutralpoint-piloted (NPP) inverters, three-level and fourlevel flying-capacitor (FLC) inverters, and a family of modular multilevel cascade converters. Some have already been put into commercial use, some have been on a research and development stage, and others have been on an academic research stage. This paper pays much attention to six family members of the modular multilevel cascade converters, intended for grid-tied applications and medium-voltage high-power motor drives.

Multilevel Converters: Control and Modulation Techniques for Their Operation and Industrial Applications The publisher explained the operation of multilevel converters focusing on control and modulation techniques for different well-known applications. The new developments are presented as an extension of conventional methods for two-level voltage-source converters which are still the mainstream solution for most cases.

Generation of High-Resolution 12-Sided Voltage Space Vector Structure Using Low-Voltage Stacked and Cascaded Basic Inverter Cells It says about the generation of a 15-level (14 concentric) dodecagonal voltage space vector structure (DVSVS) for a star connected induction motor drive. The proposed multilevel DVSVS is obtained by cascading two inverters, namely a primary and secondary inverter. The primary inverter is a five-level (5L) structure formed by stacking two three-level flying capacitors with individual reduced dc sources and the secondary inverter is also a 5L structure formed by cascading two capacitor-fed cascaded H-bridges (CHB). The active power is supplied by the primary inverter, while the secondary inverter acts as switched capacitor harmonics filter, and capacitors in the secondary inverter are balanced naturally irrespective of load power factor for entire modulation index. The highvoltage dc supply fed primary inverter is operated in quasi-square wave mode, while the high frequency switching is applied to low voltage CHBs, thus, reducing the overall switching loss.

A Novel Hybrid Voltage Balance Method for Five-Diode-Clamped Level Converters Multilevel converters are widely employed in the 30-50 kW medium-voltage grid-connected photovoltaic (PV) generation systems due to their higher power quality and lower switching losses compared with the twolevel converters. Dual T-type three-level converters and one three-level diode neutral point clamped circuit can be integrated to derive a simplified five-level modular composited converter (5L-MCC) for the medium-voltage PV grid-connected systems. However, realizing the capacitor voltage balance is a challenge to enhance its reliability. First, the model of dc capacitor voltage variation of the 5L-MCC is discussed to expose a limitation once the nearest threevector synthesis method is employed with conventional space vector modulation (SVM). In order to extend the operational range, a hybrid space vector modulation (HSVM) strategy is proposed, which integrates the optimized SVM switching sequence for the low-modulation (M <; 0.5) and a simplified vector synthesis method for the high-modulation region (M  $\geq$ 0.5). The proposed hybrid modulation maintains the dc capacitor voltage balance over the full modulation range and power factor.

A Novel Seven-Level Hybrid Clamped (HC) Topology for Medium-Voltage Motor Drives It explains about a novel seven-level (7L) hybridclamped which competitive converter, has performance and lower device count compared to existing topologies. It can easily balance the floating capacitor voltage at the switching frequency, and therefore ensure low capacitor voltage ripples even under very low fundamental frequencies. Both multiple diode front-end and active front-end structures can be used with the proposed 7L converter, where the 7L active front end has the ability to balance the dc-link capacitors.

Operation and Control Scheme of a Five-Level Hybrid Inverter for Medium-Voltage Motor Drives. Researcher said about control method for a five-level hybrid flying-capacitor (5L-HFC) inverter, of which structure stems from the conventional five-level active neutral-point-clamped (5L-ANPC) topology by dividing the dc-link stage into three connected capacitors. In this inverter, the voltage stress on the power switches connected to the dc link is reduced by a half compared with that of the 5L-ANPC topology, thus the lower number of equally voltage-rated power

devices can be employed. Also, the power losses in the 5L-HFC inverter are more evenly distributed than in the 5L-ANPC.

## III. PROPOSED SYSTEM

Fig.2 demonstrates the circuit topology of the system. It employs a single dc source, two capacitors, two floating capacitors, and only ten mosfet switches. To obtain a seven-level output and 1.5v boost with the help of two floating capacitor C<sub>F1</sub> and C<sub>F2</sub>, with a magnitude of each level 0.5V<sub>dc</sub>. The floating capacitor C<sub>F1</sub> is charged to V<sub>dc</sub> when switch S4 and S9 are ON during 0.5 V<sub>dc</sub> and -1.5 V<sub>dc</sub> and C<sub>F2</sub> is charged to V<sub>dc</sub> during 1.5  $V_{dc}$  and -0.5  $V_{dc}$ . The floating capacitors operate symmetrically for each half cycle, which results in self-balancing of their voltages during operation. All the switches experience same voltage stress and current stress. By seeing the above circuit operation, it implies the superiority of the proposed seven level dual T type boost ANPC inverter in attaining enhanced voltage boosting gain and generation of increased number of levels.

The topology generates seven output voltage levels, i.e., zero,  $\pm 0.5$ Vdc,  $\pm$ Vdc, and  $\pm 1.5$ Vdc. The switching table for the proposed topology with the tertiary mode is given in Table 1.

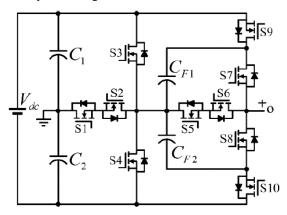


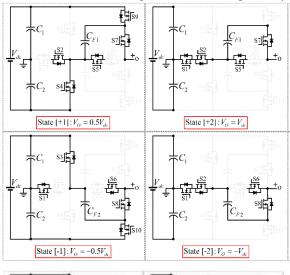
Fig.2. Proposed System

|    | 0 | +0.5     | +V | +1.5     | -    | -  | -    |
|----|---|----------|----|----------|------|----|------|
|    |   | $V_{dc}$ | dc | $V_{dc}$ | 0.5V | V  | 1.5V |
|    |   |          |    |          | de   | dc | de   |
| S1 | 1 | 0        | 1  | 1        | 1    | 1  | 0    |
| S2 | 1 | 1        | 1  | 0        | 0    | 1  | 1    |
| S3 | 0 | 0        | 0  | 1        | 1    | 0  | 0    |
| S4 | 0 | 1        | 0  | 0        | 0    | 0  | 1    |

| S5 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
|----|---|---|---|---|---|---|---|
| S6 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| S7 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| S8 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| S9 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| S1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0  |   |   |   |   |   |   |   |

Table 1. Switching combinations

The current flowing paths and the states of switches at each level are shown in Fig.3 and Table I, respectively.



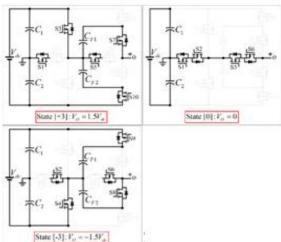


Fig.3. Current flowing paths and components states at different voltage levels

As shown in Fig 3, to obtain  $+0.5V_{dc}$  switches S2, S4, S5,S7,S9 will be closed and thus these switches only conduct,  $C_{F1}$  is charged to  $V_{dc}$  and all other remaining switches will be open and to get  $+V_{dc}$  switches S1, S2,

S5, S7 will be closed and it conducts,  $C_{F1}$  will gets discharge, for  $1.5V_{dc}$  switches S1, S3, S5,S7,S10 will conduct and  $C_{F1}$  is discharging and  $C_{F2}$  is charged to  $V_{dc}$  for  $-0.5V_{dc}$  switches S1 S3, S6, S8,S10 will be closed and  $C_{F2}$  will gets charged to  $V_{dc}$  to obtain  $-V_{dc}$  floating capacitor  $C_{F2}$  discharges, switches S1, S2, S6 and S8 will be closed. For  $-1.5V_{dc}$  floating capacitor  $C_{F2}$  discharges and  $C_{F1}$  charges, switches S2, S4, S6, S8 and S9 will be closed and thus these switches only conduct and all other remaining switches will be open. Similarly, to obtain  $0V_{dc}$ , switches S1, S2, S5, and S6 will be closed and all other switches will remain open. So it implies the enhanced arrangement of floating capacitor to have a voltage balance and voltage boosting gain.

|              | 3L-    | 5L     | 7L Boost  |
|--------------|--------|--------|-----------|
|              | ANPC   | Boost- | Dual T    |
|              |        | ANPC   | type ANPC |
| Number of    | 3      | 5      | 7         |
| levels       |        |        |           |
| Number of    | 6      | 8      | 10        |
| switches     |        |        |           |
| Maximum      | 0.5Vdc | Vdc    | 1.5Vdc    |
| level Vmax   |        |        |           |
| Voltage gain | 0      | 1      | 1.5       |
| Number of    | 0      | 1      | 2         |
| floating     |        |        |           |
| capacitors   |        |        |           |

Table 2 Comparison between the proposed topology with the 5L-boost ANPC and 3L-ANPC

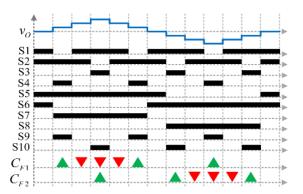


Fig.4. Waveform of the proposed seven level dual T type boost active neutral point clamped inverter.

#### IV. SIMULATION RESULT ANALYSIS

The simulation of the proposed system is demonstrated in the MATLAB as shown in Fig.6. Here

ten switches are connected in the appropriate topology with two floating capacitors are placed as shown in Fig.6. The switches are provided with appropriate pulses using sinusoidal PWM method. A voltmeter is used across the load to measure the output voltage and the waveform is observed using a scope connected to the voltmeter.

In the simulation of the proposed structure, an optimized sinusoidal PWM method is used for control strategy. Fig.5. demonstrates the modulation logic. According to Table I, the simple logic circuits or a look-up table method of the controller can be used for the PWM signals of the switches. There waveform can be seen in Fig.7.

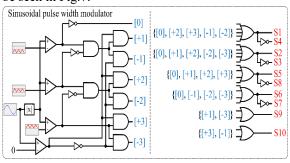


Fig.5. Sinusoidal PWM modulation strategy and logic for the proposed topology

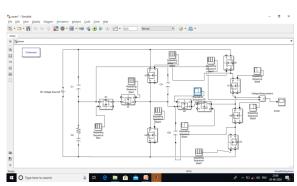


Fig.6. Proposed System in MATLAB

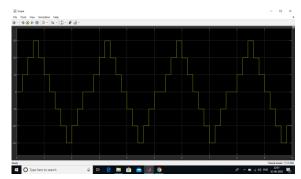


Fig.7. Seven level simulation output voltage waveforms in MATLAB

The simulation of the proposed topology of seven level dual T type boost active neutral point clamped inverter structure is observed in the MATLAB Fig.6. The simulation results shows that the output voltage is boosted 1.5 times of the input voltage with seven-levels in Fig.7.The input 100 V is given to obtain an output voltage which is 1.5 times the input i.e., 150V. The self-balancing of the capacitors can be observed in the simulation with higher efficiency. This simulation can be converted to the experimental prototype to obtain the desired output.

Similarly, the proposed topology can be used to obtain the five-level voltage output by providing the appropriate PWM pulses. By providing required pulses to the eight switches shown in Fig.8, the output voltage with five level is obtained in Fig.9 as shown. Here the input of 100V is provided to obtain a fivelevel output voltage with peak output voltage 100V.

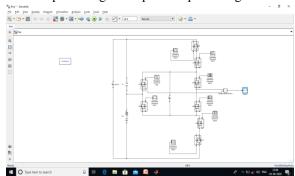


Fig.8. Simulink model for five level boost ANPC

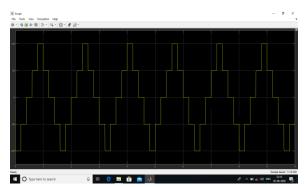


Fig.9. Output waveform of five level boost ANPC.

Similarly, the proposed topology can be used to obtain the three-level voltage output by providing the appropriate PWM pulses. By providing required pulses to the six switches shown in Fig.10, the output voltage with three level is obtained in Fig.11 as shown. Here the input 50V is provided to obtain a three-level peak output voltage 25V.

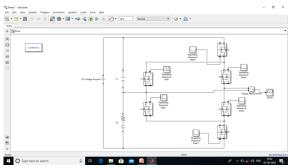


Fig.10. Simulink model for 3L-ANPC.

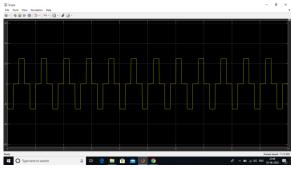


Fig.11. Output waveform of 3L-ANPC

From the above 7, 5 and 3 level output model and waveform we can clearly observe the voltage boosting gain of 1.5 times in seven level and in five level DC link voltage is gained from half to unity and in three level the output voltage is half the input voltage

#### V. CONCLUSIONS

The proposed seven level dual T type boost active neutral point clamped inverter has the 1.5 times boost ability with reduced components and self-voltage balancing capacitors. The proposed topology employs only ten switches and without any higher efficient conversion with reduced complexity of control and less cost of the converter. Thus, this converter topology can become handy in the renewable energy Finally, sources applications. the prototype experiment with sinusoidal PWM method can be implemented on the lines of the simulation to further verify the feasibility.

## REFERENCES

[1] H. Akagi, "Multilevel Converters: Fundamental Circuits and Systems," Proceedings of the IEEE, vol. 105, no. 11, pp. 2048 - 2065, 2017.

- [2] J. I. Leon, S. Vazquez, and L. G. Franquelo, "Multilevel Converters: Control and Modulation Techniques for Their Operation and Industrial Applications," Proceedings of the IEEE, vol. 105, no. 11, pp. 2066 - 2081, 2017.
- [3] A. K. Yadav, M. Boby, S. K. Pramanick, K. Gopakumar, L. Umanand, and L. G. Franquelo, "Generation of High-Resolution 12-Sided Voltage Space Vector Structure Using Low-Voltage Stacked and Cascaded Basic Inverter ells," IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 7349 7358, 2018.
- [4] W. Li, J. Hu, S. Hu, H. Yang, H. Yang, and X. He, "Capacitor Voltage Balance Control of Five-Level Modular Composited Converter with Hybrid Space Vector Modulation," IEEE Transactions on Power Electronics, vol. 33, no. 7, pp. 5629 - 5640, 2018.
- [5] D. Cui and Q. Ge, "A Novel Hybrid Voltage Balance Method for Five-Level Diode-Clamped Converters," IEEE Transactions on Industrial Electronics, vol. 65, no. 8, pp. 6020 - 6031, 2018.
- [6] W. Sheng and Q. Ge, "A Novel Seven-Level ANPC Converter Topology and Its Commutating Strategies," IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 7496 - 7509, 2018.
- [7] H. Tian, Y. Li, and Y. W. Li, "A Novel Seven-Level Hybrid Clamped (HC) Topology for Medium-Voltage Motor Drives," IEEE Transactions on Power Electronics, vol. 33, no. 7, pp. 5543 - 5547, 2018.
- [8] N. D. Dao and D.-C. Lee, "Operation and Control Scheme of a Five-Level Hybrid Inverter for Medium-Voltage Motor Drives," IEEE Transactions on Power Electronics, vol. 33, no. 12, pp. 10178 - 10187, 2018.
- [9] M. Abarzadeh and K. Al-Haddad, "An Improved Active Neutral-Point-Clamped Converter with New Modulation Method for Ground Power Unit Application," IEEE Transactions on Industrial Electronics, vol. 66, no. 1, pp. 203 - 214, 2019.
- [10] H. Wang, L. Kou, Y.-F. Liu, and P. C. Sen, "A Seven-Switch Five-Level Active-Neutral-Point-Clamped Converter and Its Optimal Modulation Strategy," IEEE Transactions on Power Electronics, vol. 32, no. 7, pp. 5146 - 5161, 2017.
- [11] Y. P. Siwakoti, "A New Six-Switch Five-Level Boost-Active Neutral Point Clamped (5L-Boost-ANPC) Inverter," in IEEE Applied Power

- Electronics Conference and Exposition (APEC), 2018, pp. 2424 2430.
- [12] P. Siwakoti and F. Blaabjerg, "Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems," IEEE Transactions on Industrial Electronics vol. 65, no. 3, pp. 2100 -2111, 2018.,