# Power-Efficient FPGA Based CLAHE Image Processing with I3C for Medical Applications

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***Abstract* — Image processing is vital in modern embedded system, Applications such surveillance, medical imaging, industrial inspection and autonomous navigation requires image enhancement technique which improves visibility, feature detection and accuracy. This project presents a high-speed pipelined Field programmable gate array (FPGA) architecture for the Contrast Limited Adaptive Histogram Equalization (CLAHE) algorithm which is interfaced with I3C protocol using Block RAM (BRAM) and Verilog HDL for FPGA platforms. Where the system reads image data stored in BRAM, and CLAHE based image processing is performed and enhanced image is stored in output BRAM, an I3C protocol is interface is integrated for allowing external devices or controllers to access the enhanced image data efficiently. Experimental results shows that the image CLAHE algorithm utilizes less power area on selecting ZYNQ (ZCU104) FPGA board on Vivado.**

***Keywords- BRAM*, CLAHE, I3C, FPGA, MATLAB.**

## I. INTRODUCTION

In recent years, the demand for high-performance image processing in embedded system has grown significantly, particularly in medical imaging, automotive surveillance, and industrial automation. CLAHE is a widely used technique that improves the local contrast of images by applying histogram regions(tiles), making it suitable for enhancing low contrast image like medical X-rays or satellite imagery. In this project Histogram is calculated using one memory, mux and counter and all the blocks of histogram process are defined so that parallel process takes place. To transfer enhanced image data between modules or external processors, the project used the I3C (Improved Inter-Integrated Circuit) protocol, which is a next-generation interface combining the simplicity of I2C with speed and flexibility of SPI.

## II. BACKGROUND

A. Wanto, Y. Yuhandri and O. Okfalisa, in the "Optimization Accuracy of CNN Model by Utilizing CLAHE Parameters in Image Classification Problems," paper investigates the use of contrast Limited Adaptive Histogram Equalization (CLAHE) as an image pre-processing technique to enhance the performance of popular Convolution Neural Network (CNN) models for retinal fundus image classification. The study evaluates models such as ResNet50, Inception V4, VGG19, MobileNetV1/V2/V3 (Small & Large) on a publicly available retinal image datasheet. The research highlights CLAHE potential in medical imaging tasks where low contrast hinders feature visibility. The work provides a foundation for extending CLAHE-assisted CNN optimization to other medical image modalities.[2] The paper details an FPGA-based hardware implementation of I²C and UART controllers for interfacing an ambient light sensor (BH1750FVI) and transmitting data to Simulink. Communication is established via an I²C-to-UART bridge implemented using VHDL and FSM architecture. The I²C controller is functionally verified with a hardware analyzer, ensuring reliable sensor data acquisition. Collected data is then sent over UART to MATLAB-Simulink for real-time monitoring and processing. The paper introduces a flexible hardware architecture for the Improved Inter-Integrated Circuit (I3C) protocol to address compatibility and adaptability issues in existing devices. The design incorporates configurable and reusable components, allowing software to dynamically adjust I3C behavior via hardware registers. This adaptability supports diverse peripheral requirements and enhances interoperability. Functional verification confirms correct operation, achieving 99.02% code coverage and 100% functional coverage. The study investigates the use of CLAHE and CNN for detecting COVID-19 from chest X-ray images, using 100 COVID-positive and 100 normal samples. CLAHE was applied as a preprocessing step to enhance image contrast before classification. Two scenarios were tested, comparing a basic CNN model with VGG16 transfer learning. Results indicate that CLAHE improves detection accuracy, with the basic CNN outperforming VGG16 in this dataset. Agalya P, M.C. HanumanthRaju, in 'An High Speed FPGA Implementation of Image Contrast enhancement using Histogram Equalization', paper proposed an architecture of Histogram equalization and synthesized and implemented on Kintex 7 family of FPGA device. Results obtained from MATLAB are found similar with Hardware implementation. To design the architecture, they have used HDL code and Vivado tool. Histogram equilization is used as technique enhance contrast of the image. Koki Honda, Kalije Wei, Masatoshi Arai,Hideharu Amano, in the 'CLAHE implementation on a low-end FPGA board by high-level synthesis' utilizes an external processor side DRAM for storing processed image. The technique used for processing an image is CLAHE algorithm the overall design performed well in device performance and power consumption compromising with resource utilization.

## III. PROPOSED SYSTEM

The proposed system implements the Contrast Limited Adaptive Histogram Equalization (CLAHE) algorithm on an FPGA platform and transfers the processed image data using the I3C communication protocol. The primary objective is to achieve high-speed, low-latency image enhancement suitable for real-time applications such as medical imaging, automotive vision, and surveillance systems.

The main objectives of the design are:

1. Efficient BRAM-based histogram computation.
2. Pipelined architecture for throughput improvement.
3. I3C-based high-speed output data transfer.

In Figure 1 the proposed architecture presents input Block RAM to store the 256*256 grayscale image data in binary format,Histogram calculation block will count number of repeated pixel intensity ,Histogram Processing block will process the image in four stages to calculate CDF,cumilative distributive function (CDF) block,output block RAM will store processed binary image data and I3C protocol acts as external interface.

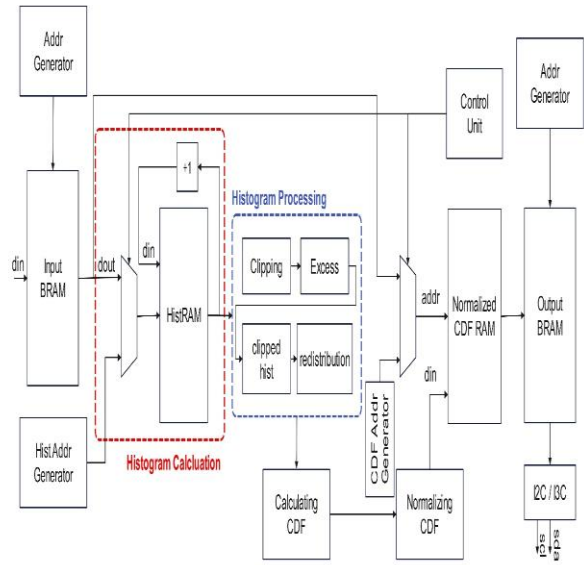


Fig. 1. Proposed architecture

## IV. METHODOLOGY

The design shown in figure 1 comprises several interconnected modules, each serving a specific role in ensuring efficient image enhancement and high-speed data transfer. The following sections elaborate on each functional block, their design rationale, and their interaction with other components.

### *A. Input Block RAM*

The input BRAM block is responsible for receiving the raw image data that needs to be processed by the CLAHE algorithm. Image in jpg format is converted to 8-bit binary format using MATLAB.

### B. *Histogram Calculation Unit*

The Histogram Calculation block computes the pixel intensity distribution for each tile. The design uses, 256 counters (one for each intensity level in an 8-bit image), Parallel counter updates when repeated pixel intensities are encountered to achieve real-time operation, the histogram calculation is pipelined so that each pixel's histogram update is completed within one clock cycle.

$$h[i] = \sum_{n=1}^{n} \{x_n = i\}, \quad i \in [0,255]$$

C. *Histogram Processing*

In CLAHE, a clipping limit is applied to the histogram to prevent over-amplification of noise in relatively homogeneous regions. If a bin exceeds the limit, excess pixels are redistributed evenly across all bins.

$$h_c[i] = \min(h[i], L_{clip})$$

Excess,

$$excess = \sum_{i=0}^{255}(h[i] - h_c[i])$$

Uniform distribution,

$$a = \left[\frac{excess}{256}\right]$$

$$h_r[i] = h_c[i] + a + a\begin{cases}1, & i<r\\ 0, & else\end{cases}$$

D. *Cumulative Distribution Function (CDF)*

Once the clipped histogram is available, the CDF Calculation module computes the cumulative sum of histogram values.

$$cdf[i] = \sum_{k=0}^{i} h_r[k],$$

$$cdf[i] = \sum_{k=0}^{i} h_r[k],$$

Normalization is done by scaling the CDF so that the output intensity range is 0–255,

$$map(i) = \left[\frac{cdf[i] - cdf_{min}}{N - cdf_{min}} .255\right]$$

Where $i \in [0, 255]$

E. *Output Block RAM*

The **output BRAM** block is responsible for receiving the enhanced image data which is processed by the CLAHE algorithm. Image 8-bit binary format is reconstructed to jpg format using MATLAB also the same binary image can also be accessed externally via I3C interface.

F. *I3C Communication Module*

The I3C Interface block is crucial for high-speed, low-pin-count communication between the FPGA and the external processor or display system.it implements single data rate (SDR) or HDR-DDR mode depending on application, handles addressing, framing, protocol timing, achieves higher bandwidth than I2C while retaining backward compatibility. In figure 1 this protocol is responsible for sending data to external devices.

## V. RESULTS

After writing a proper HDL Code the designed is synthesized to convert HDL to RTL level.

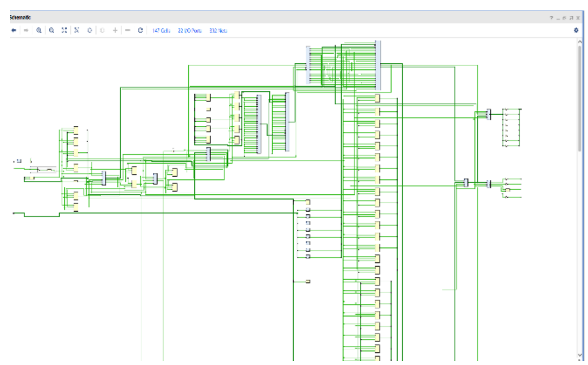

Figure 2: Synthesized Design

*A. Timing Report*

Figure 3 shows timing report of an architecture after implementing on Xilinx Vivado with worst negative slack being positive which shows there is no failing points.

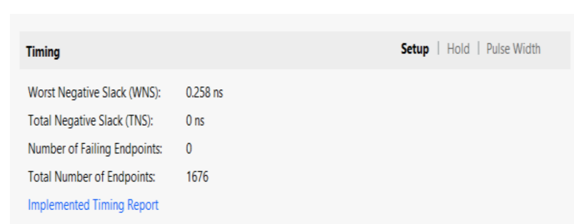


Figure 3: Timing Report

*B.Power Consumption*

The on chip power consumed is 0.602, use of On chip memory available on FPGA fascilitated less power consumption.

| | |
|---|---|
| **Total On-Chip Power:** | **0.601 W** |
| **Junction Temperature:** | **25.6 °C** |
| Thermal Margin: | 74.4 °C (74.6 W) |
| Effective ϑJA: | 1.0 °C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |
| Implemented Power Report | |

Figure 4: Power consumption Report

*C. Resource Utilization*

Figure 5 Shows overall resource utilized on selecting ZYNQ-ZCU104 FPGA Platform.

Graph | Table

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 957 | 230400 | 0.42 |
| LUTRAM | 80 | 101760 | 0.08 |
| FF | 213 | 460800 | 0.05 |
| BRAM | 32 | 312 | 10.26 |
| DSP | 2 | 1728 | 0.12 |
| IO | 22 | 360 | 6.11 |

**Figure 5:** Resource consumption report

*D. Waveform*

Input image is initialied in the form of text format pix_out is a enhanced image, the same data is seen near I3C protocol as data_byte which is used to send data to external device.

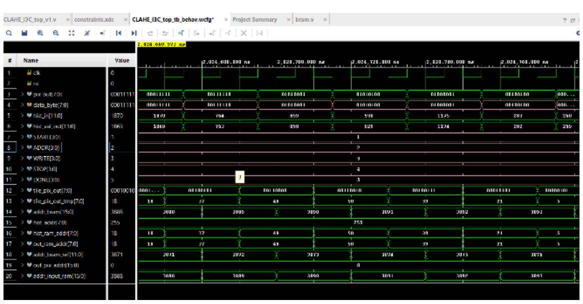

Figure 6: waveform

*E. Comparison of input and enhanced image*

Lung X-Ray image is shown in figure 7 for both input image and enhanced image.

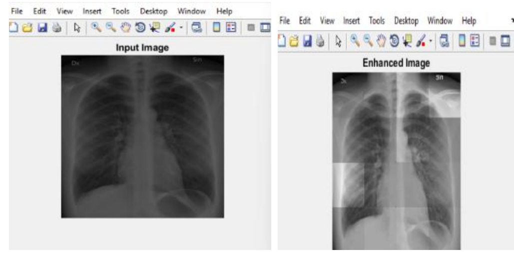


Figure 7: Lung X-Ray Image

Figure 8 show enhanced image for the Brain X-Ray image which is taken as input.

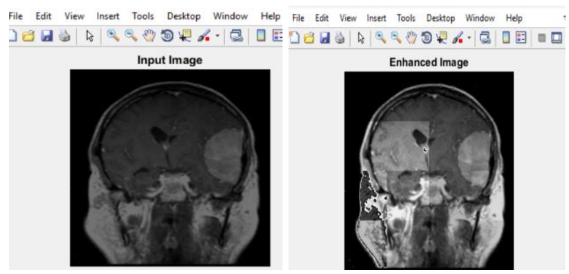


**Figure 8:** Brain X-Ray Image

## III. CONCLUSION

This project successfully designed FPGA architecture for CLAHE algorithm combined with I3C Protocol. The design improves local contrast in low-quality images. Image data is stored and processed in BRAM for low-latency, parallel execution. An I3C slave interface enables high-speed, low-power data transfer to external systems. The solution is efficient, reconfigurable, and well-suited for embedded applications.

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