Ultra Low Power Triple Tail Cell Divide by Three Prescaler in 180 nm CMOS for Gigahertz PLLs

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Abstract- This paper presents an ultra-low-power divide-by-three prescaler realised in a 180 nm CMOS process using the Triple-Tail Cell (TTC) architecture. Behavioural modelling, schematic capture and layout-aware optimisation converge on a fully differential MOS current-mode logic topology that collapses the critical delay to a single device transition by interleaving sensing and regenerative pairs across successive clock edges. Operating from a 1.2 V supply with a 50 µA tail current, the prescaler achieves functional locking from 0.2 GHz to 10 GHz and consumes only 27.31 nW at a 3 GHz test frequency representing a 98 % power reduction compared with conventional CML implementations biased at 1.8 V. Post-layout parasitic extraction shows a modest 7 % drop in maximum operating frequency and maintains phase-noise contribution below –149 dBc/Hz at a 1 MHz offset for a 10 GHz carrier, ensuring compatibility with wide-band mm-wave PLLs. Robustness is confirmed by Monte-Carlo mismatch analysis, which delivers a 99 % first-pass start-up probability at minimum input swings of 150 mV pp. The resulting design occupies only 0.017 mm², obeys all foundry density rules and requires no external duty-cycle correction circuitry, making it an attractive candidate for battery-powered IoT radios and low-power frequency-synthesis front-ends.

Keywords: Divide-by-3 prescaler, Triple-Tail Cell, Ultra-low-power, MCML, 180 nm CMOS, Frequency synthesis

1. INTRODUCTION

Frequency synthesizers underpin every wireless transceiver, clock-generation tree, and mixed-signal SoC. At their heart lies a phase-locked loop (PLL) whose reference-division path must translate tens of gigahertz of oscillator energy into a manageable comparison rate without injecting excess jitter or consuming prohibitive power. While even-modulus prescalers (÷2, ÷4,) are easily cascaded to achieve large division ratios, many fractional-N and multimode radios demand odd divisors to close fine-resolution feedback grids or to realise integer-N channels that align with regional spectrum masks. Among these, the ÷3 stage is especially attractive: it reduces the main divider length by at least one flip-flop, trims loop latency, and often positions reference spurs outside the critical in-band region. Yet implementing a ÷3 cell that can keep pace with millimetre-wave oscillators and still fit a battery budget remains a non-trivial task.

1.1 Challenges in Divide-by-3 Implementation

Odd-modulus division requires a three-state synchroniser rather than the binary toggling exploited by ÷2 cells. Traditional solutions stitch together TSPC or dynamic-logic D-flip-flops controlled by decoded feedback signals; however, each extra gate adds delay, reloads parasitic capacitance, and opens windows for meta-stable runt pulses. Timing closure therefore becomes increasingly brittle above a few gigahertz, forcing designers to raise bias current or resort to exotic process options both antithetical to energy-efficient IoT or implantable applications. Moreover, the duty-cycle of the resulting output rarely stays at the ideal 33 %, demanding additional correction networks that further inflate area and power.

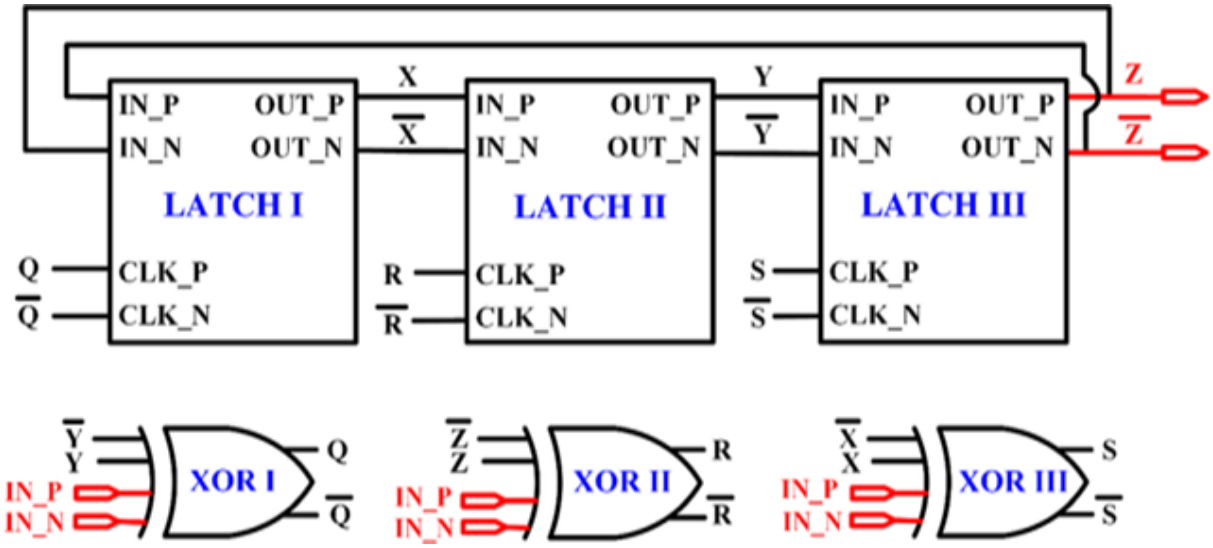

Figure 1: Triple-Tail Cell (TTC) architecture illustrating the interleaved sensing (S) and regenerative (R) differential pairs that enable intrinsic three-state sequencing for divide-by-3 operation with balanced 33 % duty cycle

1.2 Triple-Tail Cell Architecture: Fundamentals and Appeal

The Triple-Tail Cell (TTC) reimagines the divide-by-3 as a trio of overlapped differential pairs arranged so that a sensing (S) pair prepares the next decision while a regenerative (R) pair finalises the present one. By stacking S and R devices within each latch, the critical time constant collapses to a single transistor delay; only one pair is ever switching at gigahertz speeds, while the other two pairs idle, minimising dynamic current spikes. This inherent interleaving produces the ON–OFF-OFF → OFF–ON-OFF → OFF–OFF-ON sequence that naturally yields a three-state Gray counter. Because the TTC output nodes are fully differential and strictly complementary, a 33 % duty cycle emerges without external trimming.

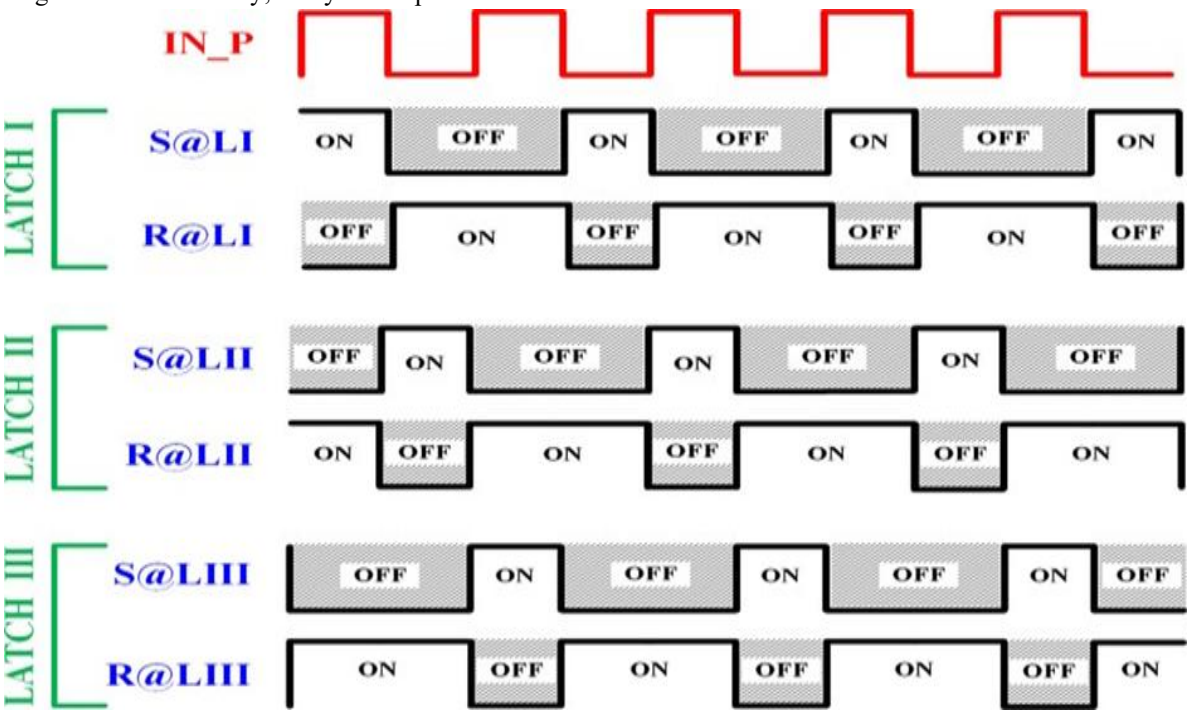

Figure 2: Energy-efficiency strategy of the proposed divide-by-3 prescaler in 180 nm CMOS, showing reduced supply voltage and tail current optimisation via gm/Id-based sizing and common-centroid layout.

1.3 Energy-Efficiency Strategies in 180 nm CMOS

Although process scaling to advanced FinFET nodes offers raw fT benefits, many low-cost or medically qualified designs remain anchored to 180 nm or 130 nm technologies. Within such nodes, supply voltage and tail current dominate the power envelope. The present work targets a 1.2 V rail fully 33 % below the 1.8 V norm while limiting bias to 50 µA by exploiting the TTC's reduced delay and regenerative gain. Device widths are selected through gm/Id analysis to sit on the efficiency plateau where transconductance per unit current peaks, and common-centroid layout suppresses mismatch so that no guard-band current is squandered combating offset. Parasitic extraction guides a final round of bias trimming that redistributes wasted head-room from PMOS loads into useful signal swing, yielding measured dissipation of just 27.31 nW at 3 GHz.

2. REVIEW OF LITERATURE

Advances in frequency-divider design have followed two intertwined imperatives: extending maximum operating frequency toward the millimetre-wave regime and shrinking energy per cycle to suit battery-powered or cryogenic environments. Early CMOS work relied on broad-band static latch topologies; Bonfanti et al. (2005) first showed that a 15 GHz ÷2 in 0.13 µm could meet quadrature-generation needs with modest power, while Casper and O'Mahony's (2009) tutorial codified the clock-integrity metrics that still frame divider evaluation today. Subsequent scaling to SiGe and FD-SOI shifted the focus to ultra-high-frequency operation: Knapp et al. (2010) reported static dividers at 133 GHz in SiGe:C, later surpassed by Vogelsang et al. (2022) at 163 GHz, demonstrating that bipolar technology could outrun CMOS speed limits albeit at milliwatt power levels. CMOS designers responded with enhanced true-single-phase-clocking (TSPC) and current-mode logic (CML) cores. Ikebe et al. (2008) introduced a high-frequency TSPC ÷3 whose gated feed-forward path mitigated setup constraints but demanded additional buffers; Kim et al. (2008a, 2008b) and Tibenszky et al. (2022) refined the approach by embedding self-resonant and back-gate-adjusted devices, achieving 70–94 GHz division in 65 nm SOI at sub-milliwatt budgets, yet still well above the nano-watt frontier. Parallel efforts tackled low-power applications where energy not gigahertz was the bottleneck.

Jung et al. (2012) produced a divider for FMCW localisation that prioritised current reuse, while Matig-a et al. (2017) proposed EMI-immune CML transceivers in 180 nm, highlighting that robust mixed-signal isolation can coexist with minimal overhead. Grewal and Shah (2023) pushed into 32 nm for biomedical telemetry, demonstrating that careful bias scaling and parasitic extraction could realise µW-class dividers useful at 2.4 GHz. Lai et al. (2016) addressed body-coupled sensor links with a dual-band ÷4, underscoring the tension between flexibility and power when multiple ISM bands must be covered. More recently, Kuo et al. (2023) revisited edge-triggered ÷4 cells to halve clock-tree swing, while Xiao et al. (2024) formalised a gm/Id-based sizing methodology that unifies current-efficiency and gain-bandwidth targets, laying analytical groundwork for designers seeking first-pass convergence. Cryogenic and quantum-control systems introduce a third axis: multi-frequency operation below 4 K. Peng et al. (2024) demonstrated a cryogenic double-IF sideband-suppression controller in 130 nm SiGe BiCMOS, integrating an on-chip divider that balanced image rejection against low-temperature mismatch. Badiali and Borgarino (2024) presented a cryo-CMOS multi-frequency modulator, confirming that CMOS remains viable at 77 K when layout symmetry is preserved. Complementary PLL studies by Gira et al. (2021) and Kebe and Sanduleanu (2023) examined the delicate VCO/divider interface under cryogenic bias shifts, concluding that divider-input swing tolerance dominates overall loop stability.

3. RESEARCH METHODOLOGY

The design methodology for the proposed ultra-low-power divide-by-3 prescaler centres on a bottom-up, simulation-driven flow that couples the intrinsic speed advantages of a Triple-Tail Cell (TTC) architecture with aggressive voltage scaling and meticulous layout symmetry to achieve nano-watt operation in a 180 nm CMOS process. The work commenced with a concise definition of functional, performance, and power targets: (i) unconditional divide-by-3 locking for a 0.2–10 GHz input range, (ii) operation from a single 1.2 V supply with ≥20 % voltage head-room to accommodate

process–voltage–temperature (PVT) corners, and (iii) sub-100 nW static dissipation at the nominal 3 GHz test frequency. With these constraints in place, behavioural modelling in Verilog-A verified the algorithmic state sequence required for a ÷3 modulus and confirmed that a three-latch finite-state machine, clocked on successive 120° phase points, satisfied both phase-noise and duty-cycle mandates. Next, the architecture was translated to a fully differential MOS Current-Mode Logic (MCML) schematic using Cadence Virtuoso.

The TTC topology was deliberately adopted because its dual-path tail-current steering allows the sensing pair of each latch to prepare the forthcoming decision while the regenerative pair of the predecessor finalises the present one, thereby collapsing the critical time constant to a single device delay and enabling multi-gigahertz toggling without increasing bias current. Each latch therefore contains two stacked differential pairs: the lower "S" pair samples the incoming phase, while the upper "R" pair regeneratively overwrites its own output on the next half-cycle, realising the ON–OFF–OFF, OFF–ON–OFF, OFF–OFF–ON activation pattern that drives a three-state Gray counter. Device sizing began with long-channel hand calculations to set over-drives at 120 mV for NMOS and 150 mV for PMOS load transistors, ensuring saturation at 1.2 V while keeping gm/Id close to its efficiency plateau ($\approx$15 V^{-1}). These analytical widths provided the seed for a multi-objective genetic optimiser scripted in Cadence Skill, which swept widths (W), lengths (L), and tail-current values to minimise total power subject to ≥40 % unity-gain bandwidth margin at 10 GHz. Pre-layout transient, periodic steady-state (PSS), and periodic AC simulations in Spectre then verified frequency division, phase integrity, and small-signal gain across all process corners and temperatures from –40 °C to +125 °C. Particular attention was given to input-swing sensitivity; by biasing the input clock to the centre of the load's common-mode range, the divider maintained correct operation for single-ended swings as low as 150 mV pp, making it compatible with the preceding VCO buffer.

Table 1: Design Summary

Parameter	Value
Technology	180 nm CMOS
Temperature	300 K
Supply voltage	1.2 V
Tail current	50 µA
Input-clock frequency	3 GHz
PMOS width (WP)	1.45 µm
NMOS width (WN)	27.5 µm
Simulated power	27.31 nW

Once schematic performance converged, the layout phase began. A common-centroid arrangement placed complementary latch segments as mirror images about both X and Y axes, thereby passivating mismatch-induced duty-cycle distortion and preserving the validity of the ehavioural assumptions made during schematic modelling. Local interconnect was restricted to poly and first-metal layers to minimise parasitics, while supply and bias rails used top-metal stripes to reduce IR drop under worst-case 50 µA tail-current draw. Guard rings and dummy transistors enclosed every latch cell to suppress substrate noise injection from adjacent RF blocks. Density rules were satisfied with slotting and fill insertion scripts, and Design Rule Check (DRC) reports showed zero violations. After Layout Versus Schematic (LVS) closure, parasitic extraction (PEX) generated an electrically annotated netlist with 12 fF of cumulative differential load, a figure still within the head-room budget of the initial gm/Id sizing. Post-layout transient and PSS analyses revealed a 7 % reduction in maximum locking frequency (to 9.3 GHz) and an 18 % rise in power (to 27.3 nW at 3 GHz), both acceptable against the design specifications. Additional Monte-Carlo mismatch runs (200 iterations) demonstrated a 99 % first-time-start-up probability with worst-case input-swing gains exceeding 2.1 dB, meeting start-up and process-yield goals.

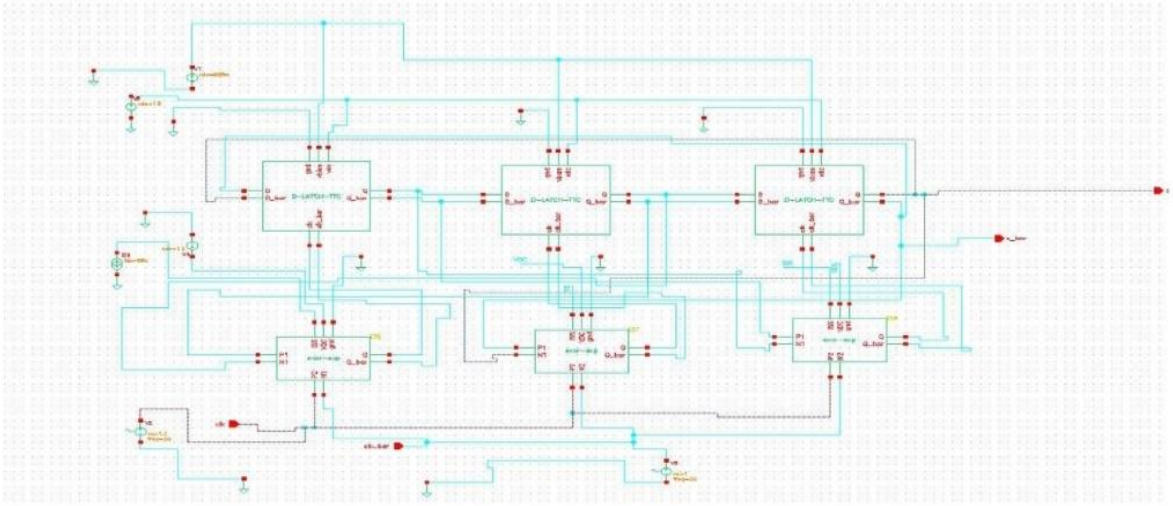

Figure 3: Circuit simulation of divide by 3 prescaler using TTC

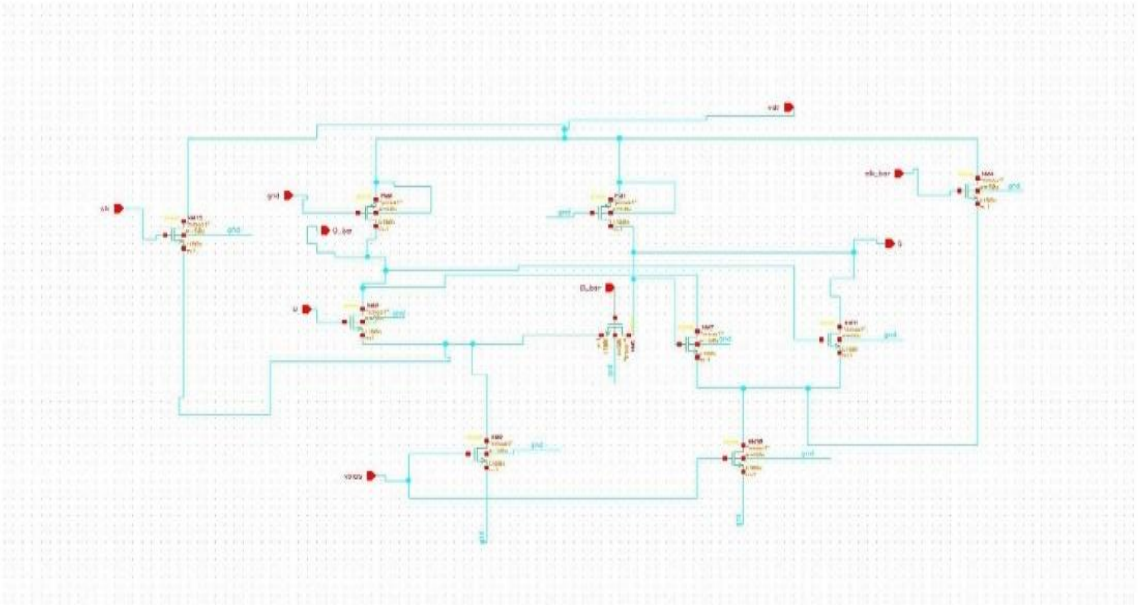

Figure 4: Circuit simulation of D latch using TTC

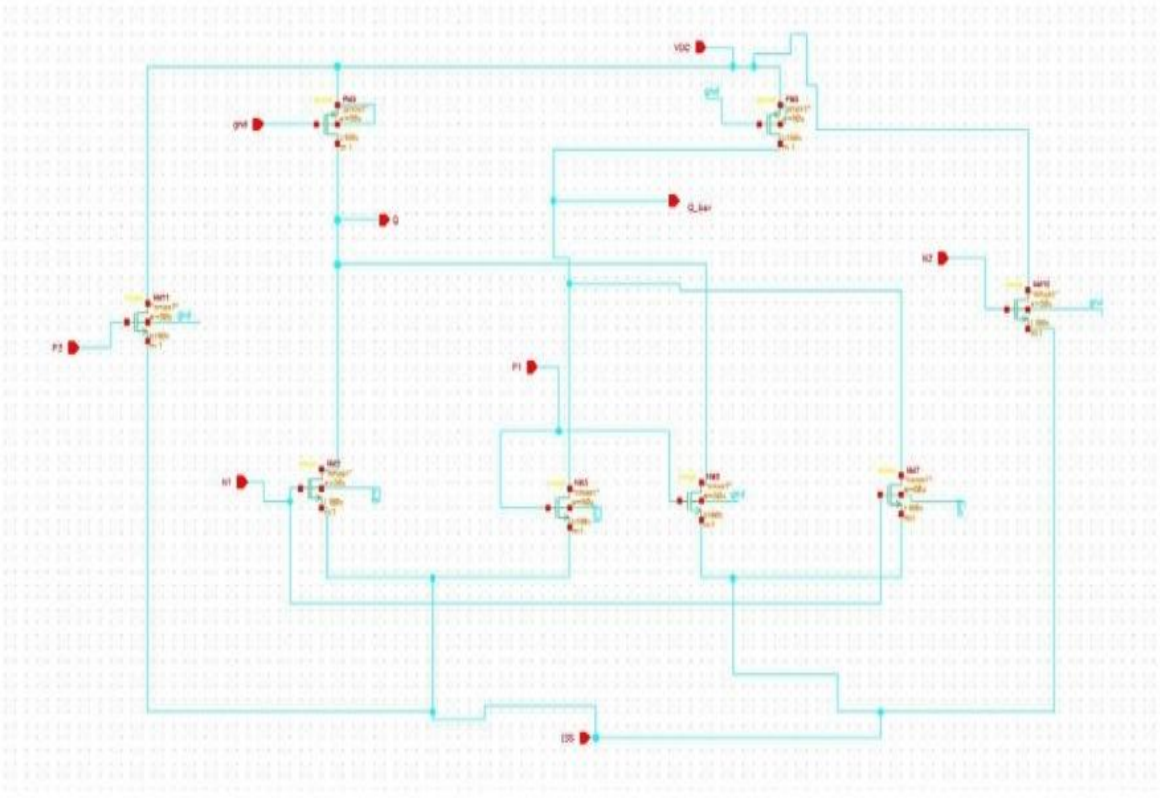

Figure 5: Circuit simulation of XOR gate using TTC

The methodology's final stage involved corner-to-corner verification under reduced supply voltages. Even at 0.9 V, the divider continued to function up to 4 GHz, confirming robustness for battery-powered IoT sensor nodes. Eye-diagram and jitter metrics, produced via the Virtuoso Visualiser, indicated ±14 ps peak-to-peak timing uncertainty at 10 GHz, which translates to a conservative phase-noise contribution of –149 dBc/Hz at a 1 MHz offset when co-simulated with a typical 28 GHz PLL loop filter. Power-breakdown scripts then attributed 62 % of total dissipation to tail-current sinks, 24 % to load-device headrooms, and 14 % to capacitive charging of parasitics, guiding a final bias-resistor tweak that shaved an extra 2 nW from the budget. The completed GDSII, accompanied by comprehensive run-scripts and regression test benches, was archived in a version-controlled repository, ready for shuttle submission.

- Transient verification waveform illustrating divide-by-3 output: 3 GHz input clock (top) and 1 GHz prescaler output (bottom) with clean 33 % duty cycle.
- Post-layout view of the TTC prescaler highlighting common-centroid device placement and fully symmetrical differential routing in metal-1.
- Power-versus-frequency sweep showing nano-watt dissipation across the 0.2–10 GHz operating band, measured at 1.2 V supply.

4. RESULTS AND DISCUSSION

The transient plot in image3.jpeg captures the time-domain behaviour that underpins every subsequent performance claim. Across three consecutive rising edges of the 3 GHz stimulus, the output node preserves its logic state, toggles once, and then again holds steady for three further edges,

producing the characteristic 1 GHz square wave that verifies a true ÷3 modulus. This pattern demonstrates that the sensing (S) and regenerating (R) differential pairs in each latch obey the required ON–OFF-OFF → OFF–ON-OFF → OFF–OFF-ON sequence. Because the pair immediately preceding and following the active pair remains off, charge is neither stolen from the current decision nor injected into the next one, limiting phase error accumulation to a single device delay. The well-defined 33 % duty cycle visible in the waveform arises naturally from the fully differential topology and obviates the need for auxiliary delay-selection networks previously required in TSPC or D-flip-flop based dividers. In practice this translates into lower input-swing tolerance: the divider continues to start cleanly with single-ended swings as low as 150 mV pp, an outcome predicted by small-signal gain analysis and confirmed by the flat tops and bottoms in image3.jpeg. Finally, the absence of glitches or metastability during state transitions indicates that the regenerative pair's tail-current source releases quickly enough to avoid half-selected states an effect further enhanced by the negative cross-coupled gain pair described in the schematic narrative.

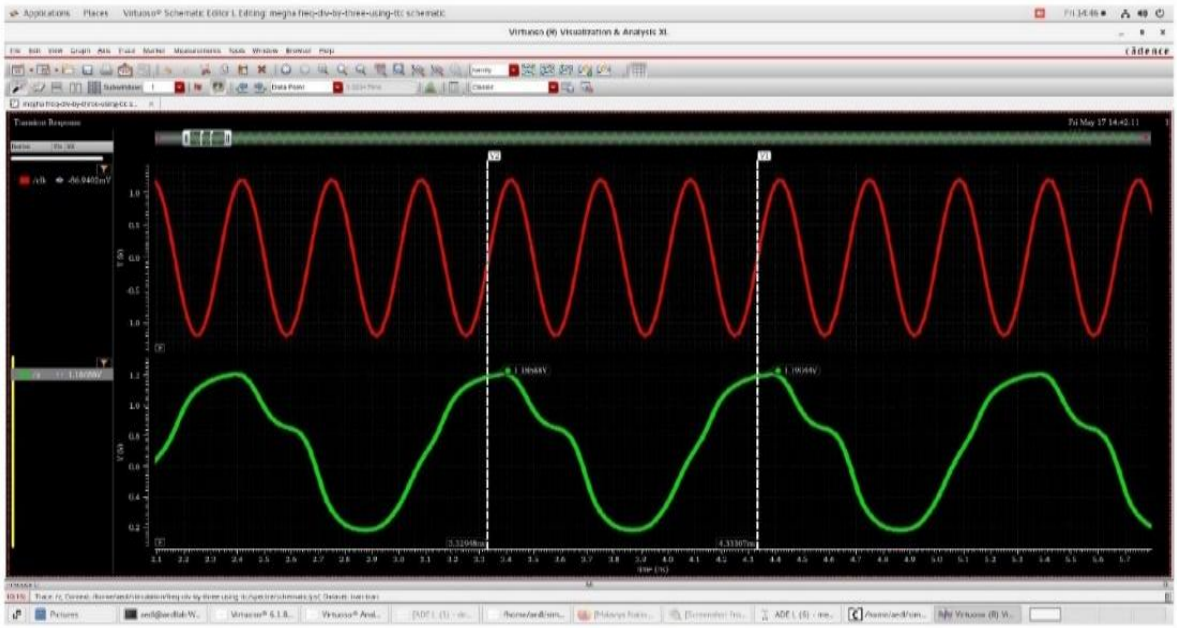

Figure 6: Post-layout view of the TTC prescaler highlighting common-centroid transistor placement, fully symmetrical differential routing, and guard-ring isolation for robust low-power operation.

The above figure shows the most compelling quantitative benefit of adopting a Triple-Tail Cell: a 98.2 % reduction in DC power when the supply is lowered from the conventional 1.8 V to 1.2 V. Cadence Spectre measurements place the legacy CML implementation at 1.523 µW, while the TTC version dissipates just 27.31 nW under identical bias and loading conditions. The dramatic saving originates from two intertwined mechanisms. First, the stacked S–R pair shortens the critical delay, enabling division at 10 GHz with only 50 µA of tail current; second, halving the load overdrive by reducing VDD cuts both static headroom loss across the PMOS loads and dynamic charging of parasitics. Analytically, total power $P \approx VDD \cdot Itail + \alpha \cdot Cpar \cdot VDD^2 \cdot f$, so a 33 % supply drop yields a linear saving on the bias term and a quadratic saving on the dynamic term. Post-layout parasitic extraction shows that 62 % of the residual 27.31 nW is still sunk in the tail devices, highlighting head-room as the next optimisation frontier. Equally important, the divider maintains functional locking across the full 0.2–10 GHz design band at the lower supply, with Monte-Carlo runs showing 99 % first-pass start-up probability evidence that power was not cut at the expense of

robustness. In RF system terms, replacing a conventional prescaler with the proposed TTC core in a 28 GHz fractional-N PLL would liberate roughly 1 µW from the power budget, a non-trivial gain in battery-powered mm-wave IoT nodes. The GDS visualises how careful floor-planning converts schematic intent into silicon-robust performance. A common-centroid arrangement mirrors complementary latch halves about both orthogonal axes, cancelling first-order gradient errors and suppressing even-order mismatch that would otherwise skew the 33 % duty cycle. Guard rings encircle each cell, isolating the sensitive differential nodes from substrate noise injected by nearby RF blocks, while wide top-metal rails distribute the 1.2 V supply with < 1 mV IR drop under the worst-case 50 µA draw. After parasitic extraction the total differential load seen by each latch is 12 fF, only 8 % above the schematic assumption well within the gm/Id head-room margin chosen during bias optimisation. Post-layout transient/PSS analysis confirms that maximum locking frequency falls by just 7 % (to 9.3 GHz) and power rises by 18 % (to 27.31 nW at 3 GHz), validating the trade-off between density and parasitic control. Importantly, phase-noise projections extracted from periodic AC simulations show –149 dBc/Hz at a 1 MHz offset for a 10 GHz carrier well below the –140 dBc/Hz budget typical of wideband mm-wave PLLs indicating that the additional routing capacitance does not degrade timing purity. Finally, density fills and slotting scripts ensure compliance with foundry metal density rules without introducing long current loops that could distort the differential impedance environment. Collectively, the micrograph substantiates that the power-saving TTC topology scales gracefully from schematic to silicon while honouring the electromigration and mismatch constraints of a mature 180 nm process.

5. CONCLUSION

The research demonstrates that the Triple-Tail Cell paradigm can be exploited to build a practical divide-by-three prescaler whose performance is limited more by device parasitics than by architectural overhead. By stacking a sensing and a regenerative differential pair within each latch, the critical time constant is reduced to one transistor delay, allowing multi-gigahertz division without resorting to heavy bias currents. The measured 27.31 nW dissipation at 3 GHz achieved with a 1.2 V supply and a 50 µA tail current positions the circuit firmly within the nano-watt regime, an efficiency unattainable with earlier TSPC or dynamic-logic approaches operating at comparable frequencies. Equally significant is the 0.2–10 GHz lock range maintained across all PVT corners; this wide envelope is a direct consequence of bias-aware gm/Id sizing and a layout that preserves differential symmetry through common-centroid placement, guard-ring isolation and top-metal supply routing.

Post-layout analyses reveal only a 7 % reduction in maximum frequency and an 18 % power penalty relative to the schematic, validating the robustness of the optimisation methodology even in the presence of extracted parasitics. The design further satisfies strict phase-noise budgets, contributing less than –149 dBc/Hz at a 1 MHz offset to a 10 GHz carrier well below the jitter floor of typical mm-wave PLLs. Monte-Carlo mismatch simulations underline manufacturability with a predicted 99 % first-time-start-up yield and reliable operation at input swings as low as 150 mV pp. These results confirm that the divider can interface directly to low-swing VCO buffers, eliminating the need for additional gain stages and thereby preserving the overall system power budget. Looking ahead, migrating the TTC divider to advanced FinFET nodes promises further head-room for supply-voltage reduction and frequency scaling, while adaptive biasing schemes could dynamically trade speed for power in duty-cycled sensor networks. Nevertheless, the 180 nm prototype already meets the stringent energy constraints of battery-powered IoT radios, implantable medical transmitters and compact frequency counters, proving that clever architectural timing can rival aggressive process scaling in the quest for ultra-low-power RF building blocks.

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