Optimized VLSI Architectures for Signal Processing and Data Compression: A Comparative Analysis

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Abstract— The evolution of Very Large-Scale Integration (VLSI) architectures has significantly improved computational efficiency in signal processing, video compression, and data encoding. This paper reviews three innovative VLSI designs: Feedforward FFT hardware architectures, which enhance efficiency through optimized rotator allocation; HEVC deblocking filter architectures, which improve video compression performance; and high-speed Huffman encoder architectures, which maximize data encoding throughput. A comparative analysis of these architectures highlights their unique advantages, efficiency improvements, and potential future applications. The discussion explores hardware optimization techniques, computational trade-offs, and real-world implementation considerations.

Keywords: Feedforward FFT, HEVC Deblocking Filter, Huffman Encoding, Parallel Processing, Memory Interlacing

I. INTRODUCTION

With the rapid advancements in technology, the demand for high-performance and energy-efficient computing architectures has significantly increased. Various domains, including video processing, data compression, wireless communication, and biomedical signal processing, require specialized hardware solutions to enhance throughput and reduce computational complexity. Recent research has focused on optimizing Very Large Scale Integration (VLSI) architectures for diverse applications, leading to improved efficiency in hardware implementations.

In video compression, the emergence of High Efficiency Video Coding (HEVC) has revolutionized the field by providing superior compression rates compared to its predecessor, H.264/AVC. HEVC employs advanced block-based hybrid coding techniques, including Coding Units (CU), Prediction Units (PU), and Transform Units (TU), to achieve a substantial reduction in bit rates. However, blocking artifacts introduced by compression algorithms necessitate the use of an efficient deblocking filter to enhance visual quality. Hardware implementations of HEVC deblocking filters require optimized architectures to balance processing speed and memory utilization.

In parallel, the efficiency of data compression techniques plays a crucial role in storage and transmission systems.

Huffman encoding, a widely used lossless compression method, is integral to various applications such as image processing and data security. Traditional Huffman encoding approaches suffer from low throughput mainly in multiple data scans during the encoding process. The introduction of high-throughput VLSI architectures, particularly those based on Canonical Huffman encoding, has demonstrated significant improvements in encoding efficiency by reducing the number of operations required for codeword generation.

Similarly, biomedical applications have witnessed notable advancements in data compression and real-time signal processing. Electrocardiogram (ECG) monitoring is critical for diagnosing cardiovascular diseases, and efficient compression techniques without loss are essential for telemedicine applications. Modern ECG compression algorithms integrate adaptive prediction and entropy coding methods, such as Golomb-Rice coding, to achieve highly efficient compression ratios while preserving diagnostic accuracy.

In the domain of wireless power transmission, rectenna are extensively studied for energy harvesting applications. The integration of microstrip antennas with rectifier circuits facilitates the conversion of radiofrequency (RF) signals into usable DC power. Optimized rectenna designs employ genetic algorithms to enhance power conversion efficiency, making them viable for low-

power wireless sensor networks and Internet of Things (IoT) applications.

Moreover, the Fast Fourier Transform (FFT) implementation algorithms on Field Programmable Gate Arrays (FPGAs) has been a subject of extensive research. FFT is a foremost operation in digital signal processing, and efficient hardware architectures are essential to achieve the computational demands of real-time applications. Recent studies have explored feedforward FFT architectures and rotator allocation techniques to minimize hardware complexity while maximizing throughput.

VLSI-based architectures across multiple domains, including video processing, compression of dataset, medical signal processing, and RF energy harvesting. The survey highlights key design challenges, optimization techniques, and comparative performance analyses of various hardware implementations. By examining these developments, the main purpose of study is to provide important insights into the future directions of high-performance VLSI architectures.

II. LITERATURE SURVEY

Many studies have been explored several VLSI architectures to increase throughput and efficiency of medical image processing

[1] The Fast Fourier Transform (FFT) is a fundamental algorithm in digital signal processing, widely utilized for computing the Discrete Fourier Transform (DFT) efficiently. Given the increasing demand for high-performance and real-time processing in modern applications, researchers have explored various hardware architectures to optimize FFT computation. Pipelined architectures are most important approaches because of their ability to achieve high throughput and low latency while maintaining an efficient balance between hardware resources and power consumption. FFT hardware implementations is divided into three types: feedback architectures, feedforward architectures, and serial commutator-based architectures. Feedback-based designs, such as single-path delay feedback (SDF) and multi-path delay feedback (MDF), involve looping certain butterfly outputs back into memory. While these architectures offer efficient memory usage, they introduce additional complexity due to the feedback paths. In contrast, feedforward architectures, particularly those using multi-path delay commutators (MDC), eliminate feedback loops, allowing for streamlined data flow and increased parallelism. Serial commutator architectures, though less common, focus on bit-wise permutations to optimize data handling. The efficiency of FFT implementations largely depends on the number and complexity of rotators used for phase computations. Various radix-based approaches have been proposed to optimize rotator placement and reduce computational overhead. Traditional radix-2 designs, while simple, require a larger number of general rotators, leading to increased hardware complexity. Radix-2k architectures attempt to balance this trade-off by reducing the number of general rotators and distributing computations more efficiently. The concept of rotator allocation, introduced in recent works, focuses on strategically distributing phase rotations across FFT stages to minimize both the number and complexity of required rotators. This method exploits mathematical properties of the FFT to consolidate similar rotations, thereby reducing hardware redundancy. Experimental results demonstrate that architectures employing rotator allocation significantly decrease hardware costs while maintaining or even improving performance compared to conventional designs.

[2High Efficiency Video Code (HEVC) is the latest development in video capacity technology, comparing it to previous standards such as H.264/AVC compression efficiency. The goal is to reduce the bitrate to about 50% and maintain the same visual quality at the same time. The core structure of HEVC follows a block based hybrid coding approach that includes new elements such as coding units (CU), prediction units (PU), and conversion units (TU) to optimize video displays. A key output of log based compression techniques is the occurrence of blocking artifacts that affect visual quality. To mitigate this, deblocking filters (DF) are employed as an in-loop filtering mechanism. Unlike H.264/AVC, which applies adaptive low-pass filters to every 4×4 block boundary, HEVC processes only 8×8 block boundaries to reduce computational complexity. The filtering process follows a structured order, where vertical edges are filtered first, followed by horizontal edges, using data modified by the vertical filtering process.

Several research works have explored hardware implementations of deblocking filters in previous video coding standards. Notably, studies on H.264/AVC have demonstrated various optimization techniques for deblocking filter architectures. These include

parallelized approaches to increase throughput and pipeline-based designs for reducing latency. HEVC's deblocking filter follows a similar concept but introduces a different block partitioning scheme, requiring novel architectural solutions. One major challenge in hardware implementation is balancing high throughput and efficient memory utilization. Conventional designs rely on sequential processing, which limits the ability to meet real-time performance requirements for high-resolution applications. To address this, recent studies propose pipelined architectures that process multiple lines simultaneously. The introduction of interlaced memory organization is another strategy that enhances data access efficiency during both vertical and horizontal filtering operations. In conclusion, prior research has laid the groundwork for optimized deblocking filter implementations in video coding standards. The evolution from H.264/AVC to HEVC presents new architectural demands, requiring innovative techniques to improve efficiency. The proposed solutions, including multi-stage pipelining and optimized memory arrangements, demonstrate significant improvements in processing speed and power efficiency, making them well-suited for modern high-resolution video applications.

[3] Huffman coding is a widely used data compression technique, playing a crucial role in various domains such as image and audio compression, data storage, and communication systems. Traditional Huffman encoding involves generating variable-length codes based on symbol frequency, ensuring efficient data representation. However, conventional approaches require multiple scans of input data, increasing computational complexity and processing time. Canonical Huffman encoding, an optimized variant, simplifies the decoding process by ensuring that shorter codes correspond to smaller numerical values. This method eliminates the need to store complex tree structures, reducing memory usage and improving hardware efficiency. Prior research has explored hardware implementations of Huffman encoders, aiming to enhance speed, reduce power consumption, and optimize area utilization. Several studies have proposed hardware-efficient designs for Huffman encoders, focusing on aspects such as parallel processing, memory-efficient table lookups, and reduced hardware redundancy. Existing solutions often rely on precomputed code tables, which limit adaptability to varying input distributions. Some approaches leverage pipelining techniques to accelerate encoding, but they introduce increased circuit complexity and require additional hardware resources. The proposed VLSI architecture in this study points out these limitations by introducing a high-throughput, parallel computing design for frequency statistical sorting and code-size computation. Unlike traditional methods that require multiple data scans, the suggested approach enables single-pass processing, significantly reducing encoding time. Furthermore, the integrating a real-time frequency sorting mechanism enhances efficiency, make them suitable for real-time applications. Previous implementations of Huffman encoders have struggled with optimizing the trade-off between processing speed and hardware resource utilization. The proposed architecture achieves a balance by employing a structured approach to frequency sorting and symbol assignment, thereby streamlining the computation process. Compared to conventional methods, this design achieves a notable reduction in encoding time while maintaining the high compression efficiency inherent to Huffman coding. n summary, advancements in Huffman encoder designs have focused on improving throughput, reducing memory requirements, and enhancing processing efficiency. The proposed VLSI-based Canonical Huffman encoder represents a significant step forward in addressing the limitations of existing architectures, making it a viable solution for high-performance compression applications.

4] Electrocardiogram (ECG) signals play a important role in diagnosing cardiovascular diseases, which are among the leading causes of mortality worldwide. With the increasing demand for remote health monitoring and telemedicine applications, efficient ECG data compression techniques have gained significant attention. The primary challenge in ECG compression lies in reducing data size while ensuring lossless signal reconstruction for accurate medical diagnosis. Existing ECG compression method can be broadly categorized into three types: direct data compression, transform-based compression, and parameter extraction methods. Direct data compression methods operate in the time domain and include techniques such as delta pulse code modulation (DPCM), amplitude zone time epoch coding (AZTEC), and coordinate reduction time encoding system (CORTES). These methods aim to reduce redundancy by encoding signal differences rather than absolute values. Transform-based methods, on the other hand, convert the signal into a frequency domain representation using methods like

Discrete Cosine Transform (DCT), Fourier Transform (FT), and Wavelet Transform (WT). These techniques leverage the energy redistribution properties of the signal to achieve higher compression ratios. Parameter extraction methods focus on identifying key features from the ECG signal, such as peak detection and neural network-based models, to minimize data storage while preserving essential diagnostic information. Among the various ECG compression techniques, lossless methods are preferred in medical applications as they ensure complete signal reconstruction without any distortion. Traditional lossless compression approaches utilize predictive modeling combined with entropy coding. Linear predictive coding (LPC) and differential pulse code modulation (DPCM) are widely used predictive techniques, while Huffman coding, Arithmetic coding, and Golomb-Rice coding are commonly employed for entropy coding. Golomb-Rice coding, in particularly, has got popularity due to its ability to efficiently compress biomedical signals with a skewed probability distribution. Recent research has focused on developing hardware-efficient ECG compression algorithms suitable for embedded systems. Adaptive linear prediction techniques have been introduced to enhance prediction accuracy and reduce redundancy in ECG signals. Additionally, content-adaptive Golomb-Rice coding has been proposed to optimize compression performance by dynamically adjusting encoding parameters based on signal characteristics. These advancements enable real-time ECG compression on resource-constrained devices, making them suitable for wearable healthcare applications. The proposed study builds upon prior research by integrating adaptive prediction techniques with optimized entropy coding methods. By leveraging efficient data packing formats and hardware-friendly encoding schemes, the proposed approach achieves higher compression ratios while maintaining real-time processing capabilities. Compared to existing ECG compression algorithms, this system demonstrates improved performance, making it a viable solution for telemedicine and remote patient monitoring applications.

[5] With the increasing demand for efficient energy harvesting systems, wireless power transmission (WPT) has emerged as a promising technology, enabling energy transfer without physical connectors. Among various WPT techniques, rectenna-based radiofrequency (RF) energy harvesting has gained significant attention due to its capability to convert ambient RF signals into usable DC power. The rectenna system, composed of a receiving antenna and a rectifying circuit, plays a important role in determining the overall energy conversion efficiency. Several studies have explored different rectenna architectures to improve their performance in terms of efficiency, compactness, and operational bandwidth. The microstrip patch antenna (MPA) is widely used for RF energy harvesting applications due to its lightweight structure, low manufacturing cost, and ease of integration with circuits. Various designs of MPAs, including single-band, dual-band, and multi-band configurations, have been proposed to optimize power reception. Researchers have investigated different substrate materials, impedance-matching techniques, and polarization methods to enhance the antenna's gain and efficiency. To optimize the rectifying circuit, different rectifier topologies have been explored, including single-series, voltage-doubler, and multi-stage rectifiers. The choice of the rectifying diode significantly impacts the power conversion efficiency (PCE), with Schottky diodes such as the SMS7630 being widely preferred for their high sensitivity at low input power levels. Additionally, impedance-matching networks, such as coupled-line impedance transformers, are commonly integrated into rectifier designs to minimize power loss and ensure optimal power transfer between the antenna and rectifier circuit. Genetic algorithms (GAs) have been increasingly used for optimizing rectenna designs by automating parameter selection and improving overall performance.

[6] The Fast Fourier Transform (FFT) is a fundamental algorithm widely used in signal processing applications, and its efficient hardware implementation remains a critical area of research. Field-Programmable Gate Arrays (FPGAs) offer a promising solution due to their parallel processing capabilities and reconfigurability. Prior studies have focused on optimizing FFT architectures to achieve high throughput while minimizing resource utilization. Traditional multi-core processing approaches provide high-speed computations but often suffer from increased power consumption and system cost. o address these challenges, researchers have explored various FPGA-based FFT implementations, including feedforward and multi-path delay commutator (MDC) architectures. These designs prioritize parallelism and efficient memory usage to enhance computational performance. Previous works have also introduced algorithmic

optimizations, such as radix-based decompositions and pipeline-based implementations, to maximize FFT throughput. However, existing methods often struggle to balance scalability and hardware efficiency when handling large FFT sizes. The paper under review introduces an FPGA-based FFT generation tool that enables flexible customization of parameters such as FFT size, parallelization level, and memory allocation. By leveraging a highly parameterized design approach, the proposed system achieves significant improvements in throughput, supporting FFT sizes up to 65,536 points with performance scaling in the range of several to tens of gigasamples per second. The study provides a comparative analysis of different FPGA architectures and highlights the feasibility of implementing high-performance FFT systems without the need for multi-core processors.

III. COMPARATIVE ANALYSIS

Paper Title	Focus	Method	Contribution	Performance
Huffman Encoder	Compression	Parallelism	Speed	High-throughput
HEVC Deblocking	Video	Pipelining	Efficiency	Low latency
ECG Compression	Biomedical	Prediction	Lossless	High ratio
Rectenna Design	Energy	Genetic Algorithm	Optimization	High efficiency
FFT on FPGA	Signal	Parallelization	Performance	High-speed
FFT Rotator	DSP	Rotator Allocation		Low power
HEVC Standard	Video	Advanced Coding	Compression	4K/8K Support

IV. OUTCOMES OF RESEARCH

The reviewed studies contribute significant advancements in their respective domains. The Huffman encoder research improves encoding efficiency through parallel processing, reducing computation time. HEVC deblocking filter architecture enhances video quality while maintaining high throughput for 4K processing. ECG compression techniques achieve lossless data reduction, optimizing bandwidth for telemedicine applications. Rectenna design advancements using genetic algorithms enhance energy harvesting efficiency. FFT implementations on FPGA improve signal processing speed, while optimized rotator allocation reduces hardware complexity. Collectively, these studies provide optimized solutions for data compression, video coding, signal processing, and energy efficiency.

V. RESEARCH GAPS AND FUTURE DIRECTIONS

Despite notable progress, several challenges remain. Huffman encoder designs still require further optimization for real-time applications with variable data distributions. HEVC deblocking filters, though efficient, demand improvements in adaptive filtering for higher resolution formats. ECG compression techniques can benefit from hybrid approaches integrating AI-driven optimization. Rectenna designs need better impedance matching techniques to further improve energy conversion rates. FPGA-based FFT architectures face trade-offs between resource utilization and performance, requiring novel memory management strategies. Overall, more adaptive, scalable, and power-efficient solutions are needed.

Future research should focus on enhancing adaptability, efficiency, and real-time performance. Huffman encoding can integrate AI-based predictive models to optimize symbol assignment dynamically. HEVC processing can benefit from machine learning-driven noise reduction for improved video quality. ECG compression techniques should explore deep learning-based predictive models to enhance signal fidelity. Rectenna systems can be improved with advanced metamaterials to boost energy harvesting efficiency. FPGA-based FFT architectures should investigate neuromorphic computing techniques to optimize parallel processing further. By addressing these areas, future innovations will push the boundaries of computational efficiency, signal processing, and energy optimization.

VI. CONCLUSION

This review explores recent advancements in VLSI architectures for FFT, HEVC, and Huffman encoding, highlighting their influence on performance and energy efficiency. The application of these techniques in real-time domains, such as telemedicine and IoT, demonstrates their significance in next-generation embedded systems. Addressing existing research challenges will contribute to the development of more efficient, scalable, and high-performance architectures. Future studies should focus on optimizing hardware utilization, minimizing latency, and enhancing power efficiency while ensuring high throughput. Furthermore, investigating hybrid architectures and AI-driven enhancements could further improve performance across various real-time applications.

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