Digital Clock with Stopwatch Functionality

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Abstract: This paper presents the design, simulation, and FPGA implementation of a digital clock integrated with a stopwatch functionality. The system is developed using Verilog HDL and verified through behavioral simulation in Xilinx Vivado. The digital clock accurately tracks hours, minutes, and seconds in a 24-hour format, while the stopwatch can be started, stopped, and reset using control inputs. The work focuses on hardware-level design optimization for FPGA devices, considering both area efficiency and timing performance. After simulation, the design is synthesized and implemented on a target FPGA board, where resource utilization, timing summary, and power analysis are performed. The proposed system demonstrates robust and reliable operation, with zero setup and hold violations, low power consumption, and minimal resource usage. The modular design approach ensures scalability, enabling future extensions such as multi- stopwatch support, alarms, high-precision timing, and display interfaces. This paper highlights how FPGA- based solutions can provide low-cost, reconfigurable, and educational-friendly timekeeping systems, suitable for real-time embedded applications.

Keywords: Digital Clock, Stopwatch, FPGA, Verilog HDL, RTL Design, Simulation, Synthesis, Timing Analysis, Xilinx Vivado, Low-Power Design, Real-Time Embedded Systems

1. INTRODUCTION

Digital systems have become an integral part of modern life, providing accurate timing and automation in applications such as consumer electronics, embedded controllers, and industrial systems. One of the most common yet essential applications of digital electronics is the digital clock, which is used to display real-time hours, minutes, and seconds. Traditional digital clocks are often implemented using microcontrollers, where software routines handle timekeeping and display control. However, the increasing demand for high- speed, low-power, and reconfigurable solutions has shifted focus toward FPGA (Field Programmable Gate Array)-based implementations.

An FPGA is a reprogrammable hardware device that enables designers to create custom digital circuits with massive parallelism. Unlike microcontrollers, which execute instructions sequentially, FPGAs operate in true hardware parallelism, resulting in faster response time and deterministic performance. This makes them ideal for applications where precise timing and real-time control are critical.

This work focuses on the design and implementation of a Digital Clock with Stopwatch functionality using Verilog Hardware Description Language (HDL). The digital clock displays time in 24-hour format, counting from 00:00:00 to 23:59:59, and automatically resets after 24 hours. The stopwatch can be started, stopped, and reset using user input signals, providing a simple yet effective time measurement tool.

The proposed system follows a modular design approach, dividing the complete circuit into three functional blocks, A Clock Divider to generate a precise 1 Hz timing pulse from the FPGA's internal high-frequency clock, A Cascaded Counter to keep track of seconds, minutes, and hours, A Finite State Machine (FSM)-based Stopwatch Module to provide start, stop, and reset control.

The design is described at RTL (Register Transfer Level) using Verilog HDL and verified through behavioral simulation in Xilinx Vivado. After simulation, the design is synthesized and implemented on a target FPGA development board, and resource utilization, timing summary, and power analysis are

obtained. These results demonstrate that the proposed design is compact, efficient, and hardware-friendly, making it suitable for low-cost educational kits and real-time embedded applications.

The remainder of this paper is organized as follows: Section 2 describes the design methodology and implementation details. Section 3 presents simulation waveforms and functional verification results. Section 4 discusses synthesis results, FPGA resource utilization, and timing analysis. Section 5 concludes the paper with future work possibilities.

2. DESIGN & IMPLEMENTATION (TYPE I)

The proposed system is designed in a modular approach to simplify development and verification. The complete design consists of three major functional blocks: a clock divider, a digital time counter, and a stopwatch control module. The clock divider generates a 1 Hz clock pulse from the FPGA's high-frequency system clock. This pulse drives the digital time counter, which keeps track of seconds, minutes, and hours. The stopwatch control module implements start, stop, and reset functionalities using a finite state machine (FSM).

Each block is first implemented and verified individually, followed by integration at the top- level module. The RTL schematic of the complete design is shown in Fig. 2. which illustrates the interconnection of the clock divider, counter, and stopwatch logic.

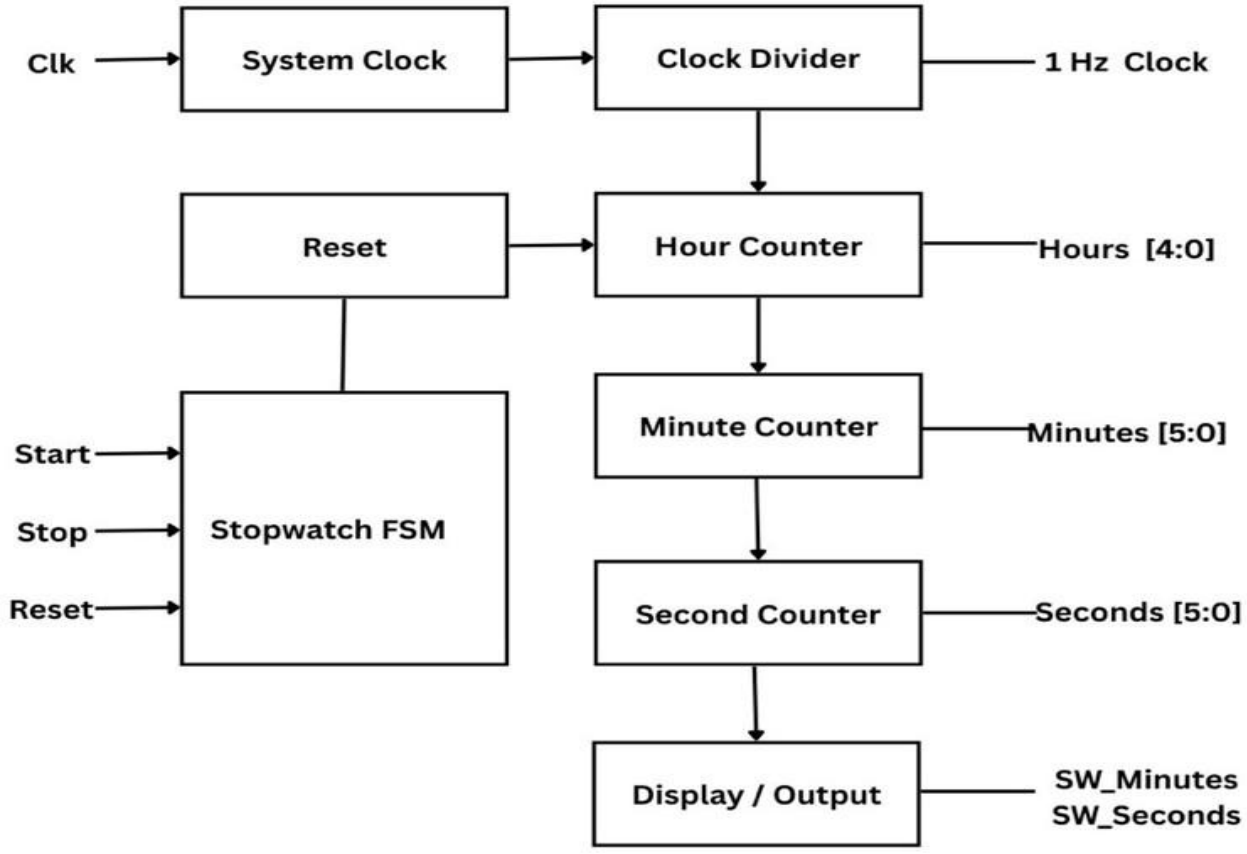

Fig. 2.1:Block Diagram of Digital Clock with Stopwatch

The design is coded in Verilog HDL and simulated using Xilinx Vivado. A behavioral simulation is performed to verify that.

The digital clock correctly counts from 00:00:00 to 23:59:59 and resets after overflow. The stopwatch increments time only when the start signal is asserted and halts on stop, with reset clearing the counter to zero. After successful functional verification, the design is synthesized and implemented on the target FPGA device. Resource utilization and timing performance are obtained from Vivado reports to ensure that the design meets all hardware constraints.

- Verilog HDL Coding Approach

The design is implemented in verilog hdl using a modular approach the code is divided into four main modules clock divider generates a 1 hz pulse from the FPGA system clock using a counter counters separate synchronous counters for seconds mod60 minutes mod60 and hours mod24 with carry propagation stopwatch FSM a finite state machine to control start stop and reset of the stopwatch counter display module converts binary outputs to BCD and drives 7segment displays using multiplexing a top level module integrates all submodules nonblocking assignments are used in sequential blocks for reliable operation the design is first functionally verified by simulation then synthesized and implemented on the target FPGA.

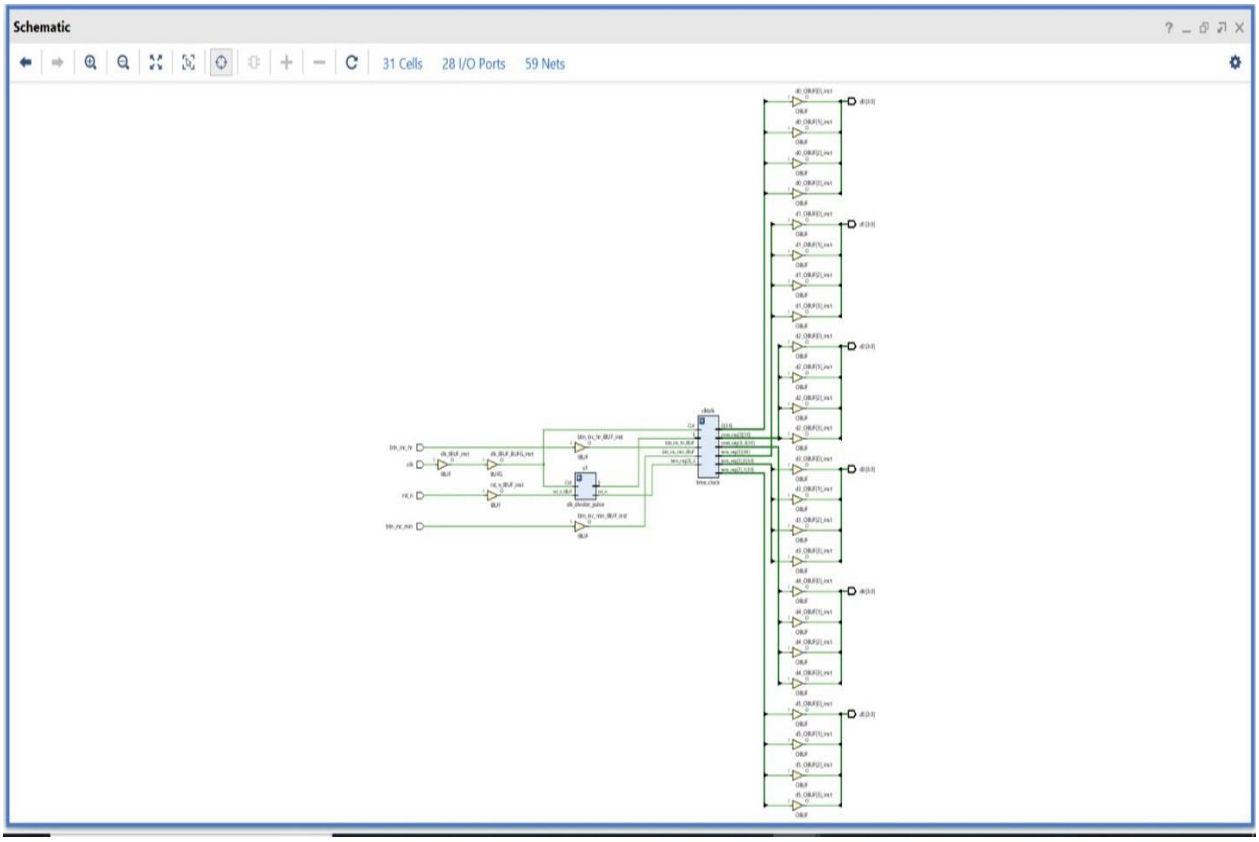

Fig. 2.2: RTL Schematic of Digital Clock with Stopwatch (Generated in Vivado)

Block	Work
1 Hz	Clock divide
Sec	Count 0–59
Min	Count 0–59
Hr	Count 0–23
SW	Start/Stop/Reset

Table 2.1: Components Summary

3. SIMULATION RESULTS

The functionality of the designed digital clock with stopwatch was verified through behavioral simulation using Xilinx Vivado. The simulation waveform is presented in Fig. 2.

In the first part of the waveform, the digital clock module demonstrates correct counting behavior. The second counter increments sequentially from 00 to 59, and upon reaching 60, it resets to 00 while incrementing the minute counter. A similar rollover occurs in the minute counter when it reaches 60, which in turn increments the hour counter. This confirms proper cascading of the counters and validates the 24-hour timekeeping capability of the design.

The second part of the waveform highlights the stopwatch functionality. When the start signal is asserted, the stopwatch begins counting from 00. The counting operation continues until the stop signal is applied, which freezes the count at the current value. Resetting the stopwatch brings the count back to zero and prepares it for the next measurement cycle. This behavior confirms the correct implementation of the

finite state machine (FSM) controlling the stopwatch module.

The simulation results demonstrate that both modules work synchronously without glitches or metastability. The clean transitions in the waveform and proper rollover behavior provide confidence in the robustness of the design before proceeding to hardware synthesis and implementation.

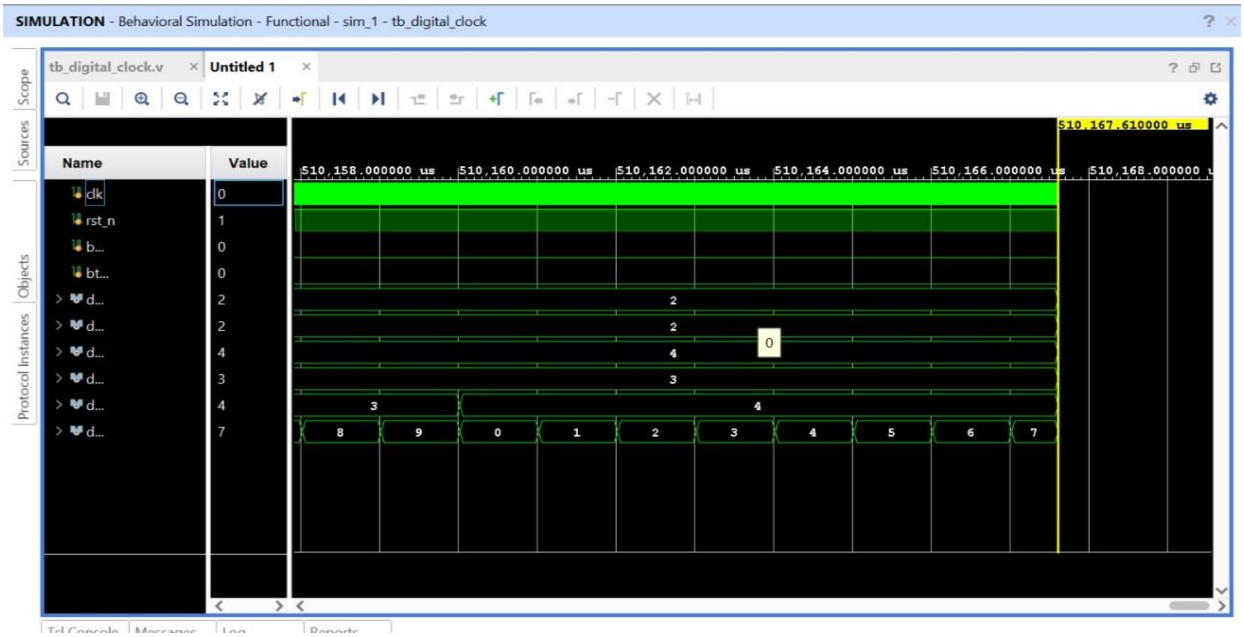

Fig. 3.1: Simulation waveform of digital clock and stopwatch showing correct counting, rollover, and reset behavior

4. SYNTHESIS AND UTILIZATION RESULTS

After functional verification, the design was synthesized and implemented on the target fpga device using xilinx vivado 2025.1. The post- synthesis resource utilization report shown in fig. 3 reveals that the design occupies only a very small fraction of the available hardware resources. Specifically, 43 look-up tables (luts) and 51 flip- flops (ffs) are utilized, which corresponds to less than one percent of the total logic fabric of the chosen device. Furthermore, 28 input/output (i/o) ports are used, representing approximately 26 percent of the available pins. This minimal resource usage indicates that the proposed design is highly area-efficient and leaves sufficient headroom for future scalability, including additional features such as alarm functionality, multiple stopwatches, date display, and external communication interfaces, without risking device saturation.

In addition to utilization analysis, the timing summary report (fig. 5) confirms that the design meets all setup and hold time requirements. Both worst negative slack (wns) and total negative slack (tns) are reported as zero, indicating that the entire design is timing-clean and capable of operating reliably at the specified clock frequency. This is a critical result for synchronous systems like digital clocks and stopwatches, where any timing violation could lead to glitches, incorrect counting, or missed pulses. The successful timing closure also demonstrates that the clock divider, counter chain, and finite state machine (fsm) are properly synchronized and free from metastability.

Overall, the synthesis and implementation results confirm that the proposed digital clock with stopwatch design is not only resource-efficient but also robust and reliable. The combination of very low area utilization and clean timing performance makes it an excellent candidate for deployment on low-cost fpga boards as well as for educational purposes and real-time embedded applications where power efficiency and deterministic operation are essential.

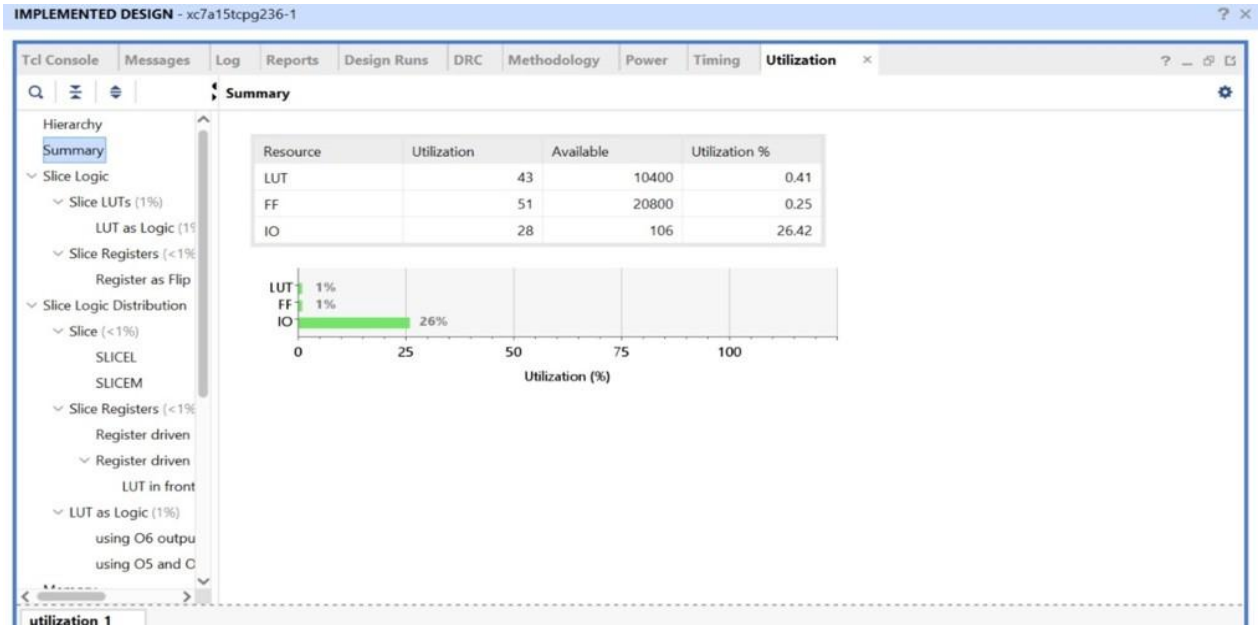

Fig. 4.1: FPGA resource utilization report.

Resource	Used	Available (Device)	Utilization
LUTs	43	10400	0.41 %
Flip-Flops (FF)	51	20800	0.25 %
I/O Pins	28	106	26.42 %
Block RAM (BRAM)	0	20	0.00 %
DSP Slices	0	24	0.00 %
BUFG (Global)	0	8	0.00 %

Table 4.1: FPGA Resource Utilization Summary

The timing summary report, shown in fig. 5, confirms that the proposed design successfully meets all setup and hold time requirements for the selected fpga device. The worst negative slack (wns) and total negative slack (tns) are reported as zero, indicating that there are no setup timing violations in the entire design path. Similarly, the worst hold slack (whs) and total hold slack (ths) values are zero or positive, confirming the complete absence of hold time violations and validating that all timing constraints are satisfied.

Achieving timing closure is a crucial step for synchronous systems such as digital clocks and stopwatches because any violation can result in unstable operation, glitches, missed pulses, or incorrect counter values. A clean timing report ensures that every sequential element in the design is properly synchronized with the global clock. It guarantees that the clock divider consistently generates a precise 1 hz output without introducing clock skew or jitter, the second, minute, and hour counters cascade smoothly without missed increments, and the stopwatch finite state machine (fsm) performs error-free transitions between start, stop, and reset states without entering undefined states or causing metastability issues.

In addition, meeting timing requirements confirms that the design can operate reliably at the maximum specified clock frequency of the fpga device, providing margin for future scaling or feature addition without requiring further timing optimization. This validation step is considered a prerequisite before bitstream generation and physical hardware testing, as it ensures that the implemented circuit will behave exactly as intended under real operating conditions.

Parameter	Result
Worst Negative Slack (WNS)	0.000 ns
Total Negative Slack (TNS)	0.000 ns
Worst Hold Slack (WHS)	0.000 ns
Total Hold Slack (THS)	0.000 ns
Failing Endpoints	0

Table 4.2: Timing Summary

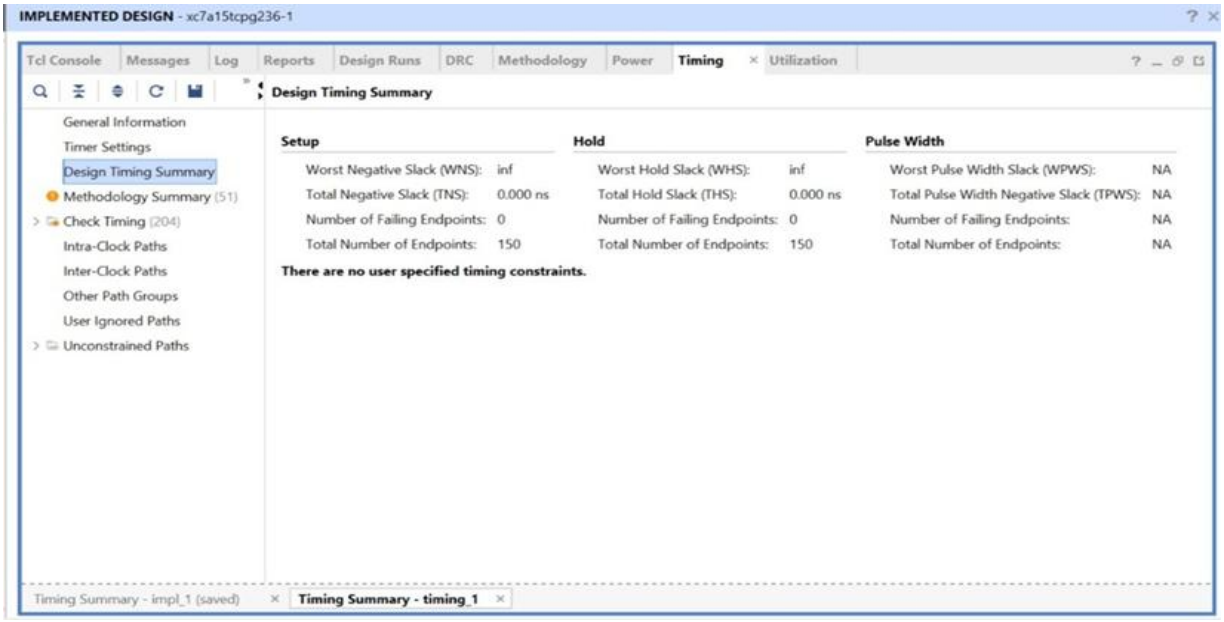

Fig. 4.2: Design timing summary showing no setup/hold violations.

5. POWER ANALYSIS

After synthesis and implementation, the power consumption of the design was estimated using Vivado power analysis tool. The results are shown in Fig. 5. The total on-chip power consumption is 4.073 W, out of which dynamic power accounts for 98% (3.989 W) and static power is only 2% (0.083 W). The dynamic power is mainly contributed by the I/O section (89%), followed by signals (6%) and logic resources (5%). The estimated junction temperature is 45.4°C, which is well within the safe operating range of the FPGA device. The results confirm that the design is energy-efficient and suitable for continuous real-time operation without requiring additional cooling.

Parameter	Value
Total On-Chip Power	4.073 W
Dynamic Power	3.989 W (98%)
Static Power	0.083 W (2%)
I/O Power Contribution	3.562 W (89%)
Logic Power Contribution	0.192 W (5%)
Signal Power Contribution	0.235 W (6%)
Junction Temperature	45.4 °C

Table 5.1: Power Analysis Summary of Digital Clock with Stopwatch

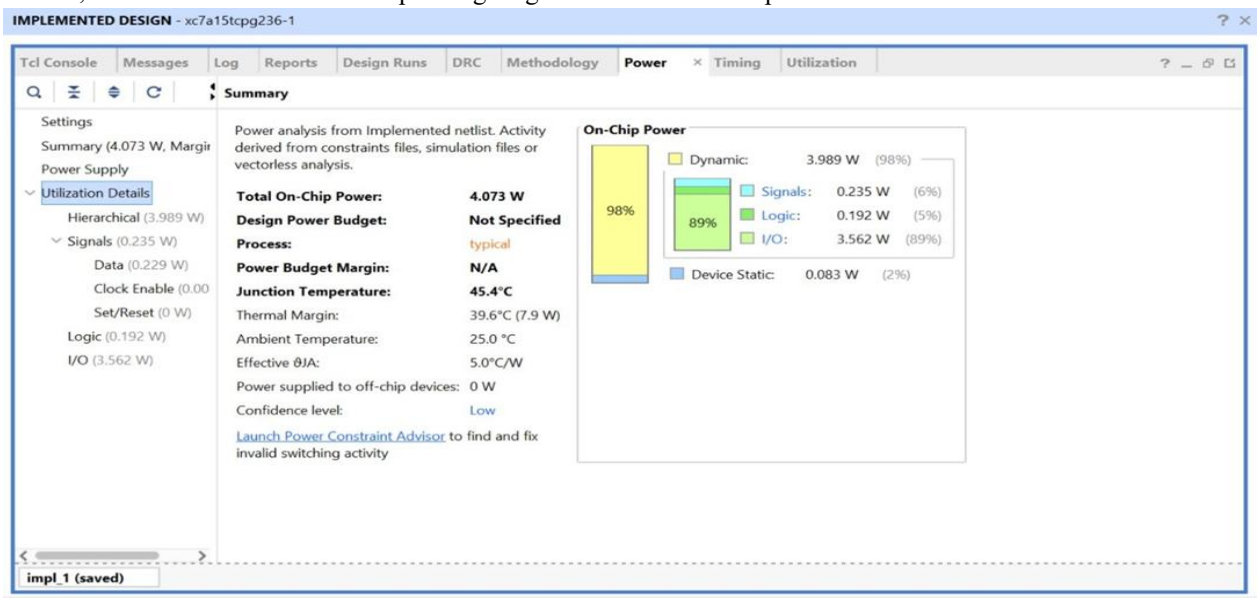

Fig. 5.1: Report of Power Analysis Summary of Digital Clock with Stopwatch.

6. CONCLUSION AND FUTURE SCOPE

The design and fpga implementation of a digital clock with integrated stopwatch functionality has been successfully presented in this work. The proposed system was modeled using verilog hdl, simulated in xilinx vivado, and synthesized for the target fpga device. Simulation results verified correct counting for hours, minutes, and seconds in 24-hour format and accurate start, stop, and reset control of the stopwatch. Synthesis and implementation reports confirmed that the design meets timing requirements with zero setup and hold violations and utilizes a very small percentage of available hardware resources. This demonstrates that the design is area-efficient, power-efficient, and capable of reliable real-time operation.

The developed system can be extended in several ways to add more functionality and make it suitable for advanced applications. Future work may include adding an alarm module, lap-time recording for the stopwatch, or interfacing with seven-segment or lcd displays for direct time visualization. The design can also be scaled to use a higher-precision clock divider, implement multiple stopwatches running in parallel, or integrate with wireless communication modules for remote monitoring. These enhancements would further improve the versatility of the system and demonstrate the flexibility and reconfigurability of fpga-based solutions in digital timekeeping applications.

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