A High-Gain, High-Power-Density DC-DC Converter Based on an Interleaved Multi-Cell Forward Topology

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Abstract—**This paper presents the design, analysis, and experimental validation of a high step-up, phase-shifted DC-DC converter based on a multi-cell forward topology. The proposed configuration employs three forward converter cells with inputs connected in parallel and outputs connected in series (IPOS). This architecture ensures intrinsic sharing of the high input current, thereby reducing component stress and improving thermal performance, while the series-output connection and transformer turn ratio collectively achieve a high static gain without requiring an extreme duty cycle. A phase-shift modulation strategy, implemented via a PIC microcontroller and gate-driver circuitry, is applied to the interleaved switches. This technique effectively reduces the magnitude of the current ripple output, enabling a significant reduction in the size and volume of the single output LC filter. A comprehensive steady-state analysis, including operational stages and the derivation of design equations, is provided. The performance of the converter is verified through a 1-kW laboratory prototype, converting 24 V DC input to 210 V DC output. Experimental results demonstrate stable closed-loop operation, confirm the current-sharing capability among the parallel cells, and validate the reduction in output ripple due to interleaving. The converter proves to be a compact and efficient solution, making it highly suitable for applications requiring high voltage gain from low-voltage sources, such as renewable energy systems, electric vehicle powertrains, and energy storage interfaces.**

Index Terms—**High Step-Up DC-DC Converter, Forward Converter, Input-Parallel Output-Series (IPOS), Current Sharing, Phase-Shift Modulation, Filter Reduction.**

I. INTRODUCTION

The global energy landscape is undergoing a profound transformation, driven by the urgent need for decarbonization and the rapid integration of renewable energy sources into the power grid. This paradigm shift, supported by advancements in power electronics, sophisticated microprocessors, and robust communication protocols, is moving electricity generation away from centralized fossil-fuel plants towards distributed generation (DG) units. Among these, photovoltaic (PV) systems and wind turbines (WTs) have emerged as cornerstone technologies. However, their inherent intermittency, caused by fluctuating weather conditions, poses a significant challenge to grid stability and reliability. A widely proposed solution to this problem involves the use of energy storage systems, such as battery banks and, increasingly, hydrogen fuel cells. These systems store excess energy during peak generation periods for later use, ensuring a consistent and dispatchable power supply.

A critical technical hurdle in this architecture is the interface between these low-voltage, high-current sources and the higher-voltage DC link or grid inverter. Batteries and fuel cells typically operate at low voltages (e.g., 24V, 48V), while grid-tied inverters or motor drives require significantly higher DC voltages (e.g., 400V, 800V). This necessitates a high step-up DC-DC conversion stage that must be not only efficient and reliable but also compact and cost-effective. The challenge is twofold: first, to achieve a high voltage conversion ratio without resorting to extreme duty cycles that degrade efficiency and increase component stress; and second, to manage the high input currents, which, if not properly shared, lead to excessive conduction losses, thermal management issues, and reduced system reliability.

The literature presents a plethora of techniques to enhance the voltage gain of DC-DC converters. These can be broadly categorized into the use of switched capacitor/inductor networks, voltage multiplier cells, magnetic coupling through transformers or coupled inductors, multilevel structures, and the cascading of

converter stages. While effective for gain enhancement, many of these approaches do not inherently address the challenge of input current sharing. For high-current applications, interleaving methods—where multiple converter phases operate in parallel with phase-shifted control signals—are commonly employed to divide the input current, thereby reducing the current ripple and the stress on individual components. Furthermore, systematic connections of multiple converter modules have been explored to manage voltage and current stresses. These configurations include Input-Series Output-Series (ISOS), Input-Series Output-Parallel (ISOP), Input-Parallel Output-Series (IPOS), and Input-Parallel Output-Parallel (IPOP), each offering distinct advantages for specific input-output requirements.

The Forward converter, a well-established isolated topology, is a strong candidate for such applications due to its simplicity, inherent transformer isolation, and straightforward control. However, a standard single-switch Forward converter has limitations in its duty cycle (typically <50% to allow for transformer reset), constraining its maximum achievable gain. Researchers have attempted to overcome this by integrating gain extension techniques. For instance, Abramovitz et al. [2] focused on improving the Forward converter's efficiency with an energy regenerative snubber, addressing losses but not primarily focusing on ultra-high gain. Other studies have explored interleaved boost-derived topologies; Chen et al. [1] proposed an interleaved converter with a parallel-input series-output configuration and a voltage multiplier module, achieving high gain but potentially increasing component count and control complexity. Meanwhile, research into non-isolated high-gain topologies, such as the coupled-inductor based converters presented by Kothapalli et al. [3] and demonstrates significant gain improvement through switched-inductor and switched-capacitor techniques, though they forfeit the critical safety and noise immunity benefits of galvanic isolation.

Despite these advancements, a discernible research gap persists. Many existing solutions achieve high gain at the cost of increased circuit complexity, unbalanced current sharing requiring additional control loops, or merely relocating the problem of component stress. Crucially, the ripple reduction in interleaved systems often still necessitates large, bulky passive output filters, which contradict the pressing

need for high power density in modern applications like electric vehicles (EVs) and compact renewable energy systems. There is a clear need for a converter topology that synergistically integrates high step-up capability, inherent and balanced input current sharing, and a fundamental reduction in the output filter size without compromising performance or reliability.

To address this multifaceted challenge, this paper proposes a novel, modular DC-DC converter architecture based on a multi-cell Forward converter topology. The proposed design employs multiple identical Forward converter cells in an Input-Parallel Output-Series (IPOS) configuration. This arrangement is the cornerstone of its performance: the parallel inputs naturally share the high input current, reducing conduction losses and improving thermal distribution, while the series-connected outputs inherently sum the individual cell voltages to achieve a high static gain, expressed as

$$G = nND$$

where n is the transformer turns ratio, N is the number of cells, and D is the duty cycle. This allows for a substantial voltage boost without operating at extreme duty ratios.

The second key innovation is the application of phase-shift modulation to the control of the interleaved power switches. By phase-shifting the Pulse-Width Modulation (PWM) signals of the three cells by 120°, the input current and, more importantly, the output current pulses are staggered. This interleaving effect creates a significant cancellation of the current ripple at the common output, thereby dramatically reducing the magnitude of the ripple that the output filter must attenuate. This permits the use of a smaller, single-stage LC filter, directly contributing to a reduction in the converter's size, weight, and cost—a critical metric for power density.

This work provides a comprehensive analysis of the proposed converter, including a detailed examination of its operational stages, steady-state modeling, and the derivation of design equations for key components such as the transformer, output inductor, and capacitor. The theoretical analysis is supported by both simulation studies and experimental validation from a 1-kW laboratory prototype. The prototype, controlled by a PIC16F877A microcontroller, successfully demonstrates the conversion of a 24V DC input to a regulated 210V DC output, validating the

converter's closed-loop performance, current-sharing capability, and the efficacy of its filter reduction strategy. The proposed converter thus presents a compelling solution for high-power applications demanding high voltage gain, inherent reliability, and a compact form factor, such as renewable energy integration, EV powertrains, and industrial power supplies.

The remainder of this paper is organized as follows: Section 2 details the proposed converter topology and its operational principles. Section 3 presents the steady-state analysis and design methodology. Section 4 discusses the simulation results, while Section 5 provides the experimental verification from the hardware prototype. Finally, Section 6 offers a conclusion and discusses potential avenues for future work.

II. PROPOSED CONVERTER TOPOLOGY AND OPERATING PRINCIPLE

A. Block Diagram of Proposed system:

The proposed high step-up DC-DC converter is architected around a modular, multi-cell structure to simultaneously achieve high voltage gain, intrinsic current sharing, and reduced output filtering. The core power stage, illustrated in Fig. 2.1, comprises three identical Forward converter cells. The fundamental innovation lies in their interconnection: the inputs of the three cells are connected in parallel to a common low-voltage source (Vin), while their outputs are connected in series, feeding a single load (Ro). This configuration is classified as an Input-Parallel Output-Series (IPOS) system.
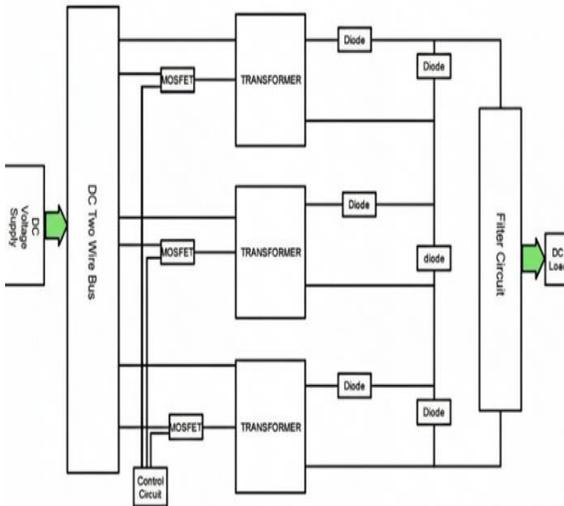

Fig. 2.2 Block Diagram Of High Step-Up Forward DC–DC Converter With Current Sharing And Filter Reduction

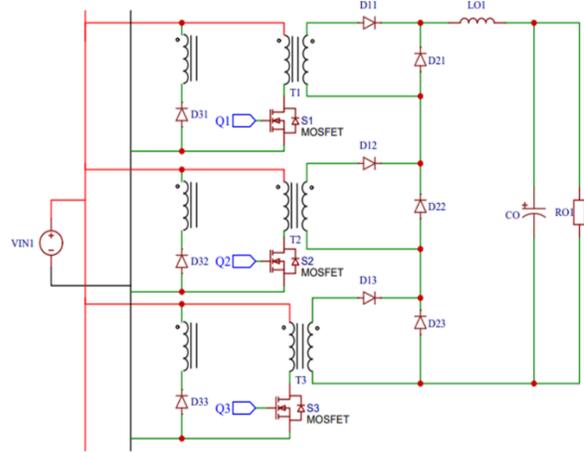*B. Circuit Diagram of Proposed system:*

Fig. 2.1 Circuit Diagram Of High Step-Up Forward DC–DC Converter With Current Sharing And Filter Reduction

Each individual cell consists of a primary-side power switch (S_1, S_2, S_3—implemented with MOSFETs IRF840), a high-frequency transformer (T_1, T_2, T_3) with a turns ratio of n:1 (where n > 1), and a secondary-side rectification stage. The rectification stage employs two diodes (e.g., D_{11} & D_{12} for Cell 1) to form a full-wave rectifier, ensuring efficient energy transfer and proper transformer reset. The outputs of these rectifiers are connected in a series-aiding configuration.

The control system, central to the converter's performance, is built around a PIC16F877A microcontroller. This controller generates three sets of Pulse-Width Modulation (PWM) signals, each phase-shifted by 120° relative to the others. These low-power signals are then fed into TLP250 optocoupler-based gate drivers, which provide necessary current amplification and critical galvanic isolation before driving the gates of the respective MOSFETs. Finally, the combined series output is passed through a single, minimized LC filter (L_0, C_0) to smooth the output voltage before it is delivered to the load.

1. Operating Principle and Switching Modes

The operation of the converter can be analyzed by examining its key switching states over one complete switching cycle, T_s. Due to the 120° phase-shift interleaving, the three cells operate in a cyclic, overlapping sequence. The following analysis describes three distinct, representative stages.

- Stage 1 [$t_0 - t_1$] (Active Power Transfer from Cell 1): During this interval, the gate drive signal is high for switch S_1, turning it ON. Switches S_2 and S_3 are in the OFF state. The input voltage V_{in} is applied across the primary winding of transformer T_1. This energizes the transformer, causing the primary current to ramp up linearly. The energy is magnetically coupled to the secondary side, where a voltage of $n*V_{in}$ is induced. This forward-biases diode D_{11} (or D_{21}, depending on the polarity), allowing current to flow into the output circuit. The output capacitors of Cell 2 and Cell 3, which are in series with Cell 1's output, also contribute to supplying the load. During this stage, the output inductor L_0 stores energy, and the filter capacitor C_o is charged. The input current is drawn solely through Cell 1 at this moment.
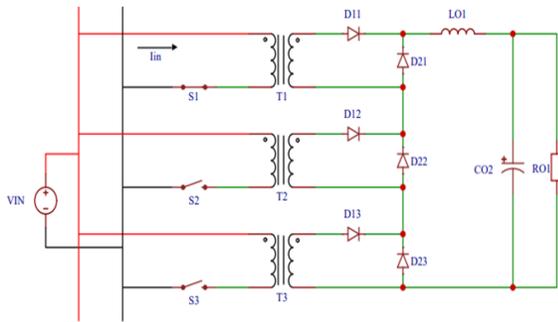

Fig. 2.3.1 Switching Mode Stage 1

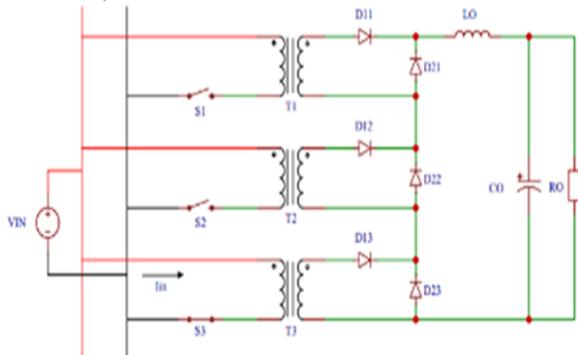- Stage 2 [$t_1 - t_2$] (Active Power Transfer from Cells 1 & 2):

Fig. 2.3.2 Switching Mode Stage 2

At time t_1, switch S_2 turned ON based on its phase-shifted control signal, while S_1 remains ON and S_3 is OFF. This is a key overlapping state. Both transformers T_1 and T_2 are now actively transferring energy to the output. Their respective secondary voltages, each equal to $n*V_{in}$, appear in series. The total voltage presented to the output filter at this point is the sum of the voltages from the two active cells. The input current is now shared between the primary windings of T_1 and T_2,

demonstrating the natural current-sharing property of the parallel-input configuration

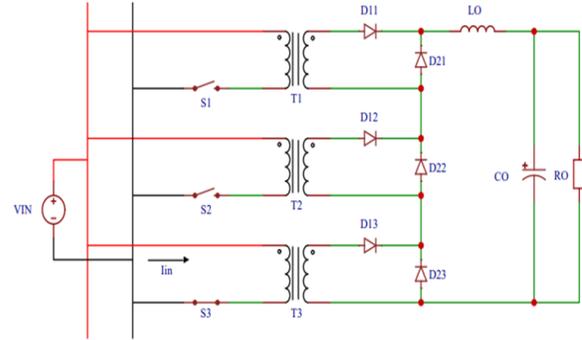- Stage 3 [$t_2 - t_3$] (All Switches OFF / Freewheeling):

Fig. 2.3.3 Switching Mode Stage 3

At time t_2, switch S_1 is turned OFF. For a brief period, all three switches (S_1, S_2, S_3) are OFF. The transformer primary currents rapidly collapse, and the magnetizing energy stored in each transformer core is returned to the circuit, resetting the cores through the tertiary windings or the inherent reset mechanisms. On the secondary side, all rectifier diodes are reverse-biased. The energy stored in the output inductor L_0 during the active phases is now released, maintaining current flow to the load through the freewheeling path. The capacitor C_0 discharges to supplement the energy and maintain a stable output voltage. This stage continues until the next switch (e.g., S_3) is turned ON, commencing the next cycle of the sequence.

2. Key Analytical Insights

The operation described yields several critical advantages:

High Static Gain: The output voltage is theoretically given by $V_0 = n* N*D*V_{in}$, where $N=3$ is the number of cells and D is the duty cycle. The gain is multiplicatively enhanced by both the transformer turns ratio (n) and the number of series-connected cells (N), allowing for a high step-up ratio without a prohibitively high duty cycle.

Intrinsic Input Current Sharing: The parallel-input connection forces the average input current to divide naturally among the N cells. This reduces the current stress on each individual switch and transformer, leading to lower conduction losses, improved thermal performance, and enhanced overall reliability.

Output Ripple Reduction via Interleaving: The phase-shifted operation of the switches ensures that the current pulses delivered to the output filter are staggered. This interleaving effect results in a

significant cancellation of the ripple current in the output inductor L_0 and a consequent reduction in the output voltage ripple. This is the fundamental principle that allows for the use of a smaller, more compact filter compared to a non-interleaved or synchronously switched system

III. SIMULATION AND MODELLING
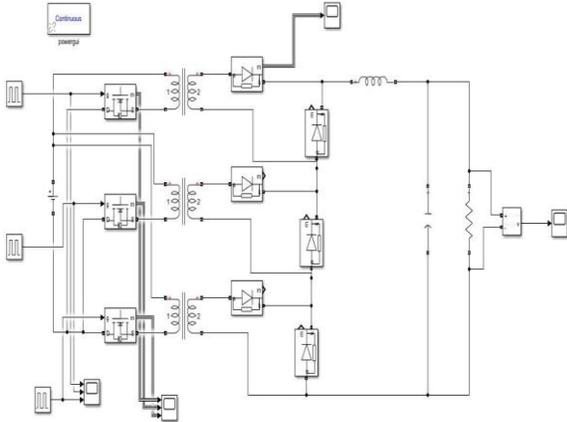
A) Simulation and results:

Fig. 3.1 Simulation Diagram Of High Step-Up Forward DC–DC Converter With Current Sharing And Filter Reduction

Three PWM generators are used to produce gate signals for the power switches in each phase of the converter. These PWM signals are interleaved, typically shifted by 120 degrees, to reduce the overall input and output ripple currents. Each converter phase contains a power switch (like an IGBT or MOSFET), a diode, and an inductor, which together form the core boost conversion circuit.

The three phases are connected in parallel, sharing the input source and combining their outputs to supply a common load. The output of each phase is summed at a node and then passed through an LC filter. The inductor and capacitor in the filter help to smooth out the pulsating DC voltage and reduce ripple before reaching the load. A resistive load is connected to the output, simulating power consumption. Voltage and current measurement blocks are used to observe the output characteristics and ensure proper operation.

This interleaved approach enhances performance by improving efficiency and distributing thermal stress among switches. It also ensures better utilization of components and faster transient response. Interleaving significantly reduces input current ripple, allowing the use of smaller filter components. It is commonly used in renewable energy systems, electric vehicles, and power supplies. Overall, the model is a practical implementation of an advanced DC-DC boost topology that demonstrates optimized power conversion using three-phase interleaving.

• *Simulation results :*

The response of an output current over time. It shows a typical transient behavior where the current quickly rises from zero and stabilizes around a steady-state value of approximately 7.5 units (possibly amperes). This indicates that the system reaches a steady state very rapidly with minimal overshoot and no significant oscillations, suggesting good dynamic performance and stable output. The smooth curve and quick settling time reflect an efficient control or regulation mechanism in the system, such as in a power converter or current-regulated power supply.

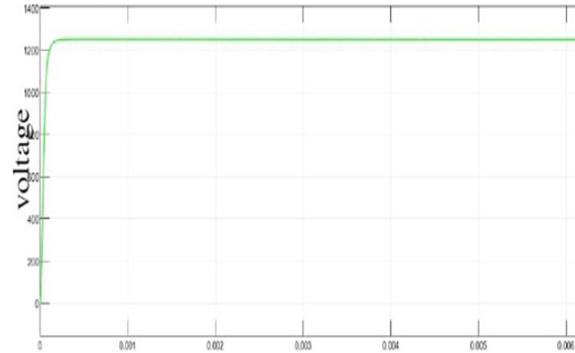Fig. 3.3 A) Simulation Of Output Current

Fig. 3.3 B) Simulation Of Output Voltage

The output voltage response of a system over time. The voltage rises sharply from zero and quickly stabilizes around 1200 volts, indicating a fast transient response with minimal overshoot or oscillations. The smooth, steady rise and flat line after the initial surge show that the system efficiently reaches its desired output voltage and maintains it without significant fluctuation. The x-axis represents time in seconds (up to 0.01 seconds), highlighting the system's rapid stabilization. The y-axis, labeled "voltage," confirms

the output voltage reaches and holds a value near 1200V, which is typical in regulated power supply or high-voltage converter applications.

B) Mathematical Modelling :

• Input voltage Vin= 24 V
• Desired output voltage Vout = 210
• Number of Forward converters N=3
• Switching frequency fs= 50 kHz
• Let's assume a duty cycle D=0.4

1)   Turns Ratio for Transformer Static Gain formula

$$G = nND$$

Where,

•   G is the static voltage gain
•   n is the transformer turn ratio
•   N is the number of forward converters
•   D is the duty cycle.

Step 1: Calculate required gain

$$G = \frac{Vout}{Vin} = \frac{210}{24} = 8.75$$

Step 2: solve transformer turn ratio n

$$Turn\ ratio = \frac{Vout}{Vin} = \frac{210}{24} = 8.75$$

$n = 8.75$
$N1 : N2 = 1 : 8$

2) Output filter design and Duty Cycle Estimation

$$G = \frac{Vo}{Vi} = nND$$

$$D = \frac{Vo}{nNVi}$$

$$D = \frac{210}{8.75 \times 3 \times 24} = \frac{210}{630} = 0.333$$

IV. HARDWARE IMPLEMENTATION

Hardware photo

To validate the theoretical analysis and simulation results, a 1-kW laboratory prototype of the proposed high step-up DC-DC converter was designed and constructed. This section details the hardware realization, including the specification of components, the printed circuit board (PCB) design, the test setup, and the methodology for data acquisition.

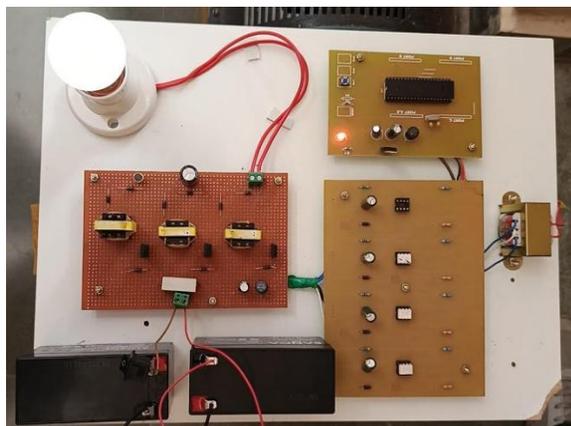Prototype Specifications and Component Selection
The prototype was designed for a nominal input voltage of V_{in}= 24V and a target output voltage of V_{out}= 210 V - 230 V at a maximum output power of 1 kW. The switching frequency was set at f_s= 50 kHz for all three converter cells.

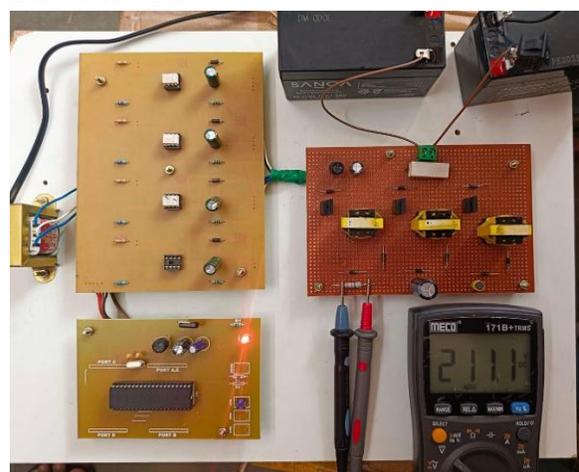The component selection was critical to ensure reliable operation under these specifications:

Control Unit: The heart of the control system is a PIC16F877A 8-bit microcontroller. It was programmed in C to generate three independent PWM signals with the requisite 120° phase shift. A 10 MHz crystal oscillator provided the stable system clock. A 7805 linear voltage regulator provided a stable 5V supply from a 12V auxiliary source.

Gate Drive Circuit: Each MOSFET gate is driven by a TLP250 optocoupler-based driver IC. This component provides essential galvanic isolation between the low-voltage control circuitry and the high-voltage power stage, while also supplying the necessary current to rapidly charge and discharge the MOSFET gates. The TLP250s were supplied with an isolated 12V rail.

Hardware photo

V. CONCLUSION

In conclusion, a High Step-Up Forward DC–DC Converter with Current Sharing and Filter Reduction was successfully designed and implemented to convert a low input voltage of 24V DC to a high output voltage of 230V DC. The converter architecture efficiently utilized a forward converter topology integrated with a transformer for high voltage gain, while current sharing ensured balanced load distribution across multiple switches or modules. Filter reduction techniques further minimize the size and complexity of output filters without compromising voltage stability or quality.

The practical results confirmed the theoretical expectations, achieving a significant step-up voltage ratio with improved efficiency, reduced ripple, and better thermal management. This converter is especially suitable for renewable energy systems, battery-powered equipment, and grid-interface applications where compactness, reliability, and high voltage output are required.

Overall, the proposed converter system demonstrates a reliable and scalable solution for high-voltage DC power applications, supporting future innovations in energy-efficient power electronics.

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