Low Power Fast Adders Using New Xor and Xnor Gates

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***Abstract*—This paper presents the design and analysis of low power, high speed adders using newly proposed XOR and XNOR gates. The performance of arithmetic circuits largely depends on the efficiency of XOR and XNOR gates used in sum and carry generation. The proposed XOR/XNOR circuits are designed using a hybrid CMOS logic style that combines transmission gate logic and pass transistor logic to minimize power consumption, propagation delay, and transistor count. These optimized XOR/XNOR gates are then integrated into different adder architectures such as Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), and Carry Select Adder (CSLA). Simulation results, carried out using 90nm CMOS technology in Cadence Virtuoso, show that the proposed designs achieve significant improvements in terms of power, delay, and Power Delay Product (PDP) when compared to conventional CMOS adder implementations. Hence, the proposed low power fast adders using new XOR and XNOR gates are highly suitable for low voltage and high-performance VLSI applications.**

***Index Terms*—Low power design, Fast adders, XOR gate, XNOR gate, Hybrid logic, Ripple carry adder, carry look ahead adder, Carry select adder, CMOS VLSI, Power delay product, Transmission gate logic, Pass transistor logic**

I. INTRODUCTION

Electronic systems have become an integral part of modern life, powering a wide range of applications, from consumer electronics like smartphones and laptops to high-performance computing and industrial automation. These systems rely heavily on digital circuits, with microprocessors, digital signal processors (DSPs), and application-specific integrated circuits (ASICs) playing a pivotal role in data processing and computation. As the demand for increased functionality and performance continues to rise, there is a parallel need to enhance the efficiency of digital circuits in terms of power consumption, speed, and silicon area utilization.

With the rapid advancement of very large-scale integration (VLSI) technology, billions of transistors are integrated into a single chip, leading to increased power dissipation and area constraints. Battery-operated devices, such as smartphones, tablets, and wearable electronics, require energy-efficient and compact designs to ensure extended battery life while maintaining high computational performance. One of the critical challenges in VLSI design is to reduce the power-delay product (PDP), which is a key metric for evaluating the energy efficiency of a circuit. One effective way to achieve this is by optimizing the width-to-length (W/L) ratio of transistors, thereby improving switching characteristics and reducing power consumption
without lowering the supply voltage, which can otherwise degrade circuit performance.

1.1 Adder

An adder is a digital circuit that performs arithmetic operations, specifically addition. It is a fundamental building block in computer architecture and plays a crucial role in computations, data processing, and mathematical calculations.

1.2 Types of Adders

There are several types of adders, including half adders, full adders, ripple carry adders, look-ahead carry adders, carry skip adders, and carry-select adders. Each type has its own characteristics, trade-offs, and applications.

1.2.1 Half adder

A half adder is the simplest form of an adder. It takes two single-bit inputs, A and B, and produces two outputs: the sum (S) and the carry (C). The sum output represents the least significant bit of the addition, while the carry output indicates whether there is a carry-over to the next bit.

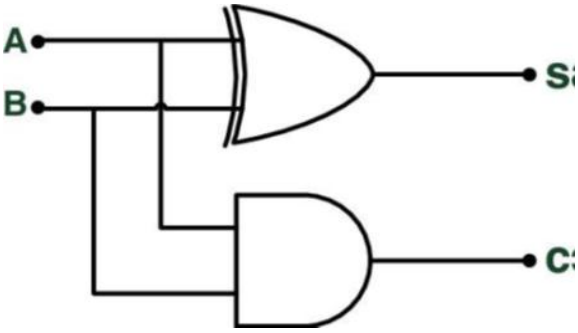


Fig 1.1: Half adder block diagram

1.2.2 Full adder

A full adder is an extension of a half adder. It takes three inputs: A, B, and a carry-in (Cin), and produces two outputs: the sum (S) and the carry (C). The carry-in represents the carry-over from the previous bit, allowing full adders to perform multi-bit additions.

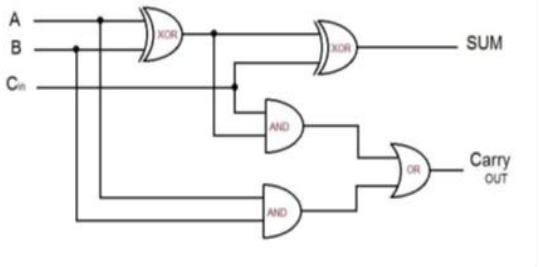


Fig 1.2: full adder block diagram

II LITERATURE SURVEY

A novel fast low-power and high-performance XOR-XNOR cell", Many existing XOR-XNOR cells suffer from non-full-swing outputs, high power consumption and low speed issues. In this paper, a new fast, full-swing and low-power XOR-XNOR cell, is presented. Simulation results in 90-nm CMOS technology show that the proposed circuit has rail to rail outputs Also, we have gained 11%-51%, 2%-19% and 18%-52% improvement in delay, power consumption and power-delay product (PDP), respectively. In order to do a comparison between the previously reported XOR-XNOR cells and our proposed circuit, they are embedded in a 4-2 compressor circuit and simulation results prove energy efficiency of ours in more complicated structures.

"Low voltage high performance hybrid full adder", This paper presents a low voltage and high performance 1-bit full adder designed with an efficient internal logic structure that leads to have a reduced Power Delay Product (PDP). The modified NOR and NAND gates, an essential entity, are also presented. The circuit is designed with cadence virtuoso tool with UMC 90-nm and 55-nm CMOS technologies. The proposed adder is compared with some of the popular adders based on power consumption, speed and power delay product. The proposed full adder cells achieve 56% and 76.69% improvement in speed and power delay product metric when compared with conventional C-CMOS full adder. It is also found that the proposed adder cells exhibit excellent signal integrity and driving capability when operated at low voltages.

"A robust power-gating structure and power mode transition strategy for MTCMOS design". The large magnitude of supply/ground bounces, which arise from power mode transitions in power gating structures, may cause spurious transitions in a circuit. This can result in wrong values being latched in the circuit registers. We propose a design methodology for limiting the maximum value of the supply/ground currents to a user-specified threshold level while minimizing the wake up (sleep to active mode transition) time. In addition to controlling the sudden discharge of the accumulated charge in the intermediate nodes of the circuit through the sleep transistors during the wake-up transition, we can eliminate short circuit current and spurious switching activity during this time.

III. METHODOLOGY

3.1 Existing System

A Full Adder (FA) is a fundamental arithmetic circuit used in digital systems to add three binary inputs: two operands (A and B) and a carry-in (Cin). It produces two outputs: Sum and Carryout (Cout). The CMOS implementation of a full adder is designed using complementary MOSFET logic.

A CMOS Full Adder can be built using static CMOS logic. The static CMOS design consists of:

XOR Gate Implementation: Built using CMOS transistors, producing Sum and intermediate results.

Multiplexer-Based Carry Generation: Using transmission gates or NAND/NOR gates for Cout computation.

Pull-up (PMOS) and Pull-down (NMOS) Networks: Ensuring rail-to-rail output voltage (full-swing operation).

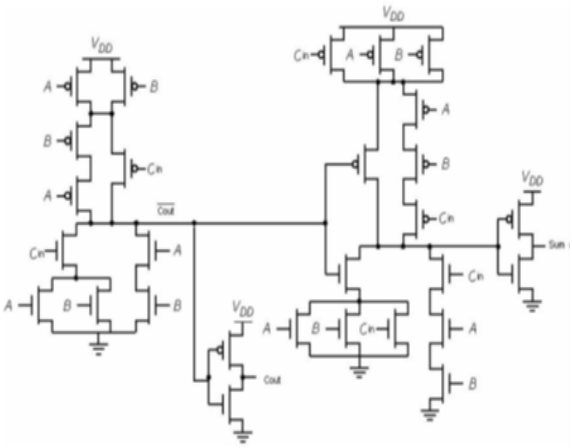


Fig 3.1: Existing full adder circuit

3.2 Disadvantages of Existing System

Higher Power Consumption – The existing full adder designs, especially in fullswing logic (CMOS), require more transistors, leading to increased dynamic and leakage power consumption. The proposed system reduces power by optimizing transistor count and improving logic design.

Increased Propagation Delay Traditional full adders, particularly those using complex carry propagation methods, introduce delays due to multiple logic levels. The proposed system minimizes delay by optimizing XOR/XNOR and carry logic circuits.

Larger Area Utilization Existing designs use more transistors, resulting in increased chip area, which is a critical factor in VLSI design. The proposed full adder structures and ripple carry adder (RCA) optimize the transistor count, reducing area without compromising performance.

IV. PROPOSED SYSTEM

Proposed Full Adder (FA) Circuits for Various Applications

This work introduces six innovative hybrid full adder (FA) circuits, which are illustrated in Fig. 4.5. These designs integrate optimized XOR/XNOR logic within a hybrid framework. The well-established four-transistor 2-to-1 multiplexer (MUX), depicted in Fig. 4.5(a), plays a central role in constructing these hybrid FA cells. The 2-to-1 MUX, implemented using transmission gate (TG) logic, effectively minimizes static and short-circuit power dissipation.

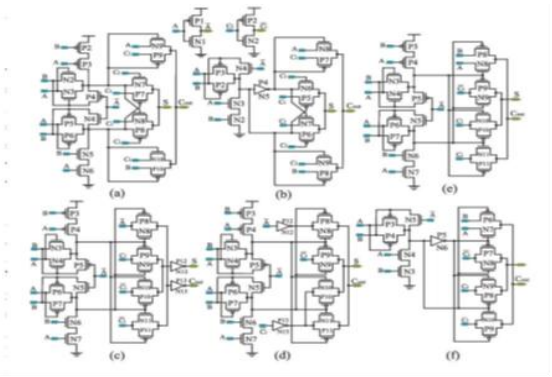


Fig 4.5: Proposed six new hybrid FA circuits. (a) HFA-20T. (b) HFA-17T. (c) HFA-B-26T. (d) HFA-NB-26T. (e) HFA-22T. (f) HFA-19T.

4.1. Six Proposed Full Adder Designs

The newly designed FA circuits include:

HFA-20T
HFA-17T
HFA-B-26T
HFA-NB-26T
HFA-22T
HFA-19T

4.1.1 HFA-20T: Hybrid FA with 20 Transistors

The first proposed FA design, HFA-20T, utilizes two 2-to-1 MUX gates along with an XOR–XNOR gate, as shown in Fig. 3.5(a). This structure, which consists of 20 transistors, achieves:

1. Full-swing output
2. Low power consumption
3. High-speed operation
4. Robust performance under supply voltage scaling and transistor sizing

V. SOFTWARE

Tanner EDA offers a comprehensive set of software tools for the design, layout, and verification of analog and mixed-signal (A/MS) integrated circuits (ICs).

Tanner's solution consists of tools for schematic entry, circuit simulation, waveform

probing, full-custom layout editing, placement and routing, netlist extraction, LVS and DRC verification. Their software is used by over 30,000 people.

when the tanner first released L-Edit in 1988, it ran under DOS and had a limit of 16

layers and orthogonal geometry. Dr. John Tanner founded the company in 1988 with the goal of

developing and marketing cost-effective, user-friendly EDA tools.

Tanner is a Spice Computer Analysis Developed for Optimized Analog Circuits. Mach motor makes up the tanner tool which consists of the following.

1 S-Edit (Schematic Entry Tool)
2 T-Sice (T Simulation Program with Integrated circuit Emphasis)
1. W-Edit (Waveforms Editor)
2. L-Edit (Layout Editor)

Before beginning the time - based and money-consuming chip manufacture process, the spice program makes it straight forward to simulate and model innovative designs in analogue microcontrollers.

5.1 Schematic Edit Tool (S-Edit)

S-Edit is a page structure, device, and script. There are now sign and diagram modes. There are picture and schematic modes available. One of the options in S-Edit includes the following options:

1.To start a plan.

1. Examining, sketching, and making changes to articles.
2. Availability of designs.
3. Real estate, financial information, and leisure.
4. Launch and browse image and schematic modes.

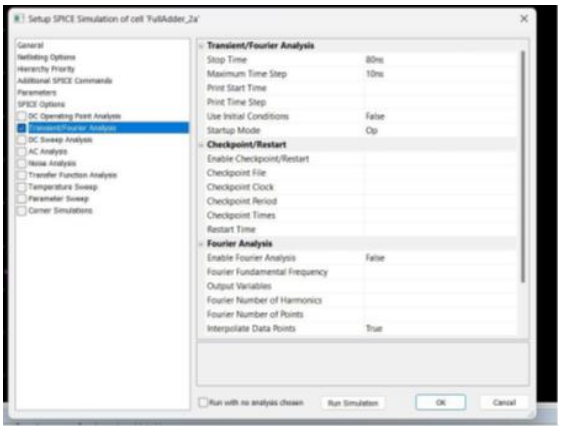
Beginning a design: The plan cycle is fully explained, including how to record module activities and module. Browser: A functional understanding of the records and module evolution in the S-Edit plan is necessary for a successful schematic design. S-Edit configuration papers are made up of modules. Similarly to a semiconductor, entrance, and intensifier, a module is a primary component of design. Modules consist of two components:

1. Primitives: Drawing tools were used to create geometric objects.
2. Instances: References to distinct modules in record. The first is the instanced module.

There are two editing modes in S-Edit:

1. Schematic Mode: In order to develop or read schematics, we use schematic mode.
2. Symbol Mode: It deals with the representation of a larger, more practical unit, such an operating speaker.

Fig5.1:S-Edit tool



VI. CIRCUIT DIAGRAMS & WAVEFORMS

6.1 Proposed Full Adder Circuit Diagrams

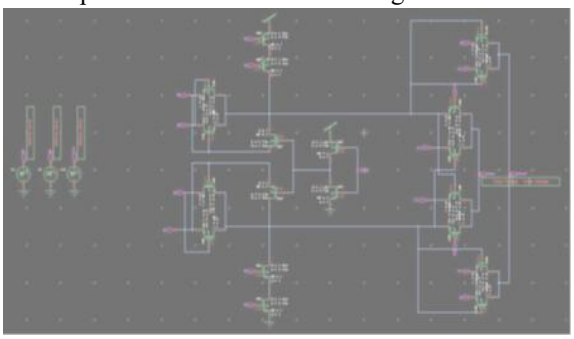


Fig 6.1: Full adder circuit with transistor count 20.

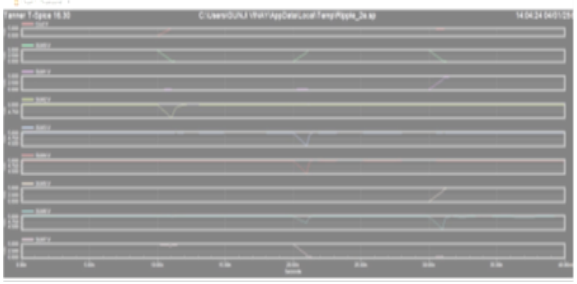


Fig 6.23: Output waveform of ripple carries adder

(22)

VII RESULT&CONCLUSION

7.1 Result

Comparison of power consumption and total time of different ripple carry adders by
using six proposed full adder circuits.

S.NO	TRANSISTOR COUNT	POWER CONSUMPTION	TOTAL TIME
1	28	171µw	2.26sec
2	20	146µw	1.26sec
3	17	60.4µw	0.66sec
4	26	122µw	1.55sec
5	26	63.7µw	1.63sec
6	22	56.3µw	1.19sec
7	19	81.5µw	0.64sec

For an existing full adder circuit, the power consumption and total time required for completing the operation is more. In order to minimize the power consumption, we proposed six new hybrid full adders. When compared to existing full adder the power consumption and total time should be reduced for a ripple carry adder by using six hybrid full adder circuits. In the above table, we observe that when the transistor count decreases the power consumption and total time required also reduces. And when compared to existing full adder circuit, the area utilization is less in proposed six new hybrid full adders.

7.2 Advantages

Reduced Power Consumption

The optimized transistor count and improved logic design minimize dynamic and leakage power, making it suitable for low-power applications.

Lower Propagation Delay

The enhanced XOR/XNOR and carry logic reduce the delay in full adders, improving the speed of the 8-bit ripple carry adder.

7.3 Applications

Digital Signal Processing (DSP)

Used in filtering, convolution, and FFT computations where fast and efficient arithmetic operations are required.

Low-Power Embedded Systems

Ideal for microcontrollers, IoT devices, and battery-operated systems like wearables and smart sensors.

Arithmetic Logic Units (ALUs)

Enhances the performance of ALUs in microprocessors and digital processors, improving computational speed and efficiency.

7.4 Conclusion

In this project, we implemented an 8-bit Ripple Carry Adder (RCA) using six different hybrid Full Adder (FA) circuits. Each of these FA designs was optimized for specific performance metrics, including power consumption, delay, and driving capability. The FA circuits were designed using a combination of XOR/XNOR gates and 2-to-1 multiplexers, leveraging transmission gate logic to minimize static and short-circuit power dissipation.

Among the proposed designs, the HFA-20T and HFA-17T prioritized transistor count reduction, leading to lower power consumption but limited driving capability. The HFA-B-26T and HFA-NB-26T incorporated buffer circuits to enhance output drive strength, improving reliability in cascaded stages like an RCA. Additionally, the HFA-22T and HFA-19T were optimized for reduced capacitance at XOR/XNOR nodes, leading to improved speed and efficiency.

By integrating these FA designs into an 8-bit RCA, we analysed their impact on overall circuit performance. The results demonstrated that FAs with buffers exhibited better output drive strength, making them more suitable for large-scale applications, whereas transistorefficient designs offered power savings but required additional buffering for effective cascading.

Thus, the selection of a suitable FA design depends on the specific application requirements, balancing trade-offs between power, speed, and area. This project provides valuable insights into designing efficient arithmetic circuits for VLSI applications, contributing to the development of high-performance digital systems

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