ASIC Implementation of 8-Bit Vedic Multiplier using Cadence

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Abstract— **This paper presents the design and ASIC implementation of an 8-bit Vedic multiplier using the Urdhva Tiryagbhyam sutra in 90 nm CMOS technology. A hierarchical structure built from 2×2 and 4×4 Vedic blocks forms the complete 8×8 architecture. The ASIC flow covers RTL modelling, simulation, synthesis, physical design, and parasitic extraction. The study highlights how Vedic mathematics enables parallel partial-product generation and modular, low-complexity design suitable for DSP, embedded systems, and low-power VLSI applications.**

Index-Terms—Vedic Multiplier, ASIC Design, Urdhva Tiryagbhyam, CMOS Technology, Physical Design, Cadence Innovus.

I. INTRODUCTION

Multiplication forms a key component of datapath units in CPUs, DSP processors, image-processing accelerators, neural-network hardware, and encryption engines. With the growing emphasis on battery-operated embedded systems, achieving low-power and high-speed multiplication has become essential. Conventional schemes such as Array multipliers suffer from high propagation delay due to sequential accumulation of partial products, whereas Booth multipliers reduce partial products but add encoding overhead.

Vedic mathematics, introduced by ancient Indian scholars, provides computational techniques that minimize complex intermediate steps. The Urdhva Tiryagbhyam (vertical-and-crosswise) sutra is inherently parallel—enabling concurrent generation of partial products and reducing the number of sequential operations.

The 90 nm technology node strikes a unique balance between performance and power. Although not as fast as deep-submicron nodes (like 45 nm), 90 nm offers significantly lowered leakage current and relaxed routing constraints, making it a stable node for educational ASIC prototyping and low-cost industrial applications.

This paper presents a detailed ASIC design flow and evaluation of an 8-bit Vedic multiplier implemented using a 90 nm standard-cell library, demonstrating the practicality of Vedic arithmetic in medium-performance digital circuits. The work further highlights how hierarchical Vedic structures simplify physical design and support efficient integration into modern low-power VLSI systems.

II. LITERATURE REVIEW

A. "Design and Implementation of 8-bit Vedic Multiplier Using Cadence 45 nm Technology" – V. Sharmila et al.

[1] The work titled "Design and Implementation of 8-bit Vedic Multiplier Using Cadence 45 nm Technology" by Sharmila and colleagues presents a complete ASIC flow for an 8-bit Vedic multiplier implemented at the 45 nm technology node. The authors focus on the physical design challenges encountered at deep-submicron scales, such as routing congestion, leakage behaviour, and timing closure. Their study demonstrates that the Urdhva Tiryagbhyam algorithm lends itself well to structured synthesis and clean floorplanning, helping achieve a compact and timing-friendly layout. This work provides a relevant benchmark for comparing behaviour across different nodes, including the more moderate 90 nm process.

B. "FPGA Implementation of Multiplier-Accumulator Unit Using Vedic Multiplier and Reversible Gates" – K. Rajesh and G. U. Reddy

[2] In "FPGA Implementation of Multiplier-Accumulator Unit Using Vedic Multiplier and Reversible Gates", Rajesh and Reddy propose a MAC unit that integrates the Vedic multiplier with reversible logic to reduce energy loss and support low-power computing paradigms. Their design exploits the inherent parallelism of Urdhva Tiryagbhyam while improving energy efficiency through reversible gates, which theoretically avoid information loss. Although implemented on FPGA, the work highlights the potential of combining Vedic arithmetic with reversible computing for power-critical applications, offering architectural insights that remain useful for ASIC-based designs as well.

C. "Speed and Power Efficient Reversible Logic Based Vedic Multiplier" – A. Eshack and S. Krishnakumar

[3] The paper "Speed and Power Efficient Reversible Logic Based Vedic Multiplier" by Eshack and Krishnakumar focuses on designing a Vedic multiplier using reversible logic to minimise power dissipation and improve computational efficiency. The authors demonstrate that reversible architectures effectively reduce switching activity and heat generation, making them suitable for future low-power VLSI systems. By combining reversible logic with the regular structure of the Urdhva Tiryagbhyam sutra, the work achieves improvements in both speed and energy utilisation, illustrating the adaptability of Vedic arithmetic to emerging logic styles.

D. "Fault Resistant 8-Bit Vedic Multiplier Using Repairable Logic" – B. S. Krishna et al.

[4] In "Fault Resistant 8-Bit Vedic Multiplier Using Repairable Logic", Krishna and co-authors propose a reliability-enhanced Vedic multiplier architecture capable of tolerating faults through built-in repairable logic. Their approach targets applications that require operational continuity under defect-prone or harsh environments. The repairable logic is integrated into the Vedic structure without significantly increasing critical-path delay, demonstrating that the regular and modular nature of Urdhva Tiryagbhyam is highly compatible with reliability-oriented enhancements. This work highlights the promise of Vedic multipliers in fault-tolerant VLSI design.

E. "Design of 8-Bit Vedic Multiplier Using Urdhva Tiryagbhyam Sutra with Modified Carry Save Adder" – M. N. Chandrashekara and S. Rohith

[5] The paper "Design of 8-Bit Vedic Multiplier Using Urdhva Tiryagbhyam Sutra with Modified Carry Save Adder" by Chandrashekara and Rohith presents an improved Vedic multiplier architecture integrating a modified carry-save adder to enhance speed. By optimising the partial-product addition stage, the authors reduce propagation delay while preserving the parallelism of the Urdhva Tiryagbhyam method. The design demonstrates that fine-grained adder optimisation can significantly boost overall multiplier performance, particularly for medium-bit-width arithmetic units.

F. "Design and Implementation of High-Speed 8-Bit Vedic Multiplier on FPGA" – A. Aravind Kumar and Sk. Mastan Basha

[6] In "Design and Implementation of High-Speed 8-Bit Vedic Multiplier on FPGA", Aravind Kumar and Basha implement an 8-bit Vedic multiplier targeting high-speed FPGA applications. Their work emphasises that the hierarchical decomposition of Vedic multiplication leads to shorter critical paths and better utilisation of FPGA resources compared to conventional multipliers. Although focused on reconfigurable hardware, the findings highlight key architectural strengths—parallel computation, modularity, and regular layout—that are equally beneficial in ASIC environments.

G. "Design of High Performance 8-Bit Multiplier Using Vedic Multiplication Algorithm with McCMOS Technique" – D. Kayal et al.

[12] The work "Design of High Performance 8-Bit Multiplier Using Vedic Multiplication Algorithm with McCMOS Technique" by Kayal and collaborators integrates McCMOS low-power logic with the Vedic multiplication algorithm to achieve enhanced switching efficiency and reduced power. The technique selectively controls charge recycling to minimise dynamic power consumption while improving speed. This combination of circuit-level optimisation with the structural efficiency of Vedic arithmetic demonstrates a strong pathway for designing high-performance and low-power multipliers in CMOS technology.

III. DESIGN METHODOLOGY

A. Architectural Description

The architecture of the 8-bit Vedic multiplier is derived from the Urdhva Tiryagbhyam sutra, a key principle of Vedic mathematics that performs multiplication using vertical and crosswise operations. Unlike conventional multipliers that generate and accumulate partial products sequentially, the Vedic approach computes them in parallel, significantly reducing the computational depth.

The 8-bit multiplier is built hierarchically to maintain structural regularity and simplify the physical design process. At the lowest level, a 2×2 Vedic multiplier forms the fundamental block, which is then expanded into a 4×4 multiplier by appropriately arranging four such units. The final 8×8 architecture is constructed by combining four 4×4 multipliers along with additional adders to aggregate vertical and crosswise products.

This hierarchical construction not only enhances modularity but also ensures that the layout remains uniform and predictable. Such regularity is beneficial during backend implementation because it minimizes routing congestion, reduces fan-out, and ensures shorter interconnect lengths. As a result, the design naturally lends itself to efficient placement and routing, making it more suitable for ASIC implementation than irregular or highly complex multiplier architectures.

B. RTL Design and Verification

The Register Transfer Level (RTL) description of the multiplier is written using Verilog HDL. At this level, the focus is on accurately expressing the logical flow of data and the hierarchical structure of the Vedic multiplier. Each block—from basic 2×2 elements to the final 8×8 module—is coded as an independent, reusable component.

To validate the correctness of the RTL description, a dedicated testbench is developed. It applies a wide set of input combinations to ensure correct functionality across the entire input range. Simulation waveforms are examined to check whether partial products propagate correctly, whether the final 16-bit output is accurate, and whether the circuit remains stable without glitches or hazards.

Particular attention is given to edge cases such as all-ones input patterns, alternating bit sequences, and scenarios that may trigger carry-propagation issues. This comprehensive verification ensures that the logical structure behaves as expected before proceeding to synthesis and physical design.

C. Logic Synthesis

The synthesized implementation is generated using Cadence Genus with a 90 nm standard-cell library. During synthesis, the RTL description is translated into a gate-level netlist composed of standard logic cells such as NANDs, XORs, multiplexers, and adders.

Timing, area, and power constraints are provided to guide the synthesis engine. Based on these constraints, the tool optimizes cell selection, adjusts drive strengths, and resolves critical paths to meet performance requirements. The synthesis tool also analyzes the logical depth of arithmetic operations, replaces inefficient logic structures, and balances the propagation delay across long paths.

After optimization, a complete gate-level netlist is produced. This netlist serves as the input for backend physical design and forms the reference for all further layout and verification stages.

D. Physical Design Flow

Once synthesis is completed, physical design is carried out using Cadence Innovus. The process begins with floorplanning, where the core area is allocated based on the estimated cell count. Macro placement, IO pin assignment, and power grid generation are also finalized during this stage to ensure optimal utilization of silicon area and even distribution of power.

The physical design was completed using Cadence Innovus following these steps:

- Floor planning: Defined core, IO placement, and power rings.
- Placement: Standard cells arranged with congestion-aware algorithms.
- Power Planning: VDD/VSS rails and straps constructed to avoid IR drop.
- Clock Tree Synthesis: Balanced H-tree built to reduce clock skew.
- Routing: Multi-layer routing performed; design was DRC- and LVS-clean.

Parasitic Extraction: SPEF generated for accurate delay and power estimation.

IV. RESULTS

A. Post-layout performance at 90nm

Parameter	Value
Standard Cells	230
Post-Layout Delay	5.82 ns
Total Power	92.6 µW
Dynamic Power	81.2 µW
Leakage Power	11.4 µW
Area	38 µm × 41 µm

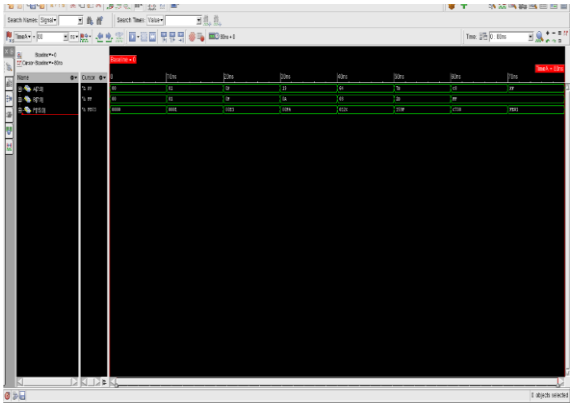
The results indicate that the 8-bit Vedic multiplier maps efficiently onto the 90 nm node, with favourable delay, power, and layout behaviour. This confirms that 90 nm remains well suited for compact, low-complexity arithmetic designs.

B. Comparison of 90nm with 45nm snd 180nm

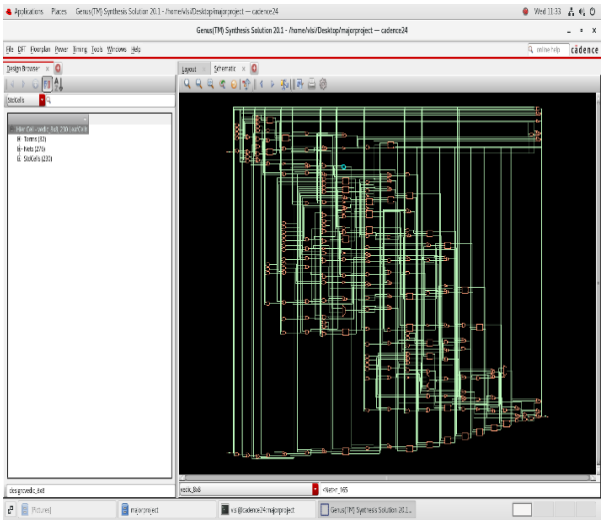
	180nm	90nm	45nm
Area [cell count]	247	230	272
Power [µW]	254	48.2	60.2
Delay [ps]	5438	3967	3490

The technology comparison demonstrates that the 90 nm implementation achieves a favorable balance among area, power, and delay when compared with the 180 nm and 45 nm nodes. The Vedic multiplier maps more efficiently in terms of cell utilization, while also exhibiting substantially improved power characteristics relative to both the older and more advanced technologies. Although 45 nm offers lower delay, it incurs higher design complexity and leakage overheads, whereas 180 nm suffers from larger area and slower operation. The 90 nm node therefore provides the most balanced operating point, offering efficient physical realization with stable timing and reduced power, making it well suited for compact arithmetic units in medium-performance VLSI systems.

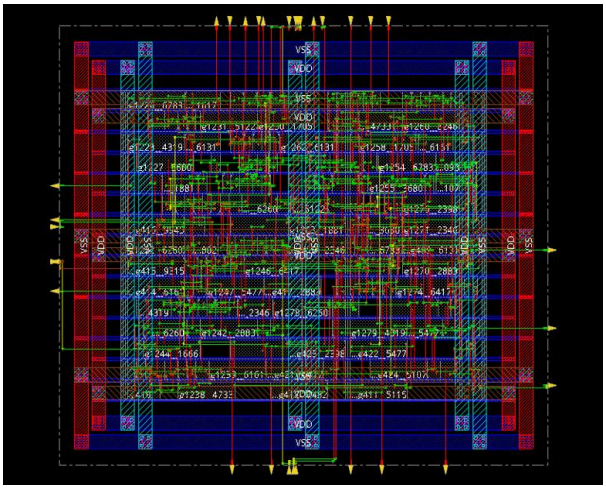
C. Simulation of 8-bit vedic multiplier using nc launch



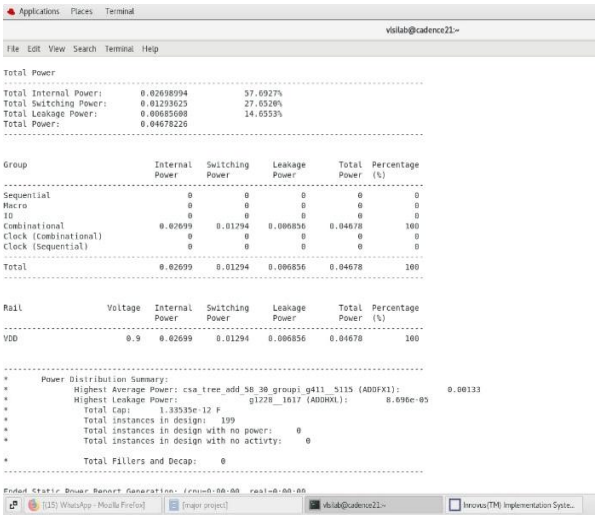
D. Synthesis of 8-bit vedic multiplier using genus



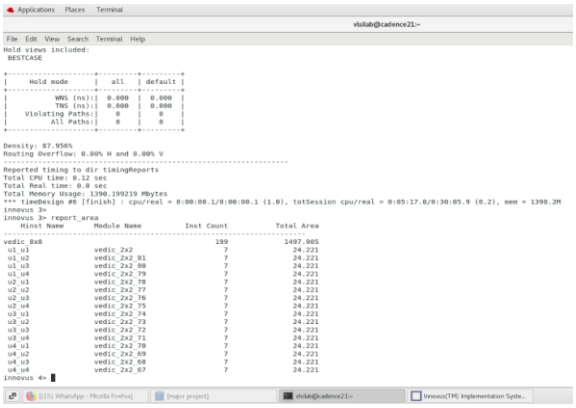
E. layout of 8-bit vedic multiplier using innovus



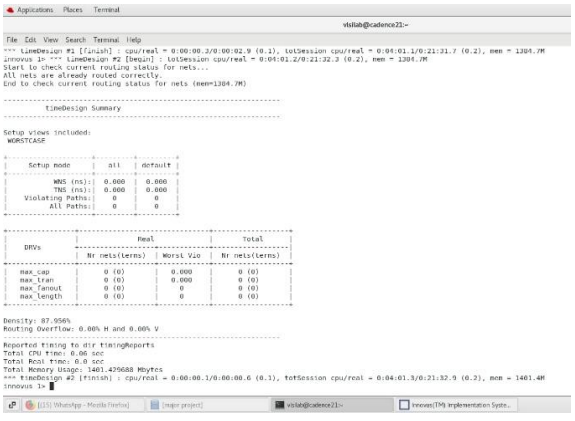
F. Power report of 32-bit vedic multiplier



G. Area report of 32-bit vedic multiplier



H. Timing report of 4bit conventional multiplier



VII. CONCLUSION

The 8-bit Vedic multiplier was implemented in 180nm, 90nm, and 45nm CMOS technologies. The 45nm design achieved the fastest delay (3490 ps) but consumed more power (60.2 µW) and used more cells, showing a clear trade-off between speed, power, and area in advanced nodes. This highlights the need for careful optimization when using smaller technologies.In future, the design can be improved using low-power techniques like clock gating or multi-threshold logic. It can also be extended for signed and floating-point operations, pipelined for higher throughput, and tested in ASIC implementations. Comparing it with other multipliers and integrating it into ALUs or accelerators can further enhance its practical usefulness.

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