Placement Of Logic Cells And Power Impact With Clock Cell Placement

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***Abstract*—Power optimization is a big challenge in the IC industry. Generally power dissipation come into two categories. One is Static power and other is Dynamic power. Here we focus more on Dynamic power dissipation, which is more dependent on clock network. Clocks do switch more frequently and drive much larger capacitances. Clock networks consume up to 40% of the total power. With register clustering we can reduce clock power. P*lacing registers in the same leaf cluster of the clock trees in a smaller area. With this, leaf-level wire capacitance of the clock tree is reduced. Finally, 'Net Switching Power' is reduced*.**

***Index Terms*—placement, clock tree synthesis, clock cell clustering, routing**

I. INTRODUCTION

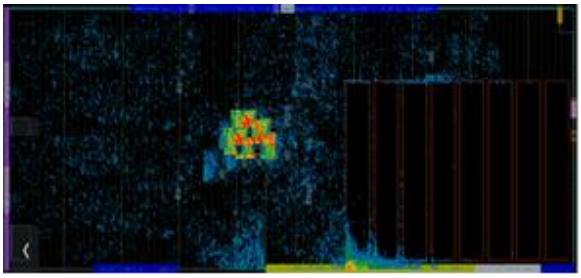
Net switching can be reduced by reducing the clock net routing capacitance. Net capacitance can be minimized by reducing the length of the wire. So finally clustering the clock cells will help in reducing power dissipation. But it will shoot up congestion issues. Here we further work on neutralizing the congestion issues by spreading the Leaf cells in a systematic manner by using cell padding methods. This will spread the module in a checker board manner. So, the pin density reduces, which open up more routing resources. Finally, power is improved with minimal congestion impact.

Cwire ≈ C per_unit_length X Length of Net

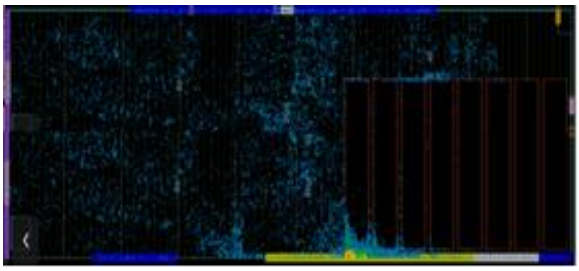
II. PLACEMENT OF DESIGN

Mapping a given module into the physical chip is called Placement. The key factors to consider while placement is Timing, Congestion, Power, Area. In complex designs, interconnect delay claims up to 60% of circuit delay. Hence, cells need to be correctly estimated and properly placed. Initially random placement is happened. During this stage cells are placed on the best possible locations Few overlaps can be accepted here. Then detailed placement happens, which includes exact cell position according to design rules. Congestion determines the routing possibility of a design. The congestion is related to the number of crossings between routed nets and global bin edges. If routing demand exceeds the routing supply. It leads to Overflow

Complexity increases day to day & area shrink causes congestion issues. Multiple options help to cut down the congestion .one is spreading the module across the tile, which opens more routing resources across the reason.



BEFORE CELL PADDING



AFTER CELL PADDING

III. CLOCK TREE SYNTHESIS

CTS is connecting the clock to each Leaf cell of the design by using Inverter/Buffers by maintaining the skew and Latency targets. As the clock network is more dominating in the design , need to use the possible top layers for the routing. To maintain uniform latency values , Buffers/Inverters are used to optimize the design. Synthesis is broadly categorized to two ways , one is Single point CTS . the other is Multi Point CTS. MPCTS is more efficient way to build the clock , by tapping the sinks to nearest clock root.

If the roots are increased , the latency & skew values are reduced which helps in timing. It helps in reducing the clock tree levels , which reduces timing issues.it uses useful skew methods to fix timing in efficient way with minimum impact.

IV. OPTIMIZATION

After placing the design , need to optimize the design with minimum congestion & better timing by meeting less area. Here tool used different methods like buffering , sizing a cell & moving the cell location to a better place. Optimization needs both for setup & hold timing fixes.

V. ROUTING

During CTS clock is routed. Now all the data paths need to be routed. Routing is mainly having two stages. The first one is global routing, where each data pin is connected. Then detail routing happens where each coordinate is laid. Routing mainly focus on cleaning shorts & DRC fixing. It also aims minimal signal integrity & power integrity. Tool also tries to route timing critical nest in top layers for minimal resistance & timing delays.

VI. OPTIMIZING CLOCK POWER

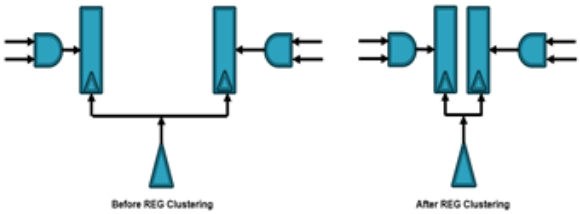
Grouping the registers which are under the same leaf cluster.

Net switching power is one of the largest sources of the total power dissipation.Net switching power can be reduced, if we reduce the Net Capacitance.

$$\text{Net switching power} = kCV^2\alpha$$

α : is the switching rate
C: is the total capacitance
V: is the supply voltage
k : is a constant,

Normally ,Clocks do switch more frequently and drive much larger capacitances. Clock networks consume up to 40% of the total power. With register clustering we can reduce clock power. *It means, placing registers in the same leaf cluster of the clock trees in a smaller area.* With this , leaf-level wire capacitance of the clock tree is reduced. Finally , depending on the previous equation, *'Net Switching Power'* is reduced. But it may increase the length of some signal nets as shown below. If required, we can assign a large weight to the signal nets with higher switching rates.

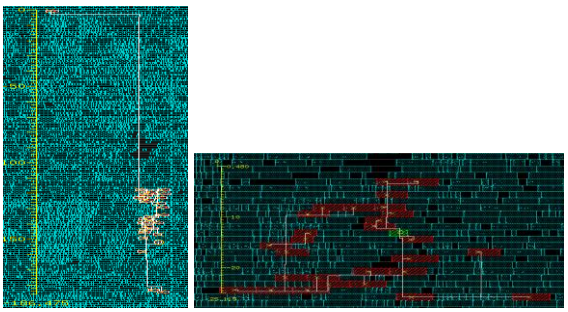


Because of register clustering , it is proven that the Net Length , Net Cap values and finally Net Switching power will be reduced abruptly. But the other impacts in terms of timing will depend on how we are clustering the registers.Normally timing will be degraded after register clustering. Up to some extent we can regain the timing with little area impact. At least this clustering can be implemented on non timing critical blocks to get advantage in terms of power

PATH WISE CLUSTERING

Implemented Reg-Clustering on Path wise.

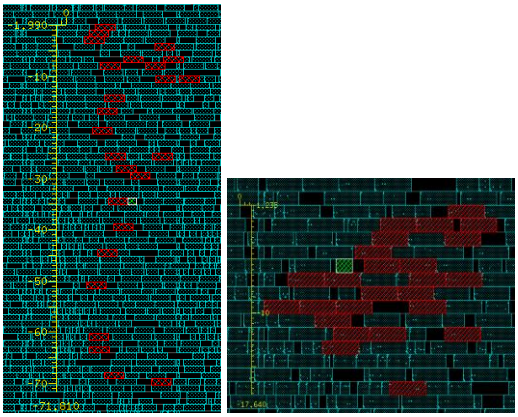
PATH 1



BEFORE CLUSTER AFTER CLUSTER

	Before	After	%Benefit
Wire Length	282Mic	127Mic	55%
Cap	49PF	32PF	33%
Pwr(Sw)	8.65	5.93	31.4%

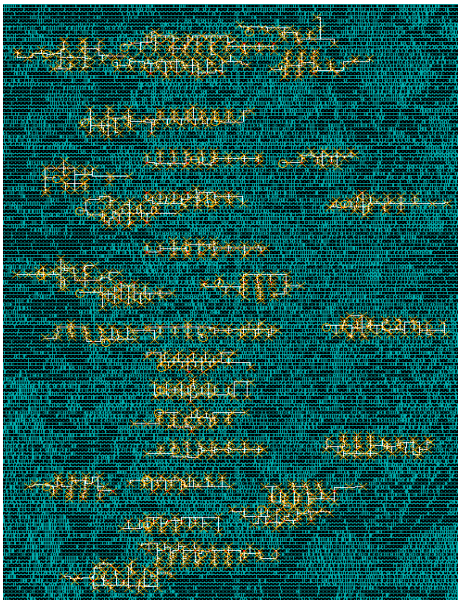
PATH 2



	Before	After	%Benefit
WL	149Mic	89Mic	41%
Cap	31PF	24PF	23%
Pwr(Sw)	5.15	3.93	23.6%

MODULE WISE CLUSTERING

Implementing register clustering on modules .Analyzing the impact of clustering on module is a little bit diffu=icult compared to the nets. Science in a module , for some paths we get advantange in terms of power But might be nullified by some othger path in the same module



	Before	After
Net Switching Power	8.46 mic W	8.23 mic W

VII. CONCLUSIONS

Because of Register Clustering Net Length , Cap value and Net Switching Power is reduced one by one respectively. These below values are calculated based on Net based clustering.

Wire length is reduced by : 25%
Cap value is reduced by : 11%
Power is reduced by : 6%
(with Net wise clustering)
Power is reduced by : 2%
(with Module wise clustering)

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