

Design and Implementation of Totem-pole Power Factor Correction (PFC)

Prof. Rajendra Sawant¹, Harshal Bhalerkar², Meetesh Bhandarkar³, Aarya Jogalekar⁴
*Dept of Electronic and Telecommunication Engineering, Bharatiya Vidya Bhavans Sardar Patel
Insititue of Technology Mumbai 400053, India*

Abstract— Modern electronic systems require advanced power conversion technologies that offer high efficiency, compact design, and superior power quality. Power Factor Correction (PFC) circuits are essential in meeting these demands, optimizing energy transfer between AC and DC power systems. This research introduces an advanced totem-pole PFC topology that redefines traditional power conversion by eliminating complex diode bridge rectifiers, significantly reducing energy losses, and boosting system performance. Utilizing wide-bandgap semiconductor technologies like Silicon Carbide (SiC) and Gallium Nitride (GaN), the design achieves remarkable efficiency. It operates in boost mode during positive AC half-cycles and inverted boost mode during negative cycles, ensuring continuous, unidirectional energy transfer with minimal losses. This approach maintains near-unity power factor and lowers harmonic distortion. Experimental validation shows a power factor over 0.99, efficiency nearing 98%, and stable voltage regulation under various loads. A dual-loop control system, featuring voltage and current loops with a PI controller, adjusts PWM signals for precise current shaping and voltage stability. This technology has potential applications in areas like server power supplies, EV charging, renewable energy systems, high-performance computing, and industrial motor drives, showcasing the potential of totem-pole PFC in modern power electronics.

Keywords— SiC - Silicon Carbide, GaN - Gallium Nitride.

I. INTRODUCTION

AC-to-DC power supplies are integral to modern electronics, requiring high efficiency and compliance with stringent power quality standards. Power Factor Correction (PFC) circuits play a critical role in achieving these goals by aligning the current drawn from the AC source with the input voltage. Power factor, the ratio of real power (watts) to apparent power, indicates the efficiency of energy transfer. An ideal power factor of 1 signifies

minimal losses from reactive power, ensuring all supplied energy is effectively utilized. PFC achieves this by compensating lagging currents with leading currents, reducing energy waste and improving system performance. The boost converter is the most common topology used for PFC. It rectifies AC input through a diode bridge before boosting it to the required DC voltage. However, this approach has significant drawbacks. The diode bridge introduces conduction losses due to its forward voltage drop, particularly at higher currents. Additionally, reverse recovery currents during switching generate heat and energy losses, reducing efficiency. The totem-pole PFC topology addresses these issues by eliminating the diode bridge [1]. It features a series inductor with two legs: a high-frequency leg using fast-switching transistors and a low-frequency leg typically composed of diodes. This design minimizes conduction losses, resulting in significantly improved efficiency. Advancements in PFC technology have been driven by wide-bandgap semiconductors like Silicon Carbide (SiC) and Gallium Nitride (GaN) [1]. These materials offer low on-state resistance, reducing heat loss, and exhibit minimal reverse recovery, eliminating current spikes and electromagnetic interference (EMI) [5]. SiC and GaN devices are ideal for high-frequency switching, ensuring stable and efficient performance, even at the zero-crossing point of the AC input. By integrating SiC and GaN into totem-pole PFC designs, modern power supplies achieve compactness, reliability, and unparalleled efficiency, meeting the demands of cutting-edge applications.

II. CONVENTIONAL POWER FACTOR CORRECTION (PFC)

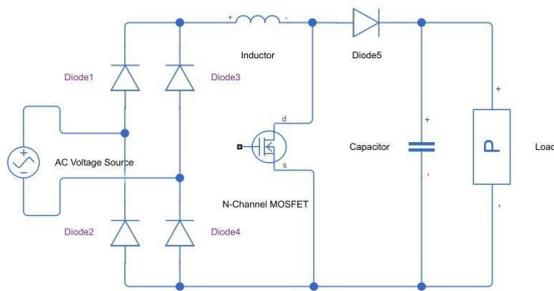


Figure 1: Conventional Power Factor Correction (PFC) circuits diagram.

Conventional Power Factor Correction (PFC) circuits are widely used in electrical power systems to improve energy efficiency and comply with power quality standards. These systems typically employ a diode bridge rectifier to convert AC input into DC bus voltage, followed by passive or active PFC techniques. While straightforward and cost-effective, conventional PFC methods face several drawbacks that limit their efficiency and performance [7].

The diode bridge rectifier introduces significant conduction losses due to the forward voltage drop across the diodes, reducing overall system efficiency. Additionally, reverse recovery currents during switching transitions lead to further energy losses in diodes and associated semiconductors, particularly under light load conditions [3]. This reduces performance and generates substantial heat, necessitating advanced cooling mechanisms. Moreover, harmonic distortion in the input current caused by the diode bridge requires additional filtering to meet power quality standards.

Traditional PFC techniques also suffer from hardware complexity, involving components like inductors, capacitors, and switching elements, which increase production costs and design intricacy. These methods often struggle to maintain voltage regulation under dynamic load conditions and exhibit limited frequency response, potentially compromising reliability. Addressing these limitations demands advanced PFC strategies with enhanced efficiency, reduced complexity, and better performance, particularly for modern, cost-sensitive applications.

III. TOTEM-POLE POWER FACTOR CORRECTION (PFC)

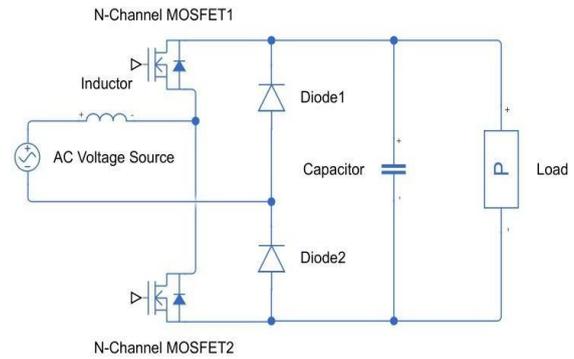


Figure 2: Totem-pole Power Factor Correction (PFC) circuits diagram.

The totem-pole power factor correction (PFC) topology offers a modern solution that improves on conventional PFC designs by reducing component count and minimizing conduction losses. Unlike traditional PFC circuits, which position the inductor on the DC side, the totem-pole PFC places the inductor on the AC side. This reduces the number of components conducting at any given time, enhancing overall efficiency.

The totem-pole PFC features two legs: a high-frequency leg with active semiconductor switches (such as silicon MOSFETs, SiC, or GaN) and a low-frequency leg with slower components like diodes. SiC and GaN devices are favoured because they exhibit negligible reverse recovery, reducing current spikes during switching and improving efficiency, especially at the zero-crossing point of the input voltage. This configuration reduces switching and conduction losses, improving efficiency compared to conventional designs that may require multiple components to conduct simultaneously [10].

The totem-pole PFC operates in two modes: boost mode during the positive half-cycle of the AC input and inverted boost mode during the negative half-cycle. In boost mode, high-frequency switches store energy in the inductor, and low-frequency diodes transfer energy to the output. In inverted boost mode, the roles of the switches and diodes reverse to maintain unidirectional current flow. This bidirectional power flow ensures efficient operation throughout both AC half-cycles, reducing power losses.

The key advantages of the totem-pole PFC include enhanced power density, reduced component count, and improved inductor utilization. The use of a single inductor for both half-cycles increase

efficiency by eliminating extra components. The design is compact, making it ideal for space-constrained applications such as server power supplies, electric vehicle chargers, and high-power systems.

In addition, the totem-pole PFC ensures excellent power quality by achieving near-unity power factor and minimizing harmonic distortion [6]. This is essential for meeting power quality standards, particularly in renewable energy inverters and industrial motor drives.

The design's performance is further optimized by the use of wide-bandgap semiconductors, which provide superior switching characteristics and higher temperature tolerance compared to silicon MOSFETs [9]. These devices enable higher switching frequencies, reducing switching losses and enhancing efficiency, particularly in high-power applications.

In conclusion, the totem-pole PFC topology represents a significant advancement in power factor correction technology, offering improved efficiency, compactness, and power density. The use of wide-bandgap semiconductors, along with the strategic inductor placement, makes it an ideal solution for modern power conversion systems that require high performance and reliability.

TABLE 1: DESIGN PARAMETERS.

Input Voltage	85 – 265 V
Output Voltage	400 V
Rated Power	2.5 kW
Line Frequency	50 Hz
Switching Frequency	40 kHz
Ripple Current	30% (0.3)
Ripple Voltage	1% (0.01)

IV. POWER CIRCUIT OF TOTEM-POLE PFC ON MATLAB

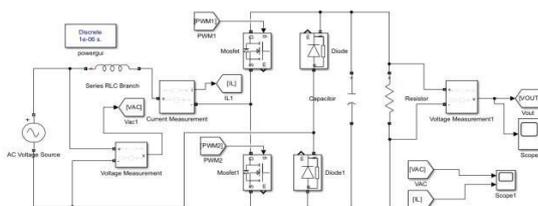


Figure 3: Power circuit of Totem-pole PFC on MATLAB. The diagram depicts a Bridgeless Totem-Pole Power Factor

Correction (PFC) Converter, a modern circuit design focused on improving efficiency in AC to DC power conversion. This setup

eliminates the need for a traditional diode bridge rectifier, reducing conduction losses and enhancing overall efficiency.

I. AC Input and RLC Filtering

The circuit starts with an AC Voltage Source that provides 230V RMS at 50Hz. This AC input is fed through a series RLC branch containing an inductor, which is crucial for current shaping and harmonic suppression. The inductor helps maintain a smooth current flow, reducing unwanted harmonics and improving the power factor by ensuring that the input current closely follows the input voltage waveform. Voltage and current sensors are connected to the AC side for monitoring and feedback.

II. Totem-Pole Topology

The core of the circuit is the totem-pole structure, which utilizes two active MOSFETs and two diodes arranged in a complementary half-bridge configuration. This structure allows efficient AC-DC conversion without the need for a conventional diode bridge. In the positive half-cycle of the AC input, the second MOSFET (labelled as Mosfet2) switches on, using a control- defined duty cycle to charge the inductor with energy. During the off period of Mosfet2, the first MOSFET (Mosfet1) switches on, discharging the energy stored in the inductor to the DC bus, which charges the capacitor.

In the negative half-cycle, the switching roles of the MOSFETs are reversed. Mosfet1 handles the charging of the inductor, while Mosfet2 discharges it into the DC bus. This alternating switching pattern ensures that the AC power is efficiently converted to DC, with the energy flowing unidirectionally towards the output load.

III. Measurement and Control

The diagram includes voltage and current measurement blocks for real-time monitoring. These measurements are crucial for the feedback loop that controls the circuit's operation. A PWM (Pulse Width Modulation) Controller generates high-frequency switching signals that adjust the duty cycles of the MOSFETs. This modulation is based on the feedback from voltage and current

measurements, ensuring that the inductor is charged and discharged optimally during each AC half-cycle. Additionally, a polarity detection mechanism is included to ensure the correct MOSFETs operate during the positive and negative half-cycles, preventing any reverse current.

IV. Output Stage

The DC output is delivered across a capacitor, which smoothens the converted voltage, ensuring stable DC output. A resistor is included in the output stage for load simulation, and the output voltage is monitored by a voltage measurement block. This allows real-time observation of the output characteristics, essential for assessing the circuit's performance and ensuring it meets desired power quality standards.

In summary, the diagram showcases a highly efficient and modern Bridgeless Totem-Pole PFC circuit with advanced control techniques for efficient AC-DC conversion. This topology is favoured for its ability to provide a near-sinusoidal input current, high power factor, and reduced harmonic distortion, making it a popular choice for applications demanding high efficiency and power quality.

V. CLOSED-LOOP CONTROL OF TOTEM-POLE PFC CONVERTER ON MATLAB

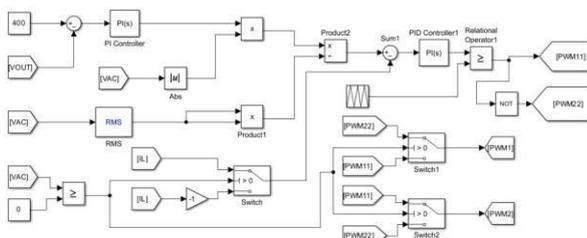


Figure 4: Closed-loop control of Totem-pole PFC converter on MATLAB.

The circuit diagram represents the closed-loop control system for a Totem-Pole Power Factor Correction (PFC) converter. This design employs two key control loops: a voltage control loop and a current control loop, along with a polarity detection mechanism to handle the alternating cycles of the AC input. Each component of the circuit plays a crucial role in ensuring efficient and accurate power factor correction.

I. Voltage Control Loop

The voltage control loop in the diagram is

responsible for regulating the output voltage (V_{out}) to a target reference, typically 400V. This is achieved by comparing the actual output voltage with the desired voltage reference using a summing block, which generates an error signal. The error is then processed through a Proportional-Integral (PI) Controller, which is highlighted in the upper part of the circuit. The PI controller's parameters include a proportional gain ($K_P=2$) and an integral gain ($K_I=50$), ensuring stability and fast response to any voltage fluctuations. The controller's output modifies the PWM duty cycle, ensuring that the output voltage remains steady despite load changes or input voltage variations.

II. Current Control Loop

The current control loop, shown in the lower part of the diagram, is crucial for shaping the inductor current (I_L) to follow a sinusoidal reference. This reference is based on the input AC voltage (V_{ac}), ensuring high power factor and low harmonic distortion. The AC voltage's RMS (Root Mean Square) value is calculated and used to generate a reference for the inductor current. The difference between the actual inductor current and this reference creates an error signal, which is processed by a second PI Controller [12]. In the diagram, this controller is configured with a proportional gain ($K_p=10$) and an integral gain ($K_i=0.5$), providing precise control of the current loop. The loop's output adjusts the PWM signals to correct the current in real-time.

III. Polarity Detection and Switching Logic

The circuit diagram includes a polarity detection mechanism to manage both the positive and negative half-cycles of the AC input. A comparator block checks whether the AC input voltage (V_{ac}) is above zero, determining the polarity of the input. Depending on the result, the control system adjusts the switching of the MOSFETs accordingly. This ensures proper conduction in the appropriate MOSFETs for each half-cycle. In the diagram, switching blocks are used to control the current's direction, toggling between positive and negative paths as needed. Logical operations coordinate the sequence to maintain continuous conduction mode (CCM) and align the input current with the AC voltage phase.

IV. PWM Signal Generation

In the diagram, Pulse Width Modulation (PWM)

signals are generated by comparing the current loop's output to a high-frequency triangular waveform. This comparison produces PWM signals that control the gate drivers of the MOSFETs, which are responsible for switching operations. Specific PWM blocks, such as PWM11 and PWM22, generate complementary signals to manage the MOSFETs' alternating operation efficiently. Logical and switching elements ensure that complementary switches do not conduct simultaneously, minimizing switching losses and optimizing efficiency.

V. Control System Design and Simulation

The control system shown in the diagram is modular, allowing easy adjustments and scalability to different power ratings. The simulation environment uses a fixed-step solver with a fine time resolution to accurately simulate the converter's behaviour. Key parameters, such as V_{out} , V_{ac} and I_L , are continuously monitored within the system to validate performance and ensure stable operation under varying conditions.

VI. Performance Metrics

The dual-loop control architecture represented in the diagram enables the Totem-Pole PFC converter to achieve a power factor greater than 0.99 [8], aligning input current with the AC voltage and reducing harmonic distortion. The configuration maintains efficiency levels above 98%, making it suitable for applications that demand high-quality AC-DC conversion with minimal energy losses.

VI. OUTPUT

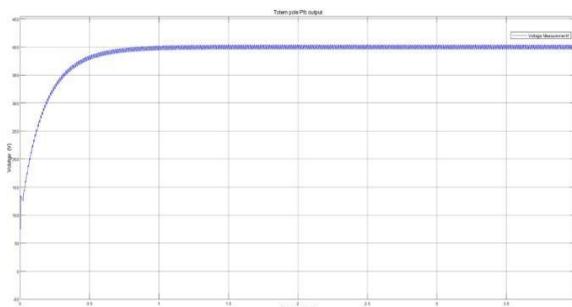


Figure 4

Figure 4: The plot shows the regulated output voltage waveform of the Totem-Pole PFC converter under closed-loop operation. The output voltage is maintained at a steady 400V DC, as indicated by the horizontal yellow line. During startup, a rapid transient response is observed as the voltage

quickly stabilizes at the desired reference level, showcasing the effectiveness of the voltage control loop. This loop, incorporating a PI (proportional-integral) controller, ensures minimal steady-state error and precise voltage regulation. The fast response and reliable regulation are essential for delivering stable power to the connected load, even with variations in input voltage or load demand.

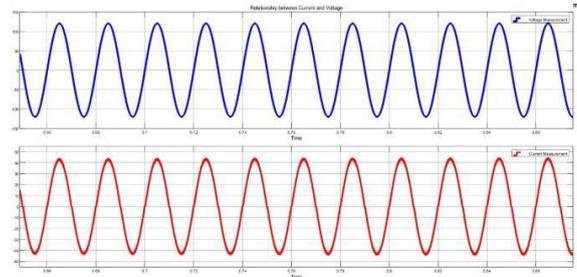


Figure 6

Figure 5: This figure illustrates the AC input voltage (yellow) and current (blue) waveforms of the Totem-Pole PFC converter. The sinusoidal input current, which is in phase with the input voltage, demonstrates the near-unity power factor achieved by the system. Such performance ensures efficient energy transfer from the AC grid to the DC output, with reduced reactive power and harmonic distortion. The current loop control, equipped with a PI controller, dynamically regulates the inductor current to maintain synchronization between the input voltage and current, even under varying load conditions. The smooth sinusoidal input current validates the converter's ability to meet stringent power quality standards.

The combined results of output voltage regulation and high-power-factor correction underscore the effectiveness of the Totem-Pole PFC control scheme. This enables the converter to meet the demanding requirements of modern applications such as server power supplies, electric vehicle chargers, and renewable energy systems. The modular design of the control system also supports its implementation on standard microcontroller or DSP platforms, making it a practical and cost-efficient solution for high-efficiency AC-DC conversion in a variety of applications.

VII. CONCLUSION

The totem-pole Power Factor Correction (PFC) topology represents a groundbreaking approach to

power conversion technology, offering significant improvements over conventional PFC designs. By strategically eliminating traditional diode bridge rectifiers and leveraging wide-bandgap semiconductor technologies, this innovative topology achieves unprecedented levels of efficiency, power density, and performance.

Key advancements of the totem-pole PFC include:

1. **Enhanced Power Conversion Efficiency:** The elimination of multiple conduction stages and integration of advanced semiconductor devices like SiC and GaN enable near-98% energy transfer efficiency.
 2. **Compact Design Architecture:** Reduced component count and strategic inductor placement facilitate smaller, more integrated power conversion systems suitable for space-constrained applications.
 3. **Superior Power Quality:** The topology ensures near-unity power factor and minimizes harmonic distortion, meeting stringent power quality standards across diverse industrial and consumer electronics domains [13].
- Future research directions should focus on further optimizing semiconductor device characteristics, developing advanced control algorithms, and exploring potential applications in emerging fields such as renewable energy systems, electric vehicle infrastructure, and high-performance computing power supplies. The presented closed-loop control methodology demonstrates the topology's potential to deliver stable, responsive power conversion with remarkable precision, positioning totem-pole PFC as a transformative technology in power electronics engineering.

VIII. ACKNOWLEDGMENT

The authors would like to take this opportunity to extend their heartfelt gratitude to everyone who contributed their support to this project. Their efforts have played a significant role in the successful completion of this work. We would also like to express our sincere thanks to the Electronics and Telecommunications Engineering Department of Sardar Patel Institute of Technology for providing us with the necessary resources.

REFERENCES

- [1] R. Singh, "Wide Bandgap Semiconductor Devices: An Overview," *IEEE Transactions on*

Electron Devices, vol. 62, no. 1, pp. 62-74, Jan. 2015.

- [2] B. Su, J. Zhang, and Z. Lu, "Totem-Pole Bridgeless PFC Implementation Using GaN HEMTs," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4513-4523, Sep. 2014.
- [3] K. M. Smith and K. I. Hwu, "A Review of Bridgeless PFC Topologies for High-Efficiency Power Conversion," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 1178-1192, June 2018.
- [4] Y. Yang, P. C. Loh, and F. Blaabjerg, "Advanced Control of Totem-Pole PFC Converters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 3108-3119, April 2017.
- [5] A. Huang, "GaN and SiC Power Devices: An Overview of Development and Applications," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2019- 2031, Nov. 2017.
- [6] IEEE Standards Coordinating Committee, "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," *IEEE Std 519-2014*, pp. 1-29, June 2014.
- [7] M. de Brito, L. Galotto, L. Poltronieri, and P. G. de Melo, "Evaluation of the Main Topologies for Three-Phase Rectifier with
- [8] Power Factor Correction," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4667-4678, Sep. 2014.
- [9] J. W. Kolar, U. Badstuebner, and Y. Sheng, "Development and Experimental Verification of a Simple, Non-Linear DC-Link Voltage Control Scheme for Universal Mains Interface," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 4, pp. 294-304, Dec. 2013.
- [10] B. Lu, W. Liu, Y. Liang, and F. C. Lee, "Optimal Design of GaN-Based MHz Totem-Pole PFC Rectifier," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11545-11556, Oct. 2021.
- [11] X. Huang, Z. Liu, and Z. J. Shen, "Bridgeless Boost PFC Converter with Reduced Conduction Losses," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5811-5819, July 2018.
- [12] F. Musavi, M. Edpuganti, and W. Eberle, "A Comparative Study of Soft-Switching

Techniques in Single-Phase Power Factor Correction Converters," IEEE Transactions on Power Electronics, vol. 32, no. 1, pp. 42-55, Jan. 2017.

- [13] R. Leyva, C. Roncero-Clemente, and E. Vázquez, "A Modified Predictive Current Controller for Power Factor Correction in Three-Phase Systems," IEEE Transactions on Industrial Electronics, vol. 66, no. 3, pp. 2176-2185, March 2019.
- [14] S. Wang, F. Xue, and W. Liu, "High-Efficiency SiC-Based Totem-Pole PFC Rectifier Design and Performance Evaluation," IEEE Transactions on Power Electronics, vol. 35, no. 12, pp. 13245-13256, Dec. 2020.