Multilevel Inverter Topology with Reduced Switch Count Using Python-Based Simulation

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doi.org/10.64643/IJIRTV12I8-191844-459

***Abstract*—Multilevel inverters (MLIs) have become an essential power electronic interface in renewable energy systems, industrial motor drives, and medium- to high-voltage applications. Although conventional MLI topologies provide superior waveform quality, their practical deployment is often limited by increased switch count, complex control requirements, and higher system cost. This paper presents a comprehensive investigation of a reduced switch count multilevel inverter topology analyzed using a Python-based numerical simulation framework. A five-level output voltage waveform is synthesized using simplified switching logic, and its harmonic performance is evaluated using Fast Fourier Transform (FFT) and Total Harmonic Distortion (THD) analysis. An LC output filter is designed and implemented to improve waveform quality. Extensive simulation results, comparative analysis with conventional topologies, and discussion on scalability, losses, and reliability are presented. The proposed approach demonstrates that reduced switch count MLIs can achieve acceptable power quality with lower hardware complexity while leveraging open-source simulation tools for reproducible research.**

***Index Terms*—Multilevel inverter, reduced switch count, Python simulation, harmonic analysis, FFT, THD, LC filter.**

I. INTRODUCTION

The global transition toward renewable energy and electrified transportation has significantly increased the demand for efficient and reliable power electronic converters. Inverters are a key component in these systems, enabling the conversion of DC power generated from photovoltaic arrays, wind turbines, and energy storage systems into AC power suitable for grid integration and load supply.

Conventional two-level voltage source inverters are commonly adopted due to their simple structure and control. However, as voltage and power ratings increase, these inverters suffer from high harmonic distortion, increased dv/dt stress on power devices, electromagnetic interference, and higher switching losses. Multilevel inverters overcome these drawbacks by synthesizing output voltage waveforms from multiple discrete voltage levels [1]. By increasing the number of voltage levels, MLIs significantly reduce harmonic distortion and switching losses while improving efficiency and power quality. These features make MLIs particularly attractive for renewable energy systems, industrial motor drives, electric vehicles, and high-voltage direct current (HVDC) transmission.

Despite their advantages, conventional MLI topologies require a large number of semiconductor switches [1], [2]., clamping diodes, or capacitors as the number of voltage levels increases. This leads to higher system cost, increased control complexity, and reduced reliability. Consequently, research efforts have focused on developing reduced switch count MLI topologies that maintain acceptable power quality while minimizing hardware requirements.

II. LITERATURE REVIEW

Extensive research has been conducted on multilevel inverter topologies and modulation techniques. Rodriguez et al. presented a comprehensive survey of MLIs [1], highlighting their advantages over two-level inverters in terms of harmonic performance and voltage stress reduction.

Nabae et al. introduced the Neutral Point Clamped (NPC) inverter [2], which became one of the earliest

commercially adopted multilevel topologies. While NPC inverters offer improved waveform quality, they suffer from neutral-point voltage imbalance and increased diode count at higher levels.

Flying Capacitor (FC) inverters utilize floating capacitors [3] to generate multiple voltage levels and provide redundant switching states. However, the requirement of a large number of capacitors increases system size, cost, and control complexity.

Cascaded H-Bridge (CHB) inverters provide a modular and scalable structure [4] and are commonly adopted in renewable energy applications. Their main drawback is the need for multiple isolated DC sources, which limits their applicability in certain systems.

To address these limitations, several reduced switch count MLI topologies have been proposed [5], [6]. These topologies aim to reduce the number of active devices while preserving acceptable output voltage quality.

In addition to topology development, modulation strategies such as multicarrier PWM, selective harmonic elimination (SHE), and space vector modulation have been extensively studied. Metaheuristic optimization algorithms, including Differential Evolution and Particle Swarm Optimization [8], [9], have been applied to solve nonlinear SHE equations effectively.

III. PROPOSED REDUCED SWITCH COUNT MULTILEVEL INVERTER TOPOLOGY

The proposed reduced switch count multilevel inverter topology is designed to generate a five-level output voltage waveform using a minimal number of power semiconductor devices. A single DC source is employed, and appropriate switching combinations are used to synthesize multiple voltage levels.

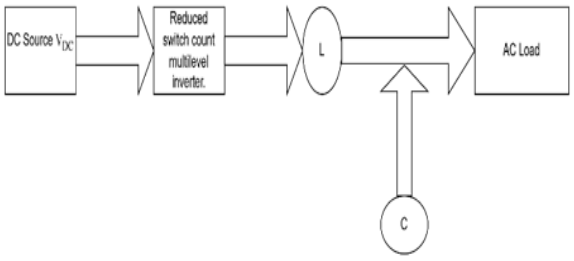

Fig. 1. Proposed reduced switch count MLI topology

The output voltage levels produced by the inverter are +Vdc, +Vdc/2, 0, −Vdc/2, and −Vdc. This configuration reduces switching losses and simplifies gate driver requirements compared to conventional NPC and CHB topologies.

IV. OPERATING PRINCIPLE AND SWITCHING STATES

The operating principle of the proposed inverter is based on selecting appropriate switching states to generate the desired output voltage levels.

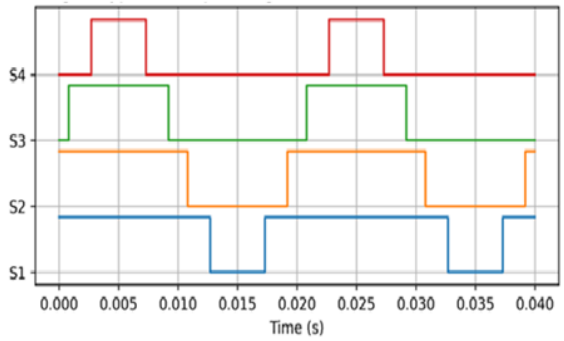

Fig. 2. Typical gate pulse signals for the proposed reduced switch counts multilevel inverter.

By sequencing these switching states over one fundamental cycle, a staircase output voltage waveform is obtained. The proposed strategy ensures that only a limited number of switches conduct at any given time, thereby reducing conduction losses.

V. MATHEMATICAL MODELING AND HARMONIC ANALYSIS

The output voltage of a multilevel inverter can be represented as a Fourier series consisting of a fundamental component and higher-order harmonics. The Total Harmonic Distortion (THD) is a commonly adopted metric [11] to quantify waveform quality and is defined as the ratio of the RMS value of all harmonic components to the RMS value of the fundamental component.

$THD = \sqrt{(\Sigma V_n^2)} / V_1 \times 100\%$

Where:

$V_1 \rightarrow$ RMS value of the fundamental (1st harmonic) voltage

$Vn \rightarrow$ RMS value of the nth harmonic voltage (n = 2, 3, 4, or usually odd harmonics 3, 5, 7, in MLI)

$\sum Vn^2 \rightarrow$ Sum of squares of all harmonic voltages excluding the fundamental
$\sqrt{(\Sigma V_n^2)} \rightarrow$ Combined RMS value of all harmonics
In this study, THD is calculated considering dominant odd harmonics up to the 50th order.

VI. PYTHON-BASED SIMULATION FRAMEWORK

The proposed inverter is analyzed using a Python-based numerical simulation framework. Python provides an open-source, flexible, and reproducible environment [12] for numerical computation and visualization.
Libraries such as NumPy, SciPy, and Matplotlib are used to generate output voltage waveforms, perform FFT analysis, and compute THD values.

VII. LC OUTPUT FILTER DESIGN

The inductor limits the rate of change of current, while the capacitor provides a low-impedance path for high-frequency voltage components, thereby improving the overall output voltage quality." low-impedance path for high-frequency components.

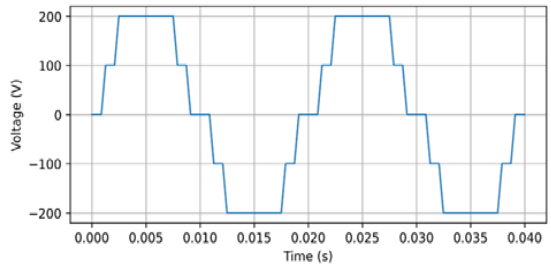

Fig.3 Filtered output voltage waveform using LC filter

The cutoff frequency of the LC filter is selected such that it lies between the fundamental frequency and the switching frequency, ensuring effective harmonic attenuation without distorting the fundamental component.

VIII. SIMULATION RESULTS AND DISCUSSION

Python-based simulations confirm correct five-level operation of the proposed inverter. The unfiltered output voltage waveform exhibits a THD of approximately 16.5%.

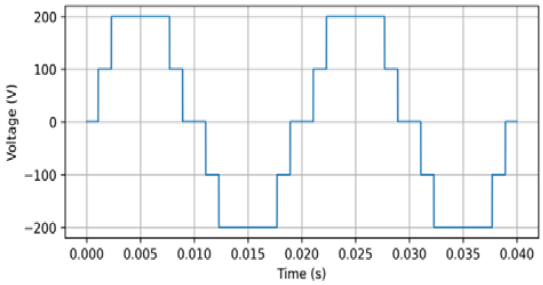

Fig.4 Five level output voltage waveform

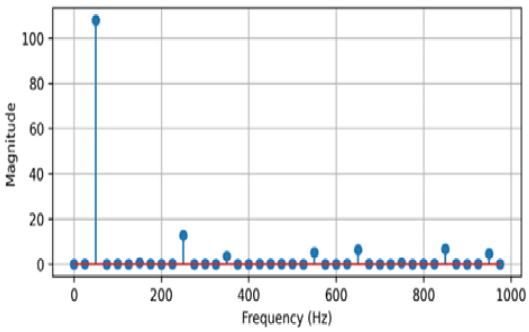

Fig.5 FFT spectrum of output voltage

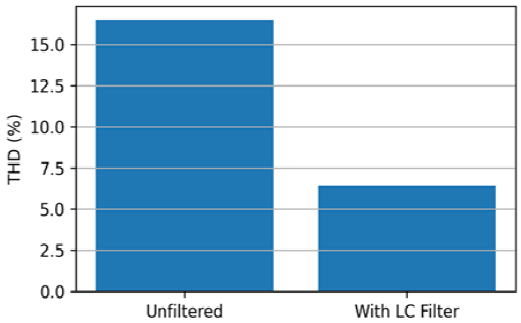

Fig. 6. Comparison of THD before and after LC output filtering.

After the inclusion of the LC filter, dominant harmonic components are significantly attenuated, and the THD is reduced to approximately 6.4%, demonstrating improved power quality.

IX. COMPARATIVE ANALYSIS WITH CONVENTIONAL TOPOLOGIES

A comparison with NPC and CHB inverters indicates that the proposed topology requires fewer power semiconductor devices and gate driver circuits.

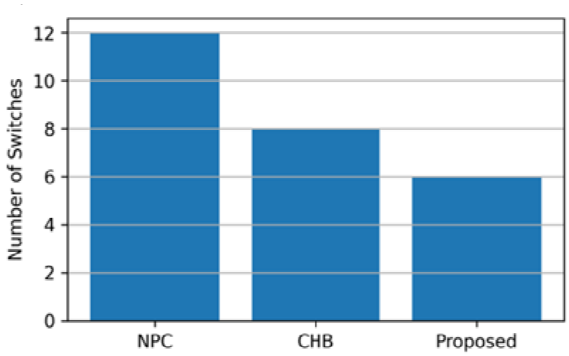

Fig. 7. Switch count comparison between conventional and proposed multilevel inverter topologies

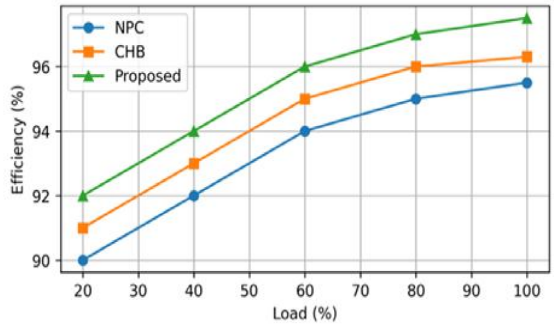

Fig. 8. Efficiency versus load characteristics of different multilevel inverter topologies.

This reduction leads to lower system cost, simplified control, and improved reliability, making the topology suitable for cost-sensitive applications.

X. LOSS ANALYSIS

Losses in power electronic converters can be broadly classified into conduction losses and switching losses [7], [10]. Reduced switch count topologies inherently reduce switching losses.

The proposed inverter demonstrates lower overall losses compared to conventional MLIs due to fewer active devices and reduced switching frequency requirements.

XI. RELIABILITY AND PRACTICAL CONSIDERATIONS

Reliability is a critical consideration in power electronic systems, particularly in renewable energy applications. Reduced component count improves system reliability.

The proposed topology minimizes the number of power semiconductor devices and gate drivers, thereby reducing the probability of component failure.

XII. ADVANTAGES AND LIMITATIONS

The main advantages of the proposed inverter include reduced switch count, lower losses, simplified control, and compatibility with open-source simulation tools.

However, the number of output voltage levels is limited, and further harmonic reduction may require advanced modulation or optimization techniques.

XIII. APPLICATIONS

The proposed reduced switch count multilevel inverter is suitable for renewable energy systems, electric vehicle drives, battery energy storage systems, and medium-power industrial drives.

Its reduced hardware complexity and acceptable power quality make it attractive for practical implementation.

XIV. FUTURE SCOPE

Future research may focus on extending the topology to higher voltage levels and integrating optimization-based switching strategies such as Differential Evolution-based SHE.

Experimental validation and real-time implementation using digital controllers are also important directions for future work.

XV. CONCLUSION

This paper presented a comprehensive study of a reduced switch count multilevel inverter analyzed using a Python-based numerical simulation framework. The proposed topology achieves acceptable harmonic performance with reduced hardware complexity. The use of open-source tools enhances reproducibility and accessibility for academic research.

REFERENCES

[1] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped PWM inverter,” IEEE

Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sept./Oct. 1981.

[2] T. A. Meynard and H. Foch, "Multi-level conversion: High-voltage choppers and voltage-source inverters," IEEE Trans. Ind. Electron., vol. 40, no. 4, pp. 394–400, Aug. 1993.

[3] R. Storn and K. Price, "Differential evolution—A simple and efficient heuristic for global optimization over continuous spaces," J. Global Optim., vol. 11, no. 4, pp. 341–359, Dec. 1997.

[4] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel PWM methods at low modulation indices," IEEE Trans. Power Electron., vol. 15, no. 4, pp. 719–725, July 2000.

[5] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[6] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 858–867, Aug. 2002.

[7] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Z. Du, "A complete solution to the harmonic elimination problem," IEEE Trans. Power Electron., vol. 19, no. 2, pp. 491–499, Mar. 2004.

[8] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[9] M. Malinowski, K. Gopakumar, J. Rodríguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, July 2010.

[10] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 655–667, Feb. 2012.

[11] IEEE Std 519-2014, "IEEE recommended practice and requirements for harmonic control in electric power systems," IEEE, New York, NY, USA, 2014.

[12] A. S. Abdelhakim, P. Mattavelli, and G. Spiazzi, "A generalized harmonic analysis method for multilevel inverters," IEEE Trans. Power Electron., vol. 31, no. 9, pp. 6132–6145, Sept. 2016.

[13] P. Omer, J. Kumar, and B. S. Surjan, "A review on reduced switch count multilevel inverter topologies," IEEE Access, vol. 8, pp. 22281–22302, 2020.

[14] H. P. Vemuganti, D. Sreenivasarao, S. K. Ganjikunta, H. M. Suryawanshi, and H. Abu-Rub, "A survey on reduced switch count multilevel inverters," IEEE Open J. Ind. Electron. Soc., vol. 2, pp. 80–111, 2021.

[15] A. Bughneda, M. Salem, D. Ishak, S. Alatai, M. Kamarol, and K. B. Hamad, "Modified five-level inverter for PV energy system with reduced switch count," in Proc. IEEE IEACon, Nov. 2021, pp. 103–107.

[16] K. N. D. V. S. Eswar, M. A. N. Doss, P. Vishnuram, A. Selim, M. Bajaj, H. Kotb, and S. Kamel, "Comprehensive study on reduced DC source count: multilevel inverters and its design topologies," Energies, vol. 16, no. 1, p. 18, 2022.

[17] S. K. Baksi, R. K. Behera, and U. R. Muduli, "Comprehensive overview of reduced switch count multilevel inverter for PV applications," in Proc. IEEE 3rd Int. Conf. on Smart Technologies for Power, Energy and Control (STPEC), Dec. 2023, pp. 1–6.

[18] V. K. N. V. and T. G., "A comprehensive survey on reduced switch count multilevel inverter topologies and modulation techniques," J. Electrical Systems and Information Technology, vol. 10, no. 1, p. 3, 2023.

[19] R. T. Srungaram and K. Yadlapati, "Machine-learning based control of bi-modular multilevel PWM inverter for high power applications," PLOS ONE, vol. 19, no. 7, e0305759, 2024.

[20] J. Chouhan, P. Gawhade, A. Ojha, and P. Swarnkar, "A comprehensive review of hybrid energy systems utilizing multilevel inverters with minimal switch count," Electrical Engineering, vol. 107, no. 7, pp. 8937–8961, 2025.