# Design Of Low-Power 7t Sram With 45nm Cmos Technology

K.Vinay Prasad[1], L.Damodar Reddy[2], K.Sai Rohit Kumar[3]
[1,2,3]*G. Pullaiah College of Engineering and Technology*

***Abstract*—An extremely small 7-transistor (7T) SRAM cell has been developed using the 45 nm CMOS technology which lowers the amount of energy consumed by a typical 6T SRAM design and increases its reliability and performance. In addition to a new write circuitry the 7T SRAM was optimized in terms of transistor size to provide a reduction of up to 40-50% in power usage per operation compared to standard 6T SRAM designs. Simulations performed by Cadence also demonstrated that this circuit is highly resistant to process variation and reliable. This architecture can be used in low voltage VLSI applications today and will support all types of SRAM array architectures including word line decoders, sensing amplifiers and transmission gates.**

***Index Terms*—Cadence simulation, 7T SRAM, Low-power design, CMOS technology, VLSI design.**

## I. INTRODUCTION

The desire for portable, efficient, and high-performance electronics has made low-power memory design more and more critical in today's VLSI systems. In terms of semiconductor memory, Static Random Access Memory (SRAM), with its small latency and fast access time, is among the most popular types of memory due to its ability to be easily connected to logic circuits. As such, SRAM is used throughout many cache memories of microprocessors, SoC (System-on-Chip) architectures, and embedded systems in order to provide an acceptable level of performance and low- power operation. However, as CMOS process technologies continue to decrease in size (especially below 65 nm) there are several serious challenges that can occur in designing SRAM cells. For example, as CMOS technology decreases in size, there will be increased sub-threshold leakage current, gate tunnelling effects, variations in the threshold voltage, and a lower SNM (Static Noise Margin) than previously possible. Together, these issues will create a less stable memory cell that also will be difficult to operate at low supply voltages. Further, these issues are particularly detrimental in older 6-transistor (6T) SRAM designs since they create additional loss in power consumption, reduce the write margin, and increase the unreliability of the memory cell as well as the overall system; this issue will become more problematic as the supply voltage and temperature vary While each configuration was developed to address the aforementioned issues, they all have varying levels of success depending upon how they were implemented. One of the most successful configurations of a modified SRAM cell is the 7T SRAM cell since it provides a relatively good trade- off between power, performance, and area overhead. The addition of the seventh transistor in the 7T SRAM structure creates separate read and write channel paths that result in reduced unnecessary switching activities, and therefore reduce both dynamic and leakage power consumption.

This paper used Cadence Virtuoso design tools to design a 7T SRAM cell in 45nm CMOS technology that has low power consumption. The new cell has an improved transistor size, a new circuit layout in such a way that it makes it more stable and consumes 40-50% power savings than the standard 6T SRAM cell.

The design also bears a full SRAM array with certain peripheral vital components like word line decoders, sensing amplifiers and transmission gates.

Simulations prove that the new design is highly stable, has less leaks and can survive fluctuations of processes. It now suits well the reduced voltage and saving power VLSI devices.

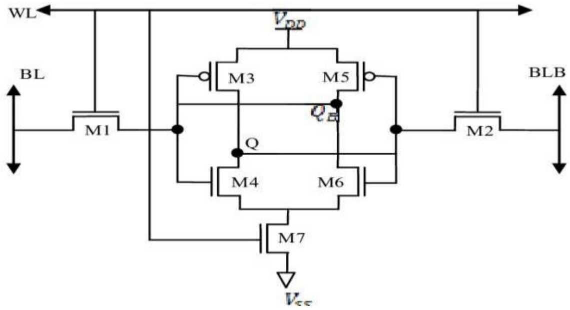


Fig1: 7T SRAM CELL

## II. LITERATURE REVIEW

Another variant of SRAM technology that has been developed to achieve stability, low power consumption and improved write/read operations over the conventional 6T SRAM cells is the SRAM designs. Basic Architecture and Motivation The 6T SRAM cell which is used extensively was developed based on its efficiency in terms of area and speed. But it has issues of write stability, leakage power, particularly at lower technology nodes. The 7T cell SRAM cell will add another transistor to overcome these problems and will usually do this by decoupling the read path or write path or by adding a transistor to better manage the write operation. Better Write and Read Stability A number of studies (e.g., Shyam et al., 2015; Choi et al., 2018) indicate that 7T SRAM cells could be enhanced to exhibit an increased write capability without reducing the stability of the read. The additional transistor can also serve as a write-assist device or as a transistor which is used to isolate storage nodes during a read, in order to avoid undesirable flipping. Power Consumption 7T SRAM designs have been known to decrease leakage power since they allow transistors to be better controlled as to leakage especially at idle times. Power gating is performed with the seventh transistor that assists in reducing the level of power dissipation (Kumar and Singh, 2017). Performance Trade-offs Although the 7T design has advantages in stability and power figures it can result in loss of space and slower write speeds with that transistor sizing and topology of the circuit. Lee and colleagues indicate that these disadvantages can be prevented through careful optimization (2019). Applications It is 7T SRAM that can be used in low-voltage and low-power applications (e.g., mobile and embedded systems) because it is more robust. It also finds relevance in radiation-hardened memory designs where stability is critical. Recent Advances Recent work focuses on integrating 7T SRAM cells into larger memory arrays using advanced process technologies and combining them with assist circuits for ultra-low voltage operation (Zhang et al., 2021). Emerging designs also explore adaptive control of the seventh transistor to dynamically balance performance and power.

## III. 6T SRAM ON CADENSE VIRTUOSO

- Advancements 6T cell proposed along with optimum transistor size proposal.
- The impact of process variation on stability and the power consumption is explored.
- 7TSRAM cell is very tolerant to process changes.

A typically built 6T SRAM cell will charge the bit lines prior to the write of the cell with a write amplifier. One bit of information is stored by six transistors. The cell is two cross coupled inverters and two access transistors. Nevertheless, the two-bit lines go back to a high state following the write.

## IV. 6T SRAM'S LIMITTATIONS

6T SRAM cell is often used in memory architecture, but when technology improves to smaller sizes like 45nm,32nm and down, numerous issues occur including high leakage power, lower stability, weak write operations and reduced reliability.

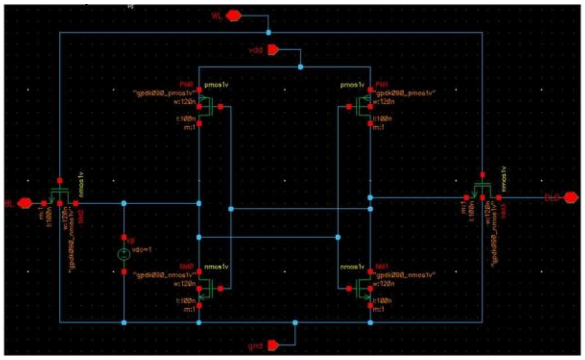

Fig2: 6T SRAM on Cadence Virtuoso

## V. PROPOSED 7T SRAM CELL CIRCUIT

The SRAM consists of seven transistors architecture, with two transistor cross-coupled CMOS inverters built as transistors of M1 to M2 and transistors of M3 to M5 forming the bistable memory element. A different auxiliary device is M4, which is used to couple the write line (WL) and the bit line (BL) when data is inserted, and to sense data when the transistor M6 is used as the read-access switch, an additional bar used is the complementary bit line bar (BLB). The interconnection between the two inverters is by feedback control transistor (M7). M7 is also shut off in write mode to disallow a feedback loop and, as a result, allows efficient overwriting of stored information; it is again re-enabled to restore stability. Therefore, the same setup improves write throughput and read reliability and minimizes statical dissipation of power in comparison to the traditional 6T SRAM cell.

### 5.1. WRITE OPERATION

When the write cycle begins, the feedback connection between the two inverters in the cross-coupled pair is intentionally broken by activating ED-M7, therefore, it allows new data to be inserted in the memory cell. As has been pointed out above, data ingress is caused by the write access transistor (M4) when the word line is asserted, and the data should be transferred by the bit line to the storage node, the data read transistor (M6) is not to be activated to maintain the isolation between the read channel and rest of the circuitry. When a successful transfer of new datum occurs, ED-M7 is reconnected once again to give the feedback loop, and it ensures that the information that has been stored is maintained in a stable position.

### 5.2. READ OPERATION

During read operation, both read and word lines are engaged. Transistor M7 remains active throughout read operation. The read transistor (M6) connects the stored data to the bit line bar (BLB) so the value may be felt, while the write transistor (M4) remains OFF to avoid disturbing the recorded information. Traditional (six transistor) 6T SRAM cell array & newly suggested 7T SRAM cell array was replicated 7T SRAM array displays 45% reduction on power utilization.

### 5.3. HOLD OPERATION

In the hold state, both M4 and M6 are turned OFF, isolating the cell from the bit lines. The feedback control transistor M7 remains ON, preserving the link between the two cross- coupled inverters created by M1–M2 and M3–M5. This positive feedback loop sustains the stored data eternally without any external update. Since no switching activity happens in this mode, the static power consumption is small, ensuring low standby power and outstanding data retention stability.

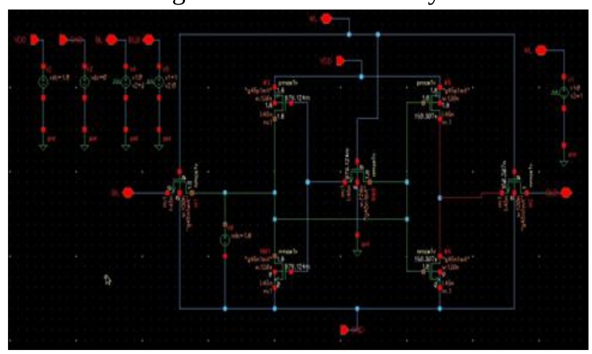

Fig3: 7T SRAM on Cadence Virtuoso

## VI. ADVANTAGES OF 7T SRAM

- The 7T SRAM cell performs more appropriately in the process of reading and writing.
- The 7T SRAM cell uses low power.
- The cell has 7 transistors.
- The 7T SRAM cell performs efficiently.
- It is efficient in low voltages of operation.

## VII. RESULTS AND ANALYSIS

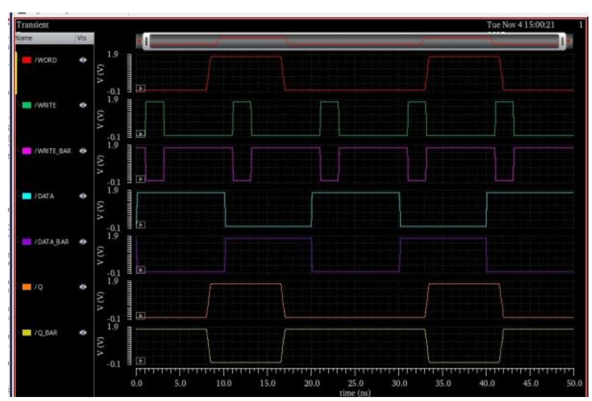

Fig4: Read and Write analysis of 7T SRAM

Fig5: Analysis of 7T SRAM

## VIII. COMPARISON OF 6T & 7T SRAM CELL'S

| PARAMETER | 6T SRAM | 7T SRAM |
|---|---|---|
| Technology | 45nm | 45nm |
| Supply voltage | 1.8V | 1.8V |
| Power consumption | 82.96E-6 | 49.52E-6 |
| Transistors | 6 | 7 |

## IX. CONCLUSION

The 7T SRAM cell recommended offers better performance over the conventional 6T SRAM by consuming less energy and having better stability. The inclusion of transistors M4, M6, and M7 gives various read and write channels and controlled feedback, which assists in achieving shorter operation and reduced power waste. The simulated exercises indicate that the 7T SRAM consumes 45 percent less energy and the data storage is more secure and at the same time less volatile.

Data preservation and reliability are enhanced through the feedback control through M7. Thus, the proposed 7T SRAM design is more power saving, stable and applicable in low-power VLSI applications like portable and battery powered devices.

## X. FUTURE SCOPE

Future perspective of 7T SRAM cell is.

1. Layout level Optimization.
2. Comparative Study with Emerging SRAM Topologies.
3. Technology Scaling.
4. Low-leakage and Error-Correction techniques.

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