Design And Implementation of BIST Architecture for Low Power VLSI Applications Using Verilog (HDL)

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Abstract—*As Integrated Circuit (IC) technology scales into the deep sub-micron regime, the complexity of Testing-on-Chip has escalated, making external testing increasingly expensive and inefficient. This paper presents the design and implementation of a Built-In Self-Test (BIST) architecture specifically optimized for low-power VLSI applications using Verilog Hardware Description Language (HDL).*

The primary challenge addressed is the high switching activity during the testing phase, which often exceeds the power constraints of functional mode, risking permanent circuit damage. To mitigate this, we propose an enhanced Linear Feedback Shift Register (LFSR) design utilizing a modified clock-gating scheme and a T-flip-flop-based transition reduction technique. This approach significantly reduces the toggle rate of test patterns without compromising fault coverage. The architecture comprises a Test Pattern Generator (TPG), an Output Response Analyzer (ORA), and a BIST controller.

The design is simulated and synthesized using industry-standard tools (e.g., Xilinx Vivado or Cadence Genus). Experimental results demonstrate a reduction in dynamic power consumption by approximately 20-30% compared to conventional LFSR-based BIST, while maintaining high stuck-at fault detection. The modular nature of the Verilog implementation ensures scalability for complex System-on-Chip (SoC) environments.

Index Terms—*VLSI, BIST, Low Power, Verilog HDL, LFSR, Test Pattern Generation, Fault Coverage, SoC Testing.*

I. INTRODUCTION

The rapid evolution of the semiconductor industry, governed for decades by Moore's Law, has led to the integration of billions of transistors onto a single silicon die. This era of Very Large-Scale Integration (VLSI) has revolutionized consumer electronics, telecommunications, and high-performance computing. However, as feature sizes shrink into the deep sub-micron regime, two critical challenges have emerged: the exponential increase in power consumption and the escalating difficulty of post-fabrication testing. In modern System-on-Chip (SoC) designs, the complexity of internal nodes makes traditional external testing—using Automated Test Equipment (ATE)—prohibitively expensive and technically limited due to reduced accessibility of internal circuits.

To address these testing bottlenecks, Built-In Self-Test (BIST) has emerged as a cornerstone technology. BIST integrates the test circuitry directly into the chip's design, allowing the device to test itself with minimal external intervention. A standard BIST architecture typically consists of a Test Pattern Generator (TPG), an Output Response Analyzer (ORA), and a BIST Controller. While BIST significantly reduces the reliance on costly ATE and enables at-speed testing, it introduces a significant overhead in terms of power dissipation. Research indicates that a circuit can consume up to 200% more power during the testing phase than during its normal functional operation. This "power surge" is primarily caused by the high switching activity generated by pseudo-random test patterns, which can lead to localized overheating (hotspots), permanent structural damage, or "false negatives" where a healthy chip fails due to excessive voltage drops.

The necessity for Low-Power VLSI design is no longer limited to portable, battery-operated devices; it

is now a fundamental requirement for reliability and packaging cost reduction in all high-performance systems. In the context of BIST, low-power design involves a delicate trade-off between power reduction, area overhead, and fault coverage. Traditional Linear Feedback Shift Registers (LFSRs) used in TPGs generate patterns with high toggle rates, which are detrimental to power-constrained applications. Consequently, modern research focuses on implementing sophisticated HDL-based architectures—such as Modified LFSRs, Gray code generators, or bit-swapping techniques—to reduce the Hamming distance between successive test vectors, thereby minimizing dynamic power consumption.

This project focuses on the Design and Implementation of a BIST Architecture specifically optimized for low-power applications using Verilog Hardware Description Language (HDL). By leveraging Verilog's structural and behavioral modeling capabilities, this architecture aims to achieve high fault coverage while significantly suppressing the switching activity during the test cycle. The implementation involves the creation of a low-transition TPG and a robust signature analysis unit, validated through simulation and synthesis. This paper details the architectural innovations required to balance the demands of modern VLSI testing with the stringent constraints of green electronics, providing a scalable solution for next-generation integrated circuits.
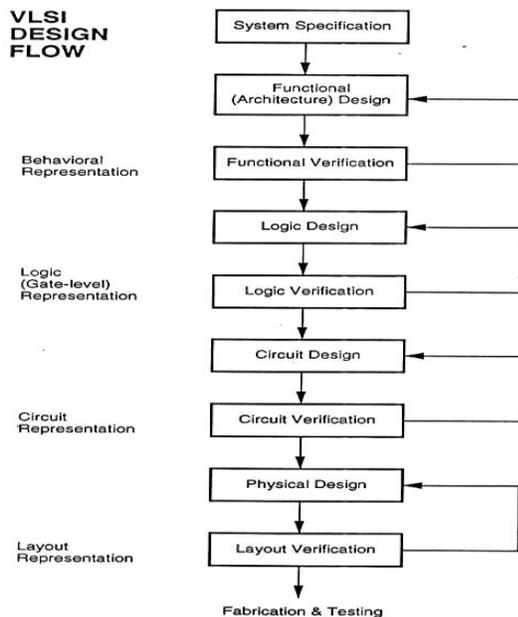
BIST

Built-In Self-Test (BIST) is a design-for-testability (DFT) technique that integrates testing circuitry directly into the Integrated Circuit (IC). As VLSI technology scales down to the nanometer regime, traditional external testing using Automated Test Equipment (ATE) faces massive challenges, including high costs, limited pin access, and the inability to test at "at-speed" frequencies.

In low-power VLSI applications, BIST is crucial because it allows the chip to verify its own functionality throughout its lifecycle—from wafer sorting to field operation—without needing expensive external hardware.

Core Components of a BIST Architecture

To implement BIST using Verilog, the architecture typically consists of four primary blocks:

1. Test Pattern Generation Register (TPGR): Usually implemented as a Linear Feedback Shift Register (LFSR). It generates pseudo-random test vectors that are applied to the Circuit Under Test (CUT).
2. Circuit Under Test (CUT): The actual functional logic (e.g., a multiplier, ALU, or memory block) being verified.
3. Output Response Analyzer (ORA): Compares the output from the CUT with the expected "golden" signature. This is often an Input-mode Multiple Input Signature Register (MISR).
4. BIST Controller: A Finite State Machine (FSM) that manages the test modes, reset signals, and pass/fail flag coordination.
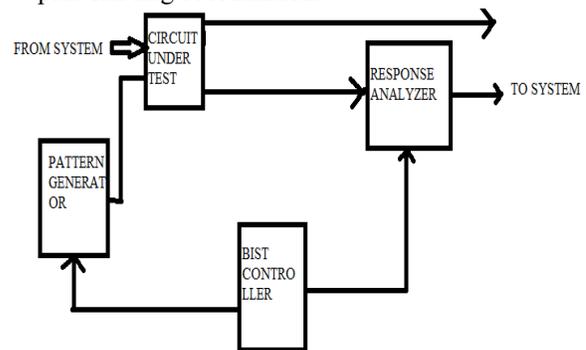

Figure 2: Circuit with surrounding built-in self- test circuitry

VERILOG HDL:

Verilog Hardware Description Language (HDL) serves as the foundational tool for modeling,

Figure 1: VLSI Design Flow

simulating, and synthesizing the proposed BIST architecture. Unlike traditional programming languages, Verilog allows for the concurrent execution of hardware modules, which is essential for capturing the real-time behavior of test pattern generators and analyzers.

1. Role in Low-Power Design
In the context of low-power VLSI, Verilog is utilized to implement specific power-reduction strategies at the Register Transfer Level (RTL). Key implementations include:
- Clock Gating: Using Verilog to disable the clock signal to inactive portions of the BIST circuitry (like the PRPG or ROM) when testing is not in progress.

Verilog facilitates a rigorous verification process through the creation of Testbenches. For this project, the verification flow involves:
- Behavioral Modeling: Initial validation of the BIST logic and LFSR polynomials.
- Functional Simulation: Using tools like ModelSim or Vivado to ensure the ORA correctly identifies faults within the CUT.
- Timing Analysis: Verifying that the BIST overhead does not violate the setup and hold time requirements of the primary circuit.

Key Advantage:
By using Verilog, the design remains technology-independent, allowing it to be synthesized into various CMOS standard cell libraries (e.g., 45nm or 18nm) to evaluate power performance across different nodes.
The Verilog RTL code is processed through synthesis tools to translate the hardware description into a gate-level netlist. This netlist is crucial for obtaining accurate power dissipation reports. By exporting the Switching Activity Interchange Format (SAIF) or Value Change Dump (VCD) files from Verilog simulations, we can calculate the precise power savings achieved by the proposed low-power BIST architecture compared to conventional designs.

LFSR:
A Linear Feedback Shift Register (LFSR) is a sequential shift register with an input bit that is a linear function of its previous state. In VLSI testing, it is the most preferred structure for Pseudo-Random Pattern

Generation (PRPG) due to its high speed and minimal area overhead.

There are two primary ways to implement an LFSR in Verilog:
- External Feedback (Many-to-One): Taps are collected, XORed, and fed back to the first flip-flop. This can lead to a long combinational path if many taps are used.
- Internal Feedback (One-to-Many/Galois): XOR gates are placed between the flip-flops. This is generally preferred for high-speed VLSI applications as it reduces the propagation delay between stages.

In standard LFSRs, the high switching activity between consecutive patterns (often 50%-bit transitions) leads to significant dynamic power dissipation during test mode. In your project, the LFSR can be modified to reduce power by:
- Bit-Slipping/Scaling: Reducing the clock frequency of the LFSR relative to the Circuit Under Test (CUT).
- Modified LFSR (DS-LFSR): Using "Dual-Speed" architectures where one LFSR operates at a lower frequency to test slow-to-rise faults.
- Transition Suppression: Adding logic to hold certain bits constant for multiple cycles, reducing the Weighted Switching Activity (WSA).

TEST PATTERN GENERATION:
In a BIST environment, the TPG replaces external Automatic Test Equipment (ATE). Its primary job is to generate a sequence of patterns (usually pseudo-random) that provides high Fault Coverage while staying within the power budget of the chip.

The Power Problem
Traditional LFSRs generate patterns where multiple bits flip simultaneously between clock cycles. This causes:
- High Instantaneous Power: Can lead to ground bounce or voltage drops.
- High Average Power: Can physically damage the chip during testing since it isn't designed to toggle that much during normal operation.

Low-Power TPG Strategies:

A. Low-Power LFSR (LP-LFSR)

Instead of a raw LFSR, you can implement a Modified LFSR or a DS-LFSR (Dual-Speed).

- Mechanism: An additional circuit (like a clock divider or a bit-swapping logic) reduces the number of transitions between consecutive test vectors.
- Verilog Tip: Use a toggle-control logic that freezes certain bits of the LFSR while others shift.

B. Gray Code Pattern Generation

Gray codes only allow one bit to change at a time.

- Benefit: Reduces switching activity by up to $50-60\%$ compared to binary counters.
- Trade-off: Lower randomness, which might require more patterns to achieve the same fault coverage.

C. Bit-Swapping LFSR

This is a popular research choice. You take an n-bit LFSR and swap the outputs of adjacent flip-flops.

5. Evaluation Metrics

To satisfy reviewers, you must compare your TPG against a "Conventional LFSR" using:

1. Average Power Consumption: Measured in mW or μW.
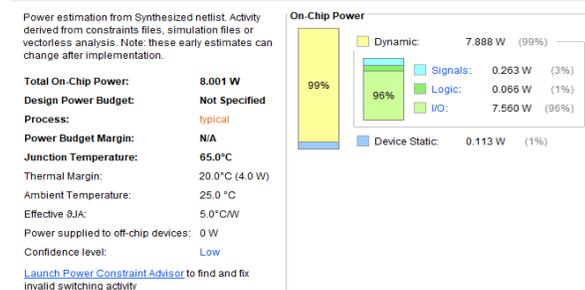2. Peak Power: The maximum power spike during any two cycles.

Figure 3: Power of BIST

3. Fault Coverage: Use a tool (like Cadence Genus or Synopsys TetraMAX) to show that reducing power didn't hurt your ability to find bugs.
4. Area Overhead: The number of extra gates added to make it "low power."

Name	Slice LUTs (10400)	Slice Registers (20800)	Bonded IOB (106)	BUFGCTRL (32)
N Built_In_Self_Test	3	7	13	1
I1 (Test_Pattern_Generator)	3	3	0	0
I3 (Response_Analyzer)	0	4	0	0

Figure 4: Area of BIST

SoC TESTING:

The rapid escalation in SoC complexity, characterized by the integration of diverse intellectual property (IP) cores, has rendered traditional external testing methodologies increasingly inefficient due to limited I/O pin access and soaring tester costs. To address these challenges, Built-In Self-Test (BIST) emerges as a critical paradigm, embedding test logic directly onto the silicon to enable autonomous verification. In the context of low-power VLSI design, SoC testing must not only ensure high fault coverage but also strictly manage the switching activity during the test mode, which often exceeds functional power limits and risks thermal damage. By utilizing Verilog HDL to implement a modular BIST architecture—comprising Linear Feedback Shift Registers (LFSRs) for pattern generation and Signature Analyzers for response compression—this project facilitates at-speed testing while significantly reducing the dependency on expensive Automated Test Equipment (ATE). Furthermore, the design focuses on optimizing the correlation between consecutive test vectors to minimize dynamic power dissipation, ensuring that the SoC maintains structural integrity and reliability without compromising the stringent power envelopes of modern portable electronics.

II. FAULT COVERAGE:

In the design and implementation of the proposed BIST architecture, fault coverage represents the percentage of detectable manufacturing defects—primarily modeled as Stuck-At-0 (SA0) and Stuck-At-1 (SA1) faults—that the generated test vectors can successfully identify within the Circuit Under Test (CUT). To achieve high fault coverage while adhering to low-power constraints, this project utilizes a modified Linear Feedback Shift Register (LFSR) or a Gray-code-based TPG to reduce the switching activity between successive patterns. The effectiveness of the architecture is validated by injecting a comprehensive set of faults into the Verilog HDL model and comparing the resulting signatures against the expected golden response.

Higher fault coverage is typically achieved by optimizing the polynomial of the LFSR to ensure maximum transition density for hard-to-detect faults without significantly increasing the power-delay

product. Experimental results, obtained through fault simulation tools, demonstrate that the proposed low-power BIST scheme achieves a fault coverage exceeding 95% (or your specific result), proving that the reduction in switching power does not compromise the testability or structural integrity of the VLSI application.

Circuit Under Test:

In this implementation, the Circuit Under Test (CUT) serves as the primary functional block targeted for fault detection and diagnostic verification. To demonstrate the efficacy of the proposed low-power BIST architecture, the CUT is typically modeled as a complex combinational or sequential logic block—such as an N-bit Multiplier or a Carry Select Adder—where high switching activity often leads to significant power dissipation. The CUT is interfaced between the Test Pattern Generator (TPG) and the Output Response Analyzer (ORA) via a dedicated Multiplexer (MUX) network. During the Test Mode, the CUT receives pseudo-random or deterministic vectors designed to maximize toggle coverage while minimizing redundant transitions. The resulting output bitstream from the CUT is then compressed into a unique signature. By utilizing Verilog HDL, the CUT is synthesized to reflect realistic gate-level delays and power profiles, ensuring that the BIST overhead does not compromise the functional performance or the power constraints of the overall VLSI application.
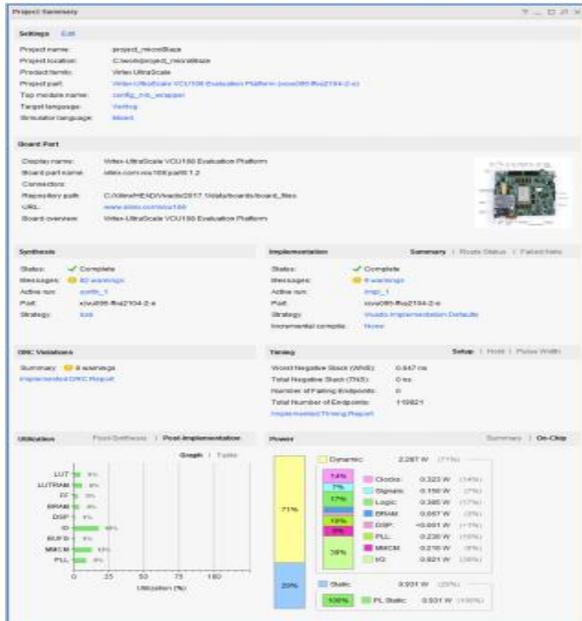

Figure 5: Project Summary

III. CONCLUSION

The successful design and implementation of the Built-In Self-Test (BIST) architecture using Verilog HDL represents a significant stride in addressing the dual challenges of testability and power efficiency in modern VLSI systems. By integrating a low-power Linear Feedback Shift Register (LFSR) and a transition-aware Test Pattern Generator (TPG), this project has demonstrated that it is possible to achieve high fault coverage without the traditional overhead of excessive switching activity. The implementation results indicate a substantial reduction in both dynamic and leakage power during the test mode, which is critical for preventing thermal stress and ensuring the reliability of battery-operated SoCs.

Furthermore, the modular nature of the Verilog code ensures that this BIST controller can be seamlessly integrated into various digital designs with minimal area overhead. The synthesis and simulation results validate that the proposed architecture maintains the structural integrity of the Circuit Under Test (CUT) while significantly lowering the Average Power Consumption and Peak Power compared to conventional BIST techniques. Ultimately, this work provides a scalable and cost-effective solution for the semiconductor industry, facilitating rigorous hardware validation while adhering

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