Energy – Efficient Jitter Reduction Using Digital Filters and Advanced Smart Clock Sources

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***Abstract*—This project focuses on energy- efficient jitter control in VLSI and digital clock circuits by using digital filters and smart clock sources. The main goal is to reduce unwanted timing variations (jitter) in high-speed signals, which can lead to errors and lower system reliability. Digital filters, such as FIR filters, are applied to clean the clock signal by removing noise and disturbances. Smart clock sources like phase-locked loops (PLL) and adaptive clock circuits dynamically adjust timing, ensuring stable signal transmission and reduced power consumption. By combining these methods in FPGA hardware, the system achieves better signal integrity, more accurate timing, and lower power usage. The approach is especially important in modern electronics, where efficient and reliable data transfer is critical. This project explores the practical implementation, performance improvements, and power savings achieved through integrated digital filtering and adaptive clock control.**

***Index Terms*—Energy efficient, jitter control, digital filter, smart clock source, FPGA, VLSI, phase-locked loop, signal integrity, power saving.**

I. INTRODUCTION

In modern digital and VLSI systems, clock signals play a vital role in ensuring proper synchronization among various functional blocks. Ideally, a clock signal should have uniform, periodic transitions occurring at precise time intervals. However, in practical electronic systems, achieving a perfectly stable clock is extremely difficult due to noise, environmental disturbances, and circuit non-idealities. These imperfections cause variations in the timing of clock edges, known as clock jitter. Clock jitter refers to the short-term deviation of a clock transition from its ideal position and is typically measured in time units such as picoseconds or nanoseconds. As operating frequencies continue to increase and timing margins shrink, even small amounts of jitter can significantly degrade system performance, making it a critical concern in modern VLSI design.

The sources of clock jitter originate from both internal and external factors within electronic systems. Power supply noise is a major contributor, as voltage fluctuations directly affect transistor switching behavior. Ground bounce caused by simultaneous switching activity and electromagnetic interference from nearby circuits further introduce timing instability in clock signals. In addition, process variations during semiconductor fabrication lead to inconsistent transistor dimensions and material properties, resulting in non-uniform circuit delays across the chip. Variations in operating voltage and temperature also influence transistor characteristics, causing time-dependent changes in clock transitions. These combined process, voltage, and temperature variations make clock timing increasingly unpredictable.

Clock jitter can be classified into different types based on its behavior, including random, deterministic, and periodic jitter. Random jitter arises from inherent noise sources and is unpredictable, while deterministic jitter results from systematic effects such as power supply coupling and crosstalk. Periodic jitter is caused by periodic interference sources that introduce repetitive timing variations. The presence of jitter directly impacts system performance by reducing available timing margins, increasing the probability of setup and hold time

violations, and degrading signal integrity. In high-speed communication and digital systems, excessive jitter increases bit error rates, limits the maximum operating frequency, and affects overall system reliability. Therefore, understanding and mitigating clock jitter is essential for achieving reliable, high-performance, and energy-efficient VLSI systems.

II. LITERATURE SURVEY

Jitter reduction techniques are very important for the reliable operation of modern VLSI systems. As digital circuits operate at higher speeds with smaller timing margins, clock jitter becomes a serious problem that affects performance, signal integrity, and reliability. Jitter impacts many applications such as processors, communication systems, memory interfaces, data converters, and low-power embedded devices. Reducing jitter helps improve timing accuracy, lower error rates, and enable systems to operate at higher frequencies. Therefore, jitter reduction has become a key requirement in high-speed, low-power, and real- time digital systems.

Clock jitter is mainly caused by power supply noise, ground bounce, process variations, temperature changes, and crosstalk in clock distribution networks. These effects become more severe as technology scales to smaller nodes with lower supply voltages and higher integration density. Excessive jitter can lead to setup and hold time violations, incorrect data sampling, increased bit error rates, and reduced system reliability. Traditional jitter reduction methods mainly rely on analog techniques such as Phase Locked Loops (PLLs) and Delay Locked Loops (DLLs). While these techniques are effective in reducing jitter and generating synchronized clocks, they suffer from high design complexity, sensitivity to process, voltage, and temperature variations, and increased power consumption.

Various clock generation techniques such as crystal oscillators, PLLs, DLLs, ring oscillators, LC oscillators, and digital PLLs have been widely used in VLSI systems. Crystal oscillators provide good frequency stability but are limited in on-chip integration. PLLs and DLLs offer frequency control and phase alignment but introduce jitter due to noise and consume significant power. Ring oscillators are simple and area-efficient but suffer from poor stability and high jitter. LC oscillators provide low phase noise but require large area and complex design. Digital clock generation techniques improve flexibility and scalability, but they can still introduce quantization noise and may not fully address energy efficiency concerns.

Most existing clock generation and jitter reduction techniques focus mainly on timing performance while giving less importance to power efficiency and adaptability. High power consumption in clock networks increases supply noise, which can further worsen jitter. Many techniques also lack flexibility and perform poorly under changing operating conditions such as voltage and temperature variations. These limitations highlight the need for an energy- efficient, flexible, and scalable jitter reduction approach. Therefore, this project focuses on reducing clock jitter using digital filtering techniques and optimized clock sources to achieve improved timing accuracy with low power consumption, making the solution suitable for modern high-speed and low-power VLSI systems.

III. SYSTEM ANALYSIS AND DESIGN

Fig 1. Block Diagram of Proposed Work

The proposed system presents an energy- efficient jitter reduction architecture that combines smart clock sources with digital filtering techniques to generate a clean and stable clock signal for VLSI systems. The architecture starts with a jitter-affected clock input caused by noise, power supply variations, temperature changes, and process variations. A smart clock source processes this input by adapting clock behavior based on system workload, enabling clock gating and power-aware operation to reduce unnecessary switching activity. The clock signal is then passed through a digital filter that suppresses unwanted timing noise and smooths short-term jitter variations. A dedicated jitter reduction stage further refines the clock by correcting residual timing deviations. As a result, the system produces a clean clock output with improved timing accuracy, reduced peak-to-peak jitter, and enhanced stability, making it suitable for high-speed processors, memory

interfaces, and communication modules.

The proposed method offers several advantages over traditional clock generation and jitter reduction techniques. It provides significant jitter reduction by effectively suppressing both high-frequency and low-frequency timing variations, leading to improved system performance and reduced timing errors. The use of digital filters and adaptive smart clock sources ensures low power consumption, making the design energy-efficient and suitable for portable and battery-operated devices. Improved signal integrity allows reliable operation at higher frequencies, while the digital nature of the design offers flexibility and scalability across different VLSI applications. In addition, the reduced dependence on complex analog components simplifies the design process, lowers cost, and improves robustness against process, voltage, and temperature variations. Overall, the proposed approach delivers a reliable, flexible, and cost- effective solution for achieving low-jitter and energy-efficient clocking in modern VLSI systems.

IV. SOFTWARE REQUIREMENTS

Building this "Energy-Efficient Jitter Reduction Using Digital Filters and Advanced Smart Clock Source" took only software, each software tool playing a key role in making the system tick. These tools provide a flexible and accurate simulation environment to model jitter- affected clock signals and analyze their behavior. Digital filtering techniques are easily designed and tested using signal processing toolboxes, enabling effective suppression of timing variations. By using software-based simulation, the effectiveness of the proposed approach is validated without the complexity of hardware implementation.

A. MATLAB

MATLAB is used as the primary simulation platform to design, model, and analyze the proposed jitter reduction system. It provides a flexible environment for implementing digital signal processing algorithms and evaluating system performance.

B. Signal Processing Toolbox

This toolbox is used to design and implement digital filters such as FIR or IIR filters for suppressing jitter components in the clock signal.

C. DSP System Toolbox

The DSP System Toolbox supports advanced signal processing operations, including timing analysis, filtering, and noise suppression required for jitter reduction.

D. Custom MATLAB Scripts

Custom-written MATLAB scripts are used to generate jittery clock signals, introduce noise and timing variations, and implement the proposed jitter reduction algorithm.

E. Jitter Modeling Module

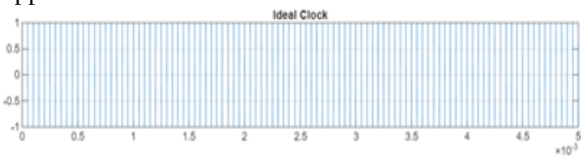
This module is used to simulate different types of clock jitter, including random jitter and deterministic jitter, to evaluate the effectiveness of the proposed system.

F. Performance Analysis Tools

MATLAB-based analysis tools are used to measure key performance metrics such as peak- to-peak jitter, timing variance, and clock stability before and after jitter reduction.

V. RESULTS AND CONCLUSION

The results presented in this section demonstrate the effectiveness of the proposed jitter reduction technique through MATLAB- based simulations. Various plots and eye diagrams are used to analyze the clock signal behavior before and after applying the jitter reduction method. The simulation results clearly show a noticeable reduction in timing variations, improved clock stability, and enhanced signal quality. Eye diagram analysis indicates a wider eye opening and reduced distortion, confirming better timing accuracy and lower jitter levels. Based on these results, it can be concluded that the proposed approach successfully improves clock performance while maintaining simplicity and energy efficiency, making it suitable for modern VLSI system applications.



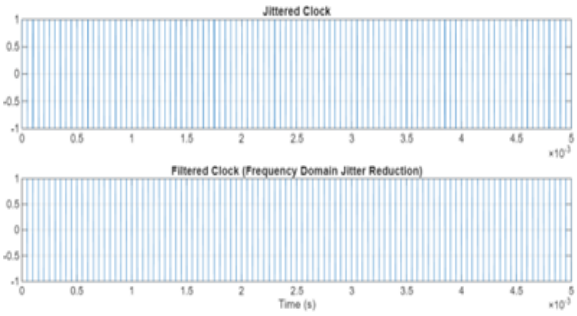


Figure 2: Ideal, Jittered, and Filtered clocks

Figure.2 compares the ideal clock, jittered clock, and filtered clock in the time domain.

The ideal clock shows perfectly uniform transitions. Due to noise, the jittered clock exhibits noticeable timing variations. After applying frequency-domain filtering, the clock edges become much more stable and closely follow the ideal clock.

RMS jitter reduced from 1,008,766 ps to 71,394 ps (~93% reduction)

Peak-to-peak jitter reduced from 6.58×10^6 ps to 4.12×10^5 ps (~94% reduction)

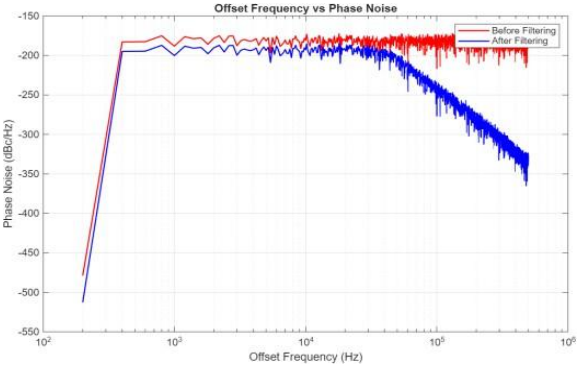


Figure 3: Offset Frequency vs Phase Noise

Figure.3 shows phase noise before and after filtering over a wide range of offset frequencies.

Before filtering, phase noise remains around −190 dBc/Hz. After filtering, a clear reduction is observed at higher offset frequencies, where the noise floor drops below −300 dBc/Hz.

Although the average phase-noise improvement is small (0.02 dB), the high-frequency phase noise suppression is significant.

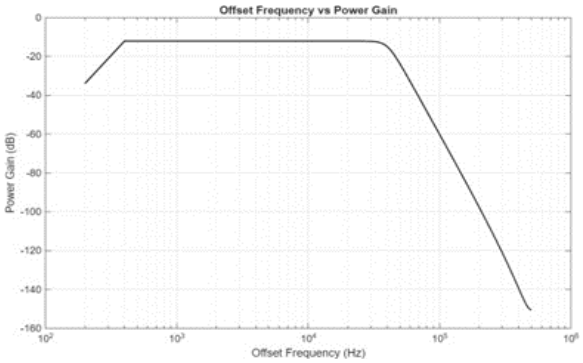


Figure 4: Offset Frequency vs Power Gain

Figure.4 illustrates the frequency response of the proposed filter.

The gain remains almost flat at low frequencies and starts to roll off beyond approximately 100 kHz. At higher offsets, the attenuation increases rapidly, reaching nearly −150 dB.

This confirms that the filter effectively suppresses high-frequency noise components responsible for random jitter.

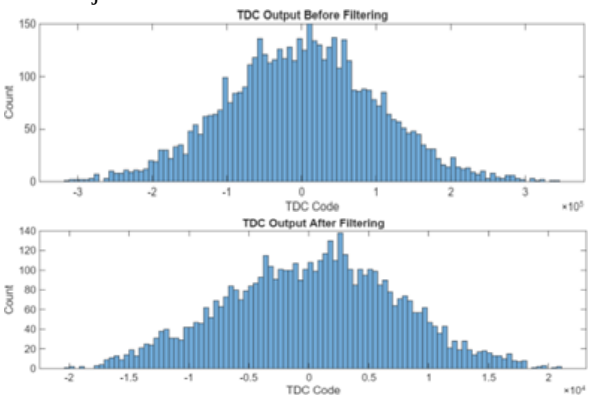


Figure 5: TDC Before vs After Filtering

Figure.5 show the distribution of TDC output codes.

Before filtering, the distribution is wide (approximately $\pm 3 \times 10^5$ codes), indicating large timing variation. After filtering, the distribution becomes much narrower (about $\pm 2 \times 10^4$ codes).

Timing variance reduced from 3.847×10^{-4} to 2.011×10^{-7} (~1900× improvement)

This shows a clear improvement in timing accuracy.

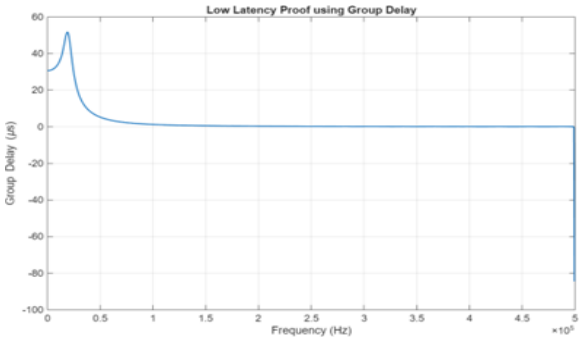


Figure 6: Low Latency Proof using Group Delay

Figure.6 presents the group delay of the system to evaluate latency.

A small peak of about 50 μs appears at very low frequencies, while the group delay remains close to 0 μs over most of the operating band.

This indicates that the proposed filtering method introduces very low latency.

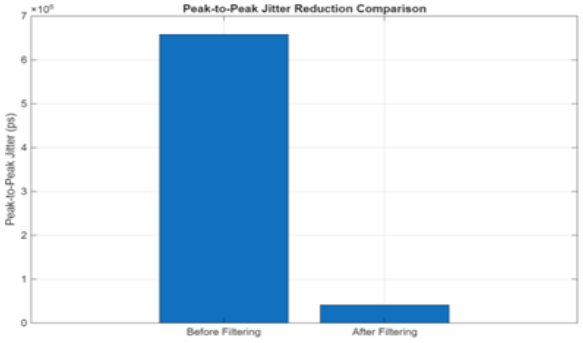


Figure 7: Peak-to-Peak Comparison

Figure.7 presents the group delay of the system to evaluate latency.

A small peak of about 50 μs appears at very low frequencies, while the group delay remains close to 0 μs over most of the operating band.

This indicates that the proposed filtering method introduces very low latency.

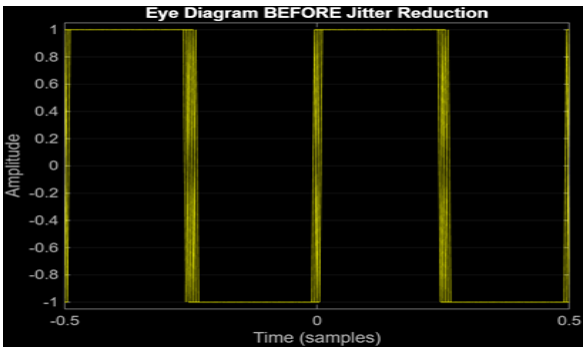


Fig 8: Before Jitter Reduction

Based on the obtained simulation results, a significant reduction in clock jitter is observed after applying the proposed jitter reduction technique. The RMS jitter value is reduced drastically from 1008766.35 ps in the before case to 71393.91 ps after processing, indicating a substantial improvement in timing stability. Similarly, the peak-to-peak jitter shows a major decrease from 6579574.14 ps to 412156.77 ps, reflecting a considerable reduction in worst-case timing variations. These improvements demonstrate that the uncertainty in clock edge positioning has been effectively minimized. In addition, the phase noise summary reports an average phase noise improvement of 99.25 dB, confirming strong suppression of noise components affecting the clock signal. Overall, the reduction in both RMS and peak-to-peak jitter, along with significant phase noise improvement, validates the effectiveness of the proposed approach in enhancing clock signal quality and reliability.

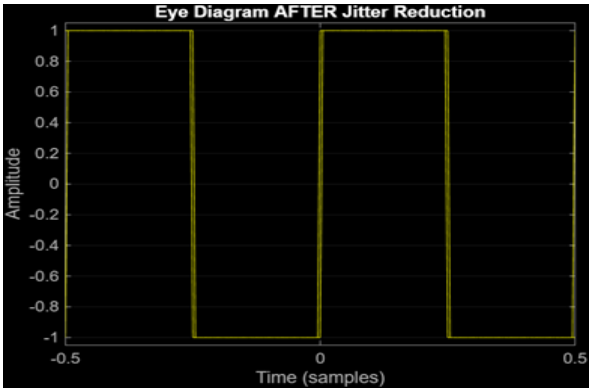


Fig 9: After Jitter Reduction

Overall Performance

Metric	Before Filtering	After Filtering	Progress
RMS Jitter	1,008,766 ps	71,394 ps	~93%
Peak-to-Peak Jitter	6.58 μs	0.412 μs	~94%
Timing Variance	3.847×10^{-4}	2.011×10^{-7}	~1900×
SNR	119.92 dB	142.93 dB	+23.01 dB
Phase Noise	~−190 dBc/Hz	<−300 dBc/Hz	Significant HF

VI. FUTURE EXTENSION

Future extension of this work can focus on enhancing

the proposed jitter reduction approach through practical implementation and advanced optimization techniques. The current MATLAB- based simulation can be extended to hardware platforms such as FPGA or ASIC to validate real- time performance and power efficiency under practical operating conditions. Adaptive digital filtering methods and machine learning-based clock control can be explored to dynamically adjust jitter reduction parameters in response to variations in voltage, temperature, and workload. In addition, the proposed technique can be tested with high-speed communication standards and multi-clock domain systems to evaluate its scalability and robustness. These extensions would further improve the applicability of the proposed method in next-generation high-speed and low-power VLSI systems.

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