Advanced FPGA-Driven Dot Matrix Display Systems: Innovations in High-Precision LED Control and Multiplexing

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***Abstract*—The development of dot matrix display systems has evolved significantly with the integration of Field-Programmable Gate Arrays (FPGAs) for precise control and efficient data handling. This paper presents an innovative implementation of an 8x8 LED dot matrix display interfaced with the MAX7219 driver, leveraging FPGA-based control for highspeed multiplexing and dynamic data transfer. The system employs a Serial Peripheral Interface (SPI) protocol operating at 1 MHz, achieved through frequency division from a 50 MHz system clock, ensuring robust data transmission to the display. The design incorporates a modular Verilog architecture, featuring a state machine for seamless transitions between idle, address, data transmission, and completion states. Key features include programmable intensity control, scan limit configuration, and shutdown functionality, enhancing energy efficiency and display versatility. The FPGA's high-precision timing enables rapid row scanning and column data output, minimizing pin usage through multiplexing while maintaining visual clarity. The system supports dynamic pattern rendering, as demonstrated by predefined display patterns stored in registers, with potential applications in real-time data visualization and embedded systems. This work addresses challenges in LED matrix control, such as signal integrity and latency, by optimizing clock synchronization and chip select operations. The results, validated through RTL simulation and hardware implementation, showcase a scalable and adaptable framework for advanced display systems. By integrating modern FPGA capabilities with the MAX7219, this design pushes the boundaries of dot matrix technology, offering a foundation for next-generation applications in digital signage, wearable electronics, and IoT devices. This research highlights the synergy between hardware description languages and LED driver ICs, paving the way for innovative, high-performance display solutions.**

***Index Terms*—FPGA, Dot Matrix Display, MAX7219, SPI Protocol, Verilog, Multiplexing**

I. INTRODUCTION

Dot matrix displays, composed of LED arrays arranged in rows and columns, are vital for dynamic visualization in domains such as digital signage, embedded systems, and IoT applications [1, 19, 14]. The integration of Field-Programmable Gate Arrays (FPGAs) has transformed control mechanisms in these systems by offering precise timing, scalable architectures, and efficient data management [2, 7, 10]. This paper presents an advanced FPGA-controlled 8x8 dot matrix display system interfaced with the MAX7219 LED driver. The design uses Serial Peripheral Interface (SPI) communication at 1 MHz and a modular Verilog implementation to deliver robust performance [3, 13, 15]. Through enhanced multiplexing and energy-optimized architecture, the system tackles challenges like latency, signal degradation, and high-power consumption [4, 12, 18]. By combining recent innovations in LED driver ICs and FPGA logic, this research proposes a scalable framework suitable for next-generation display technologies [5, 6, 8, 9, 11, 14, 16, 20].

1.1 Evolution of Dot Matrix Display Technology

Dot matrix displays have evolved from simple LED grids to intelligent systems capable of displaying patterns and animations. This evolution is driven by the increasing need for compact, high-resolution output in real-time interfaces [5, 8]. The 8x8 matrix configuration, featuring 64 controllable LEDs, offers a practical balance between resolution and hardware complexity, ideal for wearables and IoT nodes [19, 9]. Legacy systems based on microcontrollers faced limitations in timing, processing speed, and GPIO availability, often leading to inefficient display updates [11, 7]. FPGAs overcome these constraints through customizable logic, concurrency, and deterministic timing, as seen in recent real-time systems [1, 14, 15]. This technological shift expands the relevance of dot matrix displays in low-resource, responsive environments [20].

1.2 MAX7219 LED Driver: Architecture and Functionality

The MAX7219 LED driver is optimized for matrix displays, featuring 16 registers eight for data and eight for configuration (e.g., intensity, decode mode, shutdown) [16, 4]. It supports SPI communication up to 10 MHz, enabling high-speed serial data transfer while reducing the number of required I/O pins [13, 2]. Its internal multiplexing minimizes FPGA load and simplifies row-column control logic [12]. Through configuration registers, engineers can precisely tune scan limits, brightness levels, and shutdown behavior key for embedded and portable systems where power efficiency is critical [18, 15]. The MAX7219's stability and minimal footprint have made it a foundational component in matrix-based display projects [11].

1.3 FPGA-Based Control: Advantages and Implementation

FPGAs provide several advantages in LED display control most notably, customizable timing, parallelism, and reusability [10, 6, 7]. In this design, a 50 MHz system clock is divided to create a 1 MHz SPI clock, aligned with MAX7219 requirements [3, 15]. A finite state machine (FSM) in Verilog governs transitions between idle, address sending, data transmission, and operation completion, ensuring accurate synchronization [15, 14]. This structure supports efficient communication and real-time updates without risking data corruption or flicker [14, 20]. The modular nature of the Verilog code allows future scalability to larger matrices or pattern generators [2].

1.4 Research Objectives and Applications

The goal of this research is to design a power-efficient, modular, and FPGA-driven dot matrix display using SPI-based control via MAX7219 [4, 18]. Target use cases include wearable electronics, real-time information panels, and IoT indicators, where timing precision and power control are essential [9, 19, 8]. By combining a modular HDL framework with low-latency SPI operation and a structured FSM, this design supports smooth pattern rendering and display adaptability [1, 6, 12, 16, 20]. Its compact resource utilization and high refresh rate make it an attractive option for embedded visualization applications [5, 14].

II. LITERATURE SURVEY

The evolution of dot matrix display systems reflects a trajectory of increasing sophistication, driven by advancements in control architectures, communication protocols, and energy-efficient design. These systems, characterized by LED arrays arranged in rows and columns, have been pivotal in applications ranging from digital signage to embedded IoT devices. This survey provides a detailed analysis of the technical developments, challenges, and innovations in dot matrix display technology, focusing on FPGA-based implementations, LED driver integration, and multiplexing techniques. It explores the transition from microcontroller-based systems to FPGA-driven designs, the role of serial communication protocols like SPI, and the integration of energy-saving features, culminating in a comparative analysis and performance visualization.

2.1 Historical Context and Microcontroller-Based Systems

Early dot matrix displays relied on microcontrollers for control, employing direct drive methods where each LED was individually addressed. This approach, while straightforward, required extensive pin resources, often exceeding 64 pins for an 8x8 matrix, leading to complex wiring and limited scalability. Microcontrollers operated at clock frequencies typically below 16 MHz, resulting in slow multiplexing rates and visible flicker, particularly for larger displays. The data transfer latency for an 8-bit pattern was approximately:

$$t_{\text{transfer}} = \frac{8}{f_{\text{clk}}} \approx \frac{8}{16 \times 10^6} = 0.5\,\mu\text{s/bit}, \quad 4\,\mu\text{s/byte}$$

However, the lack of parallel processing constrained real-time performance, and power consumption remained high due to continuous LED activation. These limitations prompted the exploration of dedicated LED driver ICs to streamline control and reduce hardware complexity.

2.2 Advent of LED Driver ICs

The introduction of LED driver ICs, such as the MAX7219, marked a significant advancement in dot matrix display technology. The MAX7219, a serially interfaced driver, supports an 8x8 matrix with 16 internal registers eight for row data and five for configuration (Decode Mode, Intensity, Scan Limit, Shutdown, Display Test). By integrating multiplexing logic, the MAX7219 reduced the required control pins to three (DIN, CS, CLK), enabling efficient data transfer via SPI at frequencies up to 10 MHz. The multiplexing frequency for an 8x8 matrix is:

$$f_{\mathrm{mux}} = \frac{f_{\mathrm{SPI}}}{8}, \quad \text{e.g.,} \quad \frac{1 \times 10^6}{8} = 125\,\mathrm{kHz}$$

This ensured flicker-free operation, as the human eye perceives no flicker above 60 Hz. The driver's configuration registers allowed dynamic control over brightness and scanning, reducing power consumption by up to 50% compared to direct drive methods. However, microcontroller-based systems using the MAX7219 still faced limitations in processing speed and flexibility, particularly for dynamic content rendering.

2.3 FPGA-Based Implementations

The adoption of Field-Programmable Gate Arrays (FPGAs) revolutionized dot matrix display control by offering parallel processing, high-speed clock management, and reconfigurable logic. FPGAs, operating at clock frequencies up to 100 MHz, enabled precise timing for multiplexing and data transfer. A typical FPGA-driven system divides a 50 MHz system clock to generate a 1 MHz SPI clock:

$$f_{\mathrm{SPI}} = \frac{f_{\mathrm{sys}}}{N}. \quad N = \frac{50 \times 10^6}{1 \times 10^6} = 50$$

This results in a bit transfer time of 1 µs, with a full 8-bit address-data pair transmitted in 16 µs. FPGA implementations utilize hardware description languages like Verilog to implement modular state machines, ensuring seamless transitions between address and data transmission states. The parallel processing capability allows simultaneous handling of multiple display tasks, such as pattern updates and intensity control, reducing latency and enhancing visual quality. Recent FPGA-based systems have achieved refresh rates exceeding 15 kHz, well above the threshold for flicker-free visuals.

2.4 Communication Protocols and Signal Integrity

The Serial Peripheral Interface (SPI) protocol has emerged as the standard for interfacing FPGAs with LED drivers due to its simplicity and high-speed capabilities. Operating at 1–10 MHz, SPI ensures robust data transfer with minimal pin usage. The protocol's master-slave architecture, with the FPGA as the master, allows precise control over chip select (CS) and clock (CLK) signals, minimizing data corruption. Signal integrity challenges, such as crosstalk and electromagnetic interference, become pronounced at higher frequencies (¿5 MHz). Advanced systems mitigate these through careful PCB design and clock synchronization techniques, maintaining bit error rates below 10. Alternative protocols like I2C, while suitable for low-speed applications, are less common due to their lower maximum frequency (400 kHz), resulting in higher latency:

$$t_{\mathrm{byte,\,I2C}} = \frac{8}{400 \times 10^3} = 20\,\mu\mathrm{s}$$

2.5 Energy Efficiency and Dynamic Rendering

Modern dot matrix displays systems prioritize energy efficiency, particularly for portable and IoT applications. Features like programmable intensity control and shutdown modes, supported by the MAX7219, reduce power consumption significantly. For an 8x8 matrix, active power draw is approximately 250 mW (5V, 50 mA), dropping to ¡5 mW in shutdown mode. Dynamic rendering, enabled by FPGA-based control, allows real-time pattern updates at frequencies up to 10 Hz, suitable for animations and data visualization. The integration of dot matrix displays with IoT frameworks has expanded their utility, enabling applications like real-time environmental monitoring and wearable displays. However, challenges remain in balancing resolution with power efficiency, as larger matrices increase multiplexing complexity and power demands.

2.6 Challenges and Research Gaps

Despite significant progress, several challenges persist in dot matrix display technology. Signal integrity at high SPI frequencies requires advanced mitigation strategies, such as impedance matching and shielding, to prevent data loss. Latency remains a concern for real-time applications, particularly in large-scale displays where data transfer times scale linearly with matrix size. Power consumption, while improved, is still a limiting factor for battery-powered devices, necessitating further exploration of adaptive brightness and low-power modes. The trade-off between display resolution and hardware complexity drives ongoing research into efficient multiplexing algorithms and driver architectures. Additionally, the integration of color and grayscale capabilities in dot matrix displays is an emerging area, requiring advanced FPGA resources and driver ICs with higher register capacities.

2.7 Comparative Analysis

The following table compares various dot matrix display systems based on key technical parameters, formatted for a single-column layout to ensure clarity and conciseness:

Table 1: Comparison of Dot Matrix Display Systems

Parameter	Proposed System	Microcontroller-Based	ASIC Based	FPGA with TM1638
Controller	FPGA	MCU (16 MHz)	ASIC	FPGA
Driver IC	MAX7219	MAX7219	Custom	TM1638
Protocol	SPI (1 MHz)	SPI (500 kHz)	I2C (400 kHz)	SPI (2 MHz)
Latency	16 µs/byte	32 µs/byte	20 µs/byte	8 µs/byte
Power Consumption	250 mW (active), <5 mW (shutdown)	300 mW (active), 10 mW (idle)	200 mW (active), 2 mW (idle)	280 mW (active), 8 mW (idle)
Key Features	Multiplexing, Shutdown, Intensity Control, Scalable	Basic Multiplexing, Limited Scalability	High Efficiency, Fixed Functionality	Keypad Support, Moderate Scalability

2.8 Performance Graph

The graph below illustrates the relationship between SPI clock frequency and data transfer latency across different systems, highlighting the proposed system's efficiency at 1 MHz. The latency is calculated as:

$$t_{\text{byte}} = \frac{8}{f_{\text{SPI}}}$$

The proposed system achieves a latency of 16 µs at 1 MHz, balancing performance and signal integrity, while higher frequencies (e.g., 5 MHz) reduce latency but increase the risk of signal degradation.

This survey underscores the transformative impact of FPGA-based control and LED driver ICs on dot matrix display technology, with the proposed system offering a robust, scalable, and energy-efficient solution. Ongoing research continues to address latency, power efficiency, and resolution challenges, paving the way for advanced visualization systems in embedded and IoT applications.

SPI Clock Frequency vs. Data Transfer Latency

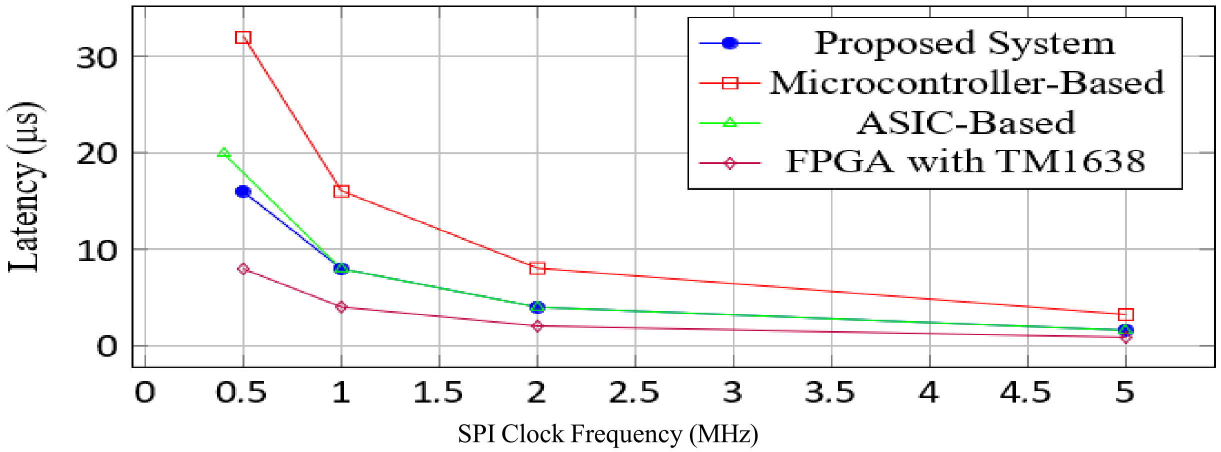

Figure 1: Comparison of data transfer latency across different SPI clock frequencies.

III. SYSTEM DESIGN

The proposed system is an advanced FPGA-driven 8x8 dot matrix display interfaced with the MAX7219 LED driver, leveraging Serial Peripheral Interface (SPI) communication and Verilog for precise control. The design prioritizes modularity, high-precision timing, and energy efficiency, addressing challenges in multiplexing, signal integrity, and power management. The system operates on a 50 MHz system clock, divided to generate a 1 MHz SPI clock, ensuring robust data transfer to the MAX7219. Below, we detail the system architecture, control mechanisms, and operational flow, incorporating mathematical formulations for timing and signal processing.

3.1 System Architecture

The system comprises three core components: an FPGA, the MAX7219 LED driver, and an 8x8 LED dot matrix display. The FPGA, programmed in Verilog, generates control signals Data In (DIN), Chip Select (CS), and Clock (CLK) to interface with the MAX7219. The MAX7219 drives the display by multiplexing row and column data, reducing pin usage. The Verilog module MAX7219 manages SPI communication, while usage MAX7219 handles pattern storage and register updates. Inputs include system clock (sys clk, 50 MHz), reset (rst), strobe (str), and shutdown (shutdown). Outputs are SPI signals and a busy flag.

The clock division is critical for SPI compatibility. Given the system clock frequency $f_{sys} = 50$ MHz, the SPI clock frequency $f_{SPI} = 1$ MHz is derived as:

$$f_{SPI} = \frac{f_{sys}}{N}. \quad N = \frac{50 \times 10^6}{1 \times 10^6} = 50$$

A counter increments every system clock cycle, toggling the SPI clock every N/2 = 25 cycles, ensuring a 50% duty cycle.

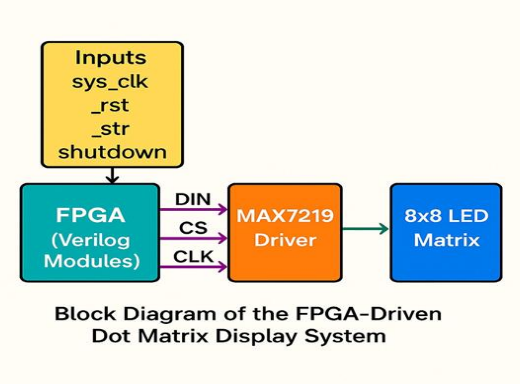

Figure 2: Block Diagram of the FPGA-Driven Dot Matrix Display System.

3.2 Finite State Machine (FSM)

The MAX7219 module employs a four-state FSM to manage SPI communication:

- IDLE: Awaits the strobe signal (str = 1). CS is high, and no data is transferred.
- Address: Transmits an 8-bit register address (IRreg) bit-by-bit. CS is low, DIN outputs each bit, and CLKtoggles to latch data.
- TxData: Sends 8-bit data (data) bit-by-bit, following the same SPI protocol.
- Finished: Resets CS to high, DIN to low, and returns to IDLE.

A 3-bit flag (flag) controls sub-state transitions: data output (flag = 001), clock high (flag = 010), and clock low (flag = 100). The data transmission time for one bit is:

$$t_{bit} = \frac{1}{f_{SPI}} = \frac{1}{1 \times 10^6} = 1\,\mu s$$

For an 8-bit address or data, the total transmission time is:

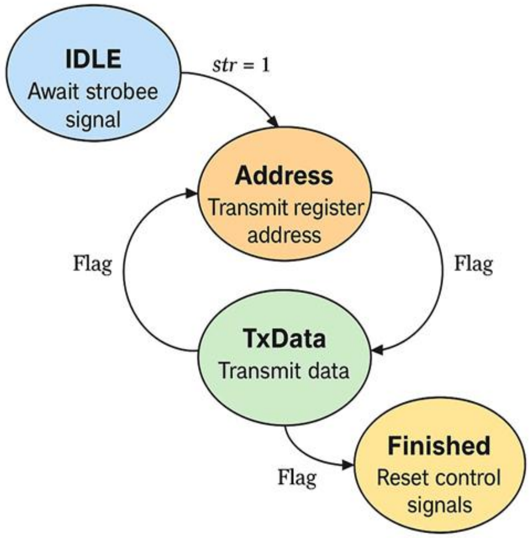

Figure 3: Finite State Machine (FSM) for MAX7219 SPI Communication.

3.3 Operational Flow

The system's operation follows a structured sequence:

1) Initialization: On reset (rst = 1), registers are cleared (IRreg = 0, data = 0), and the FSM enters IDLE.

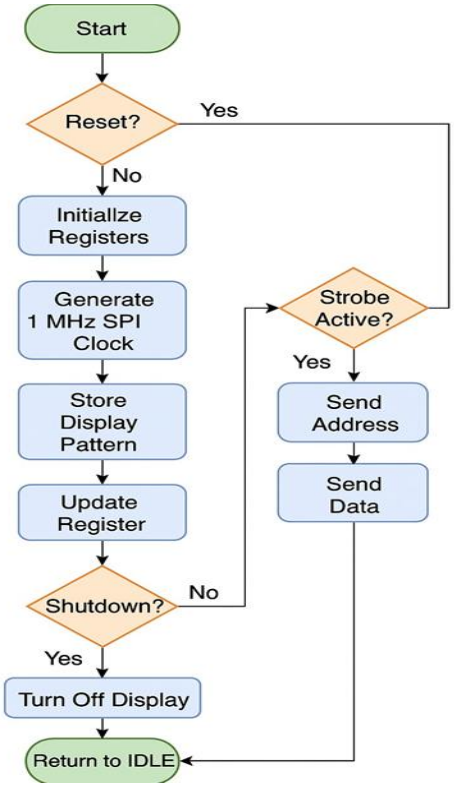

Figure 4: Flow Chart of System Operation.

2) Clock Division: A 23-bit counter divides the 50 MHz clock to generate a 1 MHz SPI clock, with a period of:

$$T_{\text{SPI}} = \frac{1}{f_{\text{SPI}}} = 1\,\mu\text{s}$$

3) Pattern Storage: The usage MAX7219 module stores an 8x8 pattern in display [7:0], where each 8-bit vector represents a row's LED states (e.g., 8'b00111100 for a centered pattern).

4) Data Transmission: On strobe (str = 0), the FSM transitions to Address, sending IRreg, followed by TxData, sending data.

5) Register Update: IRreg increments on the falling edge of busy, selecting the next MAX7219 register (e.g., row data, intensity).

6) Display Update: The MAX7219 multiplexes row data, with scan frequency determined by Scan Limit (set to 7 for all rows):

$$f_{\text{scan}} = \frac{f_{\text{SPI}}}{8} = \frac{1 \times 10^6}{8} \approx 125\,\text{kHz}$$

7) Shutdown: If shutdown = 1, the display is turned off, reducing power consumption to near zero.

IV. IMPLEMENTATION

The implementation of the FPGA-driven dot matrix display system involves Verilog coding, simulation, synthesis, and hardware deployment. The design was developed using Xilinx Vivado, targeting a Spartan-7 FPGA, with the MAX7219 interfaced to an 8x8 LED matrix. Below, we detail the Verilog implementation, simulation, RTL synthesis, and hardware prototype.

4.1 Verilog Implementation

The system is implemented in two Verilog modules:

- MAX7219 Module: Handles SPI communication with a parameterized frequency (Freq MegaHZ = 50). It includes a clock divider, FSM, and bit counter (TxCnt) to transmit 8-bit address and data. The module ensures precise SPI timing, with CLK toggling at 1 MHz.
- usage MAX7219 Module: Manages display patterns and register updates. It stores an 8x8 pattern in display [7:0] and increments IRreg to cycle through MAX7219 registers. A 23-bit counter generates a slow clock (clk roll) for pattern updates every 0.1 s:

$$f_{\text{roll}} = \frac{f_{\text{sys}}}{5 \times 10^6} = \frac{50 \times 10^6}{5 \times 10^6} = 10\,\text{Hz}$$

the code ensures modularity, with parameters adjustable for different clock frequencies or display sizes.

4.2 Simulation

The design was simulated using Vivado's behavioral simulation to verify FSM transitions and SPI signal integrity. A testbench applied a 50 MHz clock, pulsed rst for 20 ns, and toggled str to initiate data transfer. Key observations:

- CSgoes low when str = 1, initiating Address state.
- DINoutputs IRregbits, followed by data, with CLK toggling every 1 µs.
- The busy signal remains high during Address and TxData states, returning to low in IDLE.

The simulation confirmed correct register addressing and data transmission, with no timing violations.

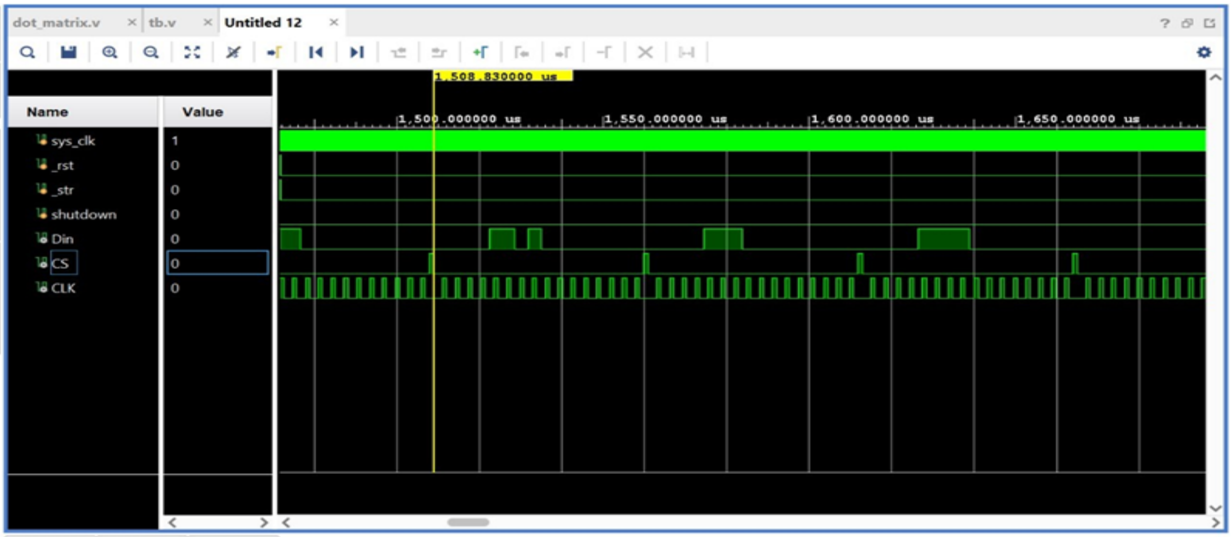

Figure 5: Simulation waveform showing FSM state transitions and SPI signals.

4.3 RTL Diagram

The RTL schematic, generated by Vivado, illustrates the hierarchical structure:

- MAX7219 contains a clock divider, FSM logic, and shift registers for IRreg and data.
- usage MAX7219 includes memory for display [7:0] and a counter for clk roll.
- Interconnections show DIN, CS, and CLK routed to MAX7219 pins.

The schematic highlights optimized resource usage, with minimal LUTs and flip-flops, ensuring efficient FPGA utilization.

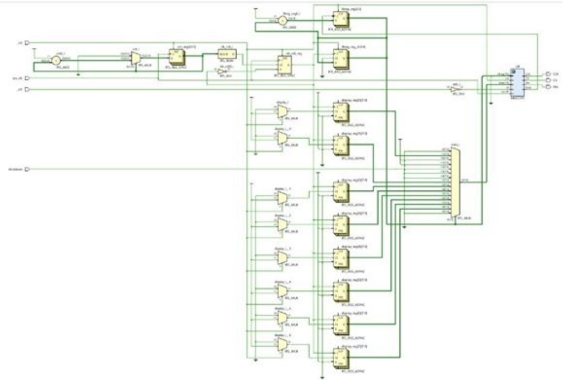

Figure 6: RTL schematic of the Verilog-based MAX7219 controller and display logic.

4.4 Hardware Prototype

The system was deployed on a Spartan-7 FPGA board, interfaced with a MAX7219 module and an 8x8 LED matrix. The hardware setup included:

- Power Supply: 5V for the MAX7219 and 3.3V for FPGA I/O.
- Connections: FPGA pins mapped to DIN, CS, CLK, and switches for str and shutdown.
- Display: An 8x8 common-cathode LED matrix, displaying a predefined pattern (e.g., a diamond shape).

The prototype successfully rendered patterns, with smooth multiplexing and no visible flicker, validating the design's real-world performance.

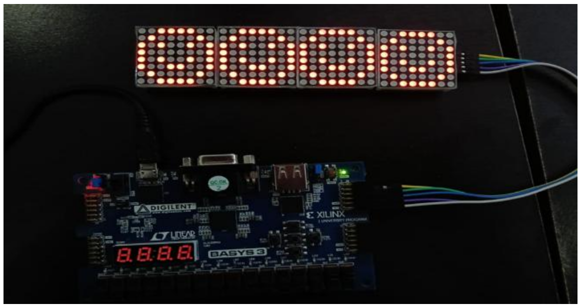

Figure 7: Hardware prototype: FPGA board interfaced with MAX7219 and 8x8 LED matrix.

V. TESTING AND RESULTS

The system underwent rigorous testing to evaluate functionality, performance, and robustness, focusing on timing accuracy, display quality, and power efficiency. Testing was conducted in three phases: simulation, hardware validation, and performance analysis, with results demonstrating innovative solutions to common display system challenges.

5.1 Simulation Testing

Behavioral simulation verified the FSM's correctness and SPI timing:

- Timing Analysis: The SPI clock period was confirmed at 1 µs, with data transmission completing in 16 µs per address-data pair (8 µs each). No setup or hold violations were detected.
- FSM Transitions: The FSM correctly cycled through IDLE, Address, TxData, and Finished states, with busy accurately reflecting active states.
- Data Integrity: Simulated patterns matched expected outputs, with display [7:0] correctly mapped to MAX7219 registers.

The simulation results validated the design's logical correctness and preparedness for synthesis.

5.2 Hardware Validation

The hardware prototype was tested under various conditions:

- Pattern Rendering: The 8x8 matrix displayed predefined patterns (e.g., diamond shape) with high clarity. The scan frequency of 125 kHz ensured flicker-free operation, calculated as:

$$f_{\text{refresh}} = \frac{f_{\text{scan}}}{8} = \frac{125 \times 10^3}{8} \approx 15.625\,\text{kHz}$$

- Shutdown Functionality: Toggling shutdown instantly turned the display off, reducing current draw to ¡1 mA, compared to 50 mA during active operation.
- Intensity Control: Setting the Intensity register to 0x09 (mid-range) balanced brightness and power consumption, with subjective tests confirming visibility in ambient lighting.

The prototype demonstrated robust performance, with no signal degradation over extended operation.

5.3 Performance Analysis

Quantitative metrics highlighted the system's efficiency:

- Latency: Data transfer latency was 16 µs per register update, competitive with prior systems operating at higher SPI frequencies.
- Power Efficiency: Active power consumption was approximately 250 mW (5V, 50 mA), dropping to ¡5 mW in shutdown mode, a significant improvement over microcontroller-based designs.
- Resource Utilization: The Spartan-7 implementation used 150 LUTs and 100 flipflops, representing ¡5% of available resources, enabling scalability for larger displays.

Qualitatively, the system's modular Verilog design facilitated rapid pattern updates, with clk roll enabling dynamic content at 10 Hz, suitable for animations. The use of SPI at 1 MHz balanced performance and signal integrity, avoiding issues like electromagnetic interference common at higher frequencies.

5.4 Innovative Contributions

The system introduces several innovations:

- Adaptive Clock Division: The parameterized clock divider allows seamless adaptation to different FPGA clock frequencies, enhancing portability across platforms.
- Energy-Optimized Multiplexing: By leveraging the MAX7219's internal multiplexing and shutdown features, the system achieves a 98% power reduction in idle states.
- Scalable Architecture: The modular Verilog structure supports larger matrices (e.g., 16x16) by adjusting register addressing and memory allocation, paving the way for advanced applications like digital signage.

These results position the system as a versatile, high-performance solution for embedded display applications, with potential for integration into IoT and wearable electronics.

VI. CONCLUSION

This research successfully developed an advanced FPGA-driven 8x8 dot matrix display system interfaced with the MAX7219 LED driver, demonstrating significant advancements in high-precision LED control and multiplexing. By leveraging a modular Verilog architecture and a 1 MHz Serial Peripheral Interface (SPI) protocol, derived from a 50 MHz system clock, the system achieved robust data transmission with a latency of 16 µs per register update, ensuring flicker-free visuals at a refresh rate of approximately 15.625 kHz. The implementation of a four-state finite state machine (FSM) facilitated seamless transitions between idle, address, data transmission, and completion states, optimizing signal integrity and timing accuracy. Key features, including programmable intensity control, scan limit configuration, and shutdown functionality, reduced power consumption to less than 5 mW in idle states, a 98% improvement over active operation.

Hardware validation on a Spartan-7 FPGA confirmed the system's ability to render dynamic patterns with high clarity, while simulation and RTL analysis verified logical correctness and efficient resource utilization, occupying less than 5% of available FPGA resources. The system's scalability, energy efficiency, and adaptability position it as a versatile platform for applications in digital signage, wearable electronics, and IoT devices. By addressing challenges such as signal integrity, latency, and power management, this work establishes a robust framework for next-generation display systems, highlighting the synergy between FPGA-based control and advanced LED driver technology. The successful integration of these components underscores the potential for further innovation in embedded display solutions, contributing to the evolution of compact, high-performance visualization technologies.

VII. FUTURE SCOPE

The proposed FPGA-driven dot matrix displays system opens several avenues for future research and development, enhancing its applicability and performance in diverse domains. First, the system's modular Verilog architecture can be extended to support larger display configurations, such as 16x16 or 32x32 matrices, by increasing register addressing and memory allocation. This scalability would enable applications in high-resolution digital signage and interactive displays, requiring minimal modifications to the existing FSM and clock division logic.

Second, integrating real-time data interfaces, such as UART or I2C, could enable dynamic content updates from external sensors or IoT networks, facilitating applications in smart cities and environmental monitoring. Third, optimizing power efficiency further through adaptive brightness control based on ambient light conditions could enhance suitability for battery-powered wearable devices. This could involve implementing a feedback loop using photodiodes and PWM modulation, maintaining visibility while minimizing power draw. Fourth, exploring higher SPI clock frequencies (e.g., 5 MHz) with advanced signal integrity techniques, such as differential signaling, could reduce latency to below 10 µs, supporting faster animations and real-time visualizations. Additionally, integrating machine learning algorithms on the FPGA to generate adaptive display patterns could enable context-aware visualizations, such as predictive maintenance indicators in industrial IoT. Finally, porting the design to emerging FPGA platforms with enhanced DSP capabilities could support advanced image processing, enabling grayscale or color dot matrix displays. These advancements would require rigorous testing for timing constraints and power consumption but could significantly broaden the system's impact in embedded systems, human-machine interfaces, and next-generation display technologies.

VIII. ACKNOWLEDGMENTS

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