

Physics of Microprocessor Operation: From MOSFETs to Quantum-Scale Limits

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Abstract—Microprocessors are the core of modern computing systems, but their performance is fundamentally governed by semiconductor-device physics rather than just architecture. This paper reviews the physics of CMOS microprocessors, focusing on MOSFET operation, scaling laws, power dissipation mechanisms, and emerging short channel and quantum effects that limit traditional scaling. We show that classical “Moore like” scaling is approaching fundamental limits posed by leakage currents, power density, and quantum tunneling, motivating new device concepts such as FinFETs, 2D channel materials, and quantum inspired chips. The analysis highlights how microprocessor design has become an applied branch of solid state and quantum physics.

I. INTRODUCTION

A microprocessor is an integrated circuit (IC) that integrates a central processing unit (CPU) on a single chip, executing instructions from a stored program. Modern microprocessors contain billions of MOS (metal oxide semiconductor) transistors built in CMOS (complementary MOS) technology, where n-type and p-type MOSFETs form logic gates and memory cells.^{[1][2]}

The continuous improvement in processor speed and density has followed Moore’s Law, which roughly states that the number of transistors on a chip doubles every two years. However, this scaling is driven by physical constraints in semiconductor devices, such as charge-transport properties, dielectric-thickness limits, and quantum effects at atomic scales.^{[3][1]}

This paper examines microprocessors from a physics perspective, addressing:

- how MOSFETs work as switches,
- how scaling affects power and performance,
- and what quantum-scale phenomena are emerging at advanced technology nodes.^{[1][3]}

II. SEMICONDUCTOR PHYSICS BACKGROUND

2.1. Energy bands and doping

In a semiconductor, electrons occupy energy bands separated by a band gap. In intrinsic silicon, the Fermi level lies near mid-gap. Doping introduces impurities (e.g., phosphorus for n-type, boron for p-type), shifting the Fermi level and creating majority carriers (electrons or holes). This control of carrier concentration is the basis of all active devices in microprocessors.^[1]

2.2. p–n junction and MOS capacitor

The p–n junction forms the core of diodes and is embedded in many device structures. Under bias, it either blocks or conducts current depending on the direction of the applied voltage. The MOS capacitor, made of a metal (or poly-Si) gate, an insulating oxide, and a semiconductor body, is the building block of MOSFETs. Applying a gate voltage modulates the surface charge, creating an inversion layer that becomes the conducting channel.^{[2][3][1]}

III. MOSFETS AND CMOS GATES IN MICROPROCESSORS

3.1. MOSFET device physics

A MOSFET is a voltage-controlled field-effect device with source, drain, gate, and body terminals. In a p-type substrate, applying a sufficiently positive gate voltage creates an n-type inversion layer between heavily doped n⁺ source and drain regions.^{[4][2]}

The threshold voltage V_{th} is approximately given by

$$V_{th} \approx \phi_{ms} + 2\phi_F + \frac{Q_{ox} + Q_B}{C_{ox}},$$

where ϕ_{ms} is the metal–semiconductor work-function difference, ϕ_F is the bulk Fermi potential, Q_B is the

body charge, Q_{ox} is oxide charge, and C_{ox} is the gate oxide capacitance.^{[2][3]}

In the saturation region, the drain current for a long-channel nMOS transistor is modeled by

$$I_D \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2,$$

where μ_n is electron mobility, W is channel width, and L is channel length.^{[3][2]}

3.2. From MOSFETs to logic gates

CMOS logic is built by combining nMOS and pMOS transistors. For example, a CMOS inverter uses an nMOS and a pMOS in series between supply (V_{DD}) and ground; when the input is high, the nMOS conducts and the pMOS cuts off, pulling the output low, and vice versa. Similar combinations form NAND and NOR gates, which are the basis of arithmetic and control logic in microprocessors.^[1]

IV. PHYSICS OF SCALING, POWER, AND PERFORMANCE

4.1. Scaling and Moore's Law

As technology nodes shrink (e.g., from 130 nm to 7 nm), L , W , and t_{ox} (oxide thickness) decrease, increasing transistor density and switching speed. Scaling also reduces the gate delay, roughly proportional to RC , where R is channel resistance and C is gate capacitance.^{[3][1]}

However, as L and t_{ox} become extremely small, quantum tunneling through the oxide and into the channel increases leakage current, which does not scale down as quickly as dynamic power.^{[5][3]}

4.2. Dynamic and static power

The dynamic power consumed by a logic gate is given by

$$P_{dyn} \approx \alpha C V_{DD}^2 f,$$

where α is the activity factor (fraction of transitions per clock cycle), C is load capacitance, V_{DD} is supply voltage, and f is clock frequency. Bringing L down allowed lowering V_{DD} to keep P_{dyn} reasonable, but leakage currents (sub-threshold and gate-tunneling) add a static power term P_{static} that grows with integration density.^{[5][3][1]}

High power density leads to significant heating, requiring advanced thermal management and limiting maximum operating frequency.^[1]

4.3. Short-channel effects

When L becomes comparable to the depletion width, the channel is no longer fully controlled by the gate. This leads to short-channel effects such as:

- Drain-induced barrier lowering (DIBL): The drain potential screens the gate, lowering the effective barrier and reducing V_{th} .^[3]
- Velocity saturation: Carrier velocity saturates at high electric fields, limiting the current gain from further scaling.^[3]

These effects break the square-law model and require more sophisticated device models (e.g., BSIM family) in microprocessor design and simulation.^{[6][5]}

V. QUANTUM-SCALE LIMITS AND EMERGING DIRECTIONS

5.1. Quantum tunneling and variability

At advanced nodes (sub-5 nm), the gate oxide and channel dimensions become only a few atomic layers thick. Quantum-mechanical tunneling of electrons through the oxide and into the channel becomes significant, increasing leakage and reducing reliability.^{[5][3]}

Furthermore, atomic-scale variations in dopant distribution and interfaces cause statistical variability in V_{th} and mobility, making tight control of device behavior difficult.^{[5][3]}

5.2. New device architectures

Several non-planar and alternative-material structures are being explored:

- FinFETs: Fin-shaped channels provide better gate control from two or three sides, improving short-channel immunity.^{[5][1]}
- SOI (Silicon-on-Insulator): A buried oxide layer reduces parasitic capacitance and leakage.^[1]
- 2D channel materials (e.g., transition-metal dichalcogenides, TMDs): These atomically thin semiconductors offer high mobility and electrostatic control at ultrathin dimensions.^{[5][1]}

5.3. Quantum-inspired and photonic microprocessors

Recent work integrates quantum-scale phenomena into processor-like chips. For example, "quantum

microprocessor chips” have been demonstrated using photonic circuits and quantum-like states to simulate molecules or solve special-purpose problems. These chips still operate at conventional temperatures but use quantum interference and superposition in photonic or superconducting elements to go beyond classical MOSFET-only logic.^{[7][5]}

VI. DISCUSSION

Microprocessors are no longer just “computer architecture” objects; they are complex systems whose performance is dominantly governed by solid-state and quantum physics. The transition from macroscopic MOS capacitors to atomic-scale channels has shifted the design focus from purely circuit-level optimization to device-physics and materials-engineering problems.^{[3][1]}

Classical CMOS scaling is now constrained by:

- leakage currents due to tunneling,
- variability at atomic scales, and
- power-density and thermal limits.^{[3][5]}

Future microprocessor development will therefore rely on a combination of new device geometries (FinFETs, GAA), new materials (2D semiconductors, high-κ dielectrics), and non-classical computing paradigms (quantum-inspired, photonic, neuromorphic).^{[7][1][5]}

VII. CONCLUSION

This paper has shown that the operation and evolution of microprocessors are deeply rooted in semiconductor-device physics. From the MOS capacitor and MOSFET through scaling laws and power-dissipation models to quantum-scale leakage and variability, each step limits how fast and dense classical CMOS chips can become.^{[1][3]}

As traditional scaling reaches its fundamental limits, physics-driven device innovation such as FinFETs, 2D materials, and quantum-inspired architectures will define the next generation of microprocessors. Understanding these physical principles is essential for students and researchers aiming to push the boundaries of computing technology.^{[7][5][1]}

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