Low-Power ECG-on-Chip System Using FPGA and Verilog HDL

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***Abstract*—Electrocardiogram (ECG) monitoring is essential for diagnosing heart-related diseases; however, conventional ECG machines are bulky and consume high power, making them unsuitable for portable and wearable applications. This work presents a low-power ECG-on-chip system designed using Verilog HDL and implemented on an FPGA platform. The proposed system performs real-time ECG signal processing and extracts vital features such as QRS complexes and heart rate. Leveraging the parallel processing capability and reconfigurability of FPGA technology, the system achieves improved performance and flexibility compared to microcontroller-based approaches. Low-power techniques such as clock gating and optimized resource utilization are applied to reduce energy consumption while maintaining signal accuracy. The proposed ECG-on-chip architecture is suitable for wearable healthcare devices, remote patient monitoring, and portable medical electronics.**

***Index Terms*—ECG, FPGA, Verilog HDL, QRS Detection, Low Power Design, Biomedical Signal Processing**

I. INTRODUCTION

The Electrocardiogram (ECG) is a widely used diagnostic tool for monitoring the electrical activity of the human heart. It plays a crucial role in detecting abnormalities such as arrhythmias, irregular heartbeats, and myocardial infarctions. With the increasing prevalence of cardiovascular diseases worldwide, continuous ECG monitoring has become increasingly important.

Traditional ECG systems are often large, expensive, and power-hungry, restricting their use to hospitals and clinical environments. The growing demand for portable and wearable healthcare devices necessitates compact, energy-efficient ECG systems capable of real-time analysis.

Field Programmable Gate Arrays (FPGAs) offer a promising solution for biomedical signal processing due to their parallel processing capability, reconfigurability, and high-speed operation. Using Verilog HDL, ECG signal processing algorithms can be efficiently implemented in hardware while maintaining low power consumption.

II. BACKGROUND

Recent advancements in FPGA technology have enabled the development of real-time ECG processing systems with reduced power consumption. FPGA-based designs outperform traditional microcontroller systems by executing multiple operations concurrently. Low-power design techniques such as clock gating and optimized arithmetic operations further enhance system efficiency.

III. OBJECTIVES AND SCOPE

The primary objective of this project is to design and implement a low-power ECG-on-chip system using FPGA and Verilog HDL. The key objectives include:

- Real-time ECG signal acquisition and processing
- Accurate QRS detection and heart rate calculation
- Reduced power consumption for wearable applications
- Scalable and modular hardware architecture

The primary objective of this research is to design and implement a low-power, real-time ECG-on-chip system using FPGA technology and Verilog HDL.

The system aims to achieve efficient cardiac signal processing suitable for modern wearable healthcare applications. The detailed objectives are as follows:

- Real-Time ECG Signal Acquisition and Preprocessing

To develop a robust hardware interface for continuous acquisition of ECG signals and perform preprocessing operations such as noise filtering, baseline wander removal, and signal normalization. The system is designed to handle real-time data streams with minimal latency, ensuring accurate representation of cardiac activity.

- Efficient Digital Signal Processing Architecture

To implement optimized digital signal processing (DSP) techniques on FPGA, including filtering and feature extraction, while ensuring minimal resource utilization. The architecture focuses on parallel processing capabilities of FPGA to enhance throughput and performance.

- Accurate QRS Complex Detection

To design and implement a reliable QRS detection algorithm (such as threshold-based or derivative-based methods) in hardware for precise identification of R-peaks. This enables accurate segmentation of ECG signals and forms the basis for further cardiac analysis.

- Heart Rate Estimation and Analysis

To compute heart rate in real time by calculating the R–R interval between successive QRS complexes. The system aims to provide consistent and accurate heart rate measurements under varying signal conditions.

- Low-Power Hardware Design for Wearable Applications

To optimize the design for reduced power consumption by employing techniques such as clock gating, efficient resource mapping, and minimized switching activity. This ensures suitability for battery-operated and wearable medical devices.

- Scalable and Modular System Architecture

To develop a modular design approach where individual components (signal acquisition, filtering, QRS detection, and heart rate calculation) can be independently modified or upgraded. This enhances system flexibility and future scalability.

- FPGA-Based Implementation and Validation

To implement the complete system on an FPGA platform and validate its performance in terms of accuracy, latency, power consumption, and hardware utilization.

IV. LITERATURE SURVEY

Several studies have explored FPGA-based ECG processing systems. Silvestri et al. implemented a low-power QRS extractor on FPGA using the Pan–Tompkin's algorithm optimized for reduced DSP switching activity [1]. Gon and Mukherjee proposed a folded lifting-based discrete wavelet transform architecture for R-peak detection, minimizing hardware resources [2]. Kripa and Jebastine introduced a simplified FPGA-based arrhythmia detection system using peak envelope extraction [3]. Desai et al. presented a low-latency ECG characterization system using Hermite polynomials [4]. Kasture et al. demonstrated FPGA-based LMS adaptive filtering to eliminate power-line interference in ECG signals [5].

V. METHODOLOGY

The ECG signal is acquired using surface electrodes and conditioned through amplification and analog filtering. The conditioned signal is digitized using an ADC and processed on FPGA using Verilog HDL modules. Digital filtering removes noise and baseline drift, followed by QRS detection and heart rate calculation. Low-power techniques such as clock gating and efficient resource utilization are employed to minimize energy consumption.

The proposed ECG-on-chip system follows a structured signal processing pipeline consisting of acquisition, preprocessing, feature extraction, and output generation.

The analog ECG signal acquired from surface electrodes typically has an amplitude range of 0.5 mV to 5 mV and is highly susceptible to noise such as power-line interference (50/60 Hz), baseline wander, and muscle artifacts. To address this, signal conditioning is performed using an instrumentation amplifier followed by bandpass filtering.

The filtered analog signal is digitized using an Analog-to-Digital Converter (ADC) with appropriate sampling frequency (typically 250–500 Hz). The digitized

signal is then processed on the FPGA.

ECG Electrodes
□
Signal 2
□
ADC (Analog-to-Digital)
□
FPGA Processing Module
↓
Output / UART / Display

Digital Filtering

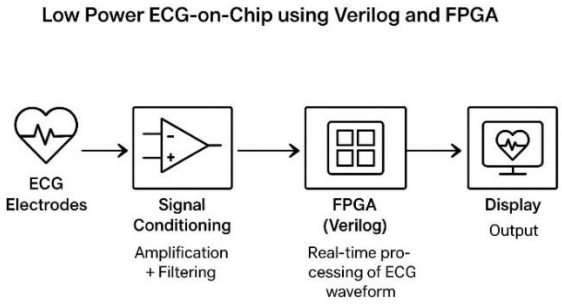
A digital bandpass filter is implemented to remove:

- Baseline drift (low-frequency noise)
- High-frequency noise

The filter can be represented as:

$$y[n] = \sum_{k=0}^{M} b_k\, x[n-k] - \sum_{k=1}^{N} a_k\, y[n-k]$$

where $x[n]$is input signal and $y[n]$is filtered output.



[1] Fig. 1. Block diagram of the proposed ECG-on-chip system architecture

VI. DESIGN AND IMPLEMENTATION

The ECG processing system is implemented on an FPGA using Verilog HDL. The design is divided into several functional modules to simplify development and improve efficiency.

The preprocessing unit is responsible for filtering the input signal. The feature extraction unit identifies important characteristics such as QRS complexes. A control unit manages the overall operation, while a communication module enables data transfer to external devices.

The use of pipeline architecture ensures that multiple stages of processing occur simultaneously, improving system throughput. FPGA's inherent parallelism helps in achieving faster performance compared to traditional software-based approaches.

VII. RESULT AND DISCUSSION

The implemented system successfully acquires and processes ECG signals in real time. The output waveform clearly displays the P, QRS, and T components of a normal ECG signal. The FPGA-based implementation demonstrates reliable performance with reduced power consumption, validating the feasibility of low-power ECG-on-chip systems.

The system is implemented using Verilog HDL on an FPGA platform. The design follows a modular architecture consisting of:

- Preprocessing Module – performs filtering
- Feature Extraction Module – detects QRS complex
- Control Unit – manages data flow
- Communication Module – UART transmission

FPGA Advantages

- Parallel execution of multiple operations
- Reduced latency compared to software-based systems
- Reconfigurability for algorithm updates

Pipeline architecture is used to improve throughput, ensuring continuous ECG signal processing without delay.

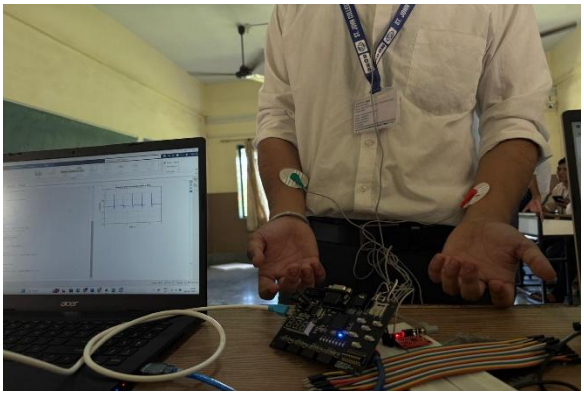


Fig. 2 The output ECG waveform is shown above

Fig.3 Illustrates the simulated ECG waveform obtained from the FPGA-based implementation. The waveform clearly shows periodic peaks corresponding to the electrical activity of the heart. The most

prominent peaks represent the QRS complexes, which are crucial for identifying heartbeats and calculating heart rate.

The smaller variations before and after the QRS peaks correspond to the P wave and T wave, representing atrial depolarization and ventricular repolarization respectively. The consistency and regularity of these waveforms indicate proper functioning of the signal processing pipeline.

It can be observed that noise and baseline drift have been effectively minimized due to the implemented digital filtering techniques. The output signal is smooth and well-defined, demonstrating the efficiency of the preprocessing stage.

Furthermore, the accurate detection of QRS peaks confirms the reliability of the feature extraction algorithm implemented on the FPGA. The system is capable of processing ECG signals in real time with minimal delay, owing to the parallel processing capability of FPGA architecture.

Overall, the simulation results validate that the proposed system achieves efficient ECG signal processing with reduced noise, accurate peak detection, and reliable heart rate estimation, making it suitable for portable and wearable healthcare applications

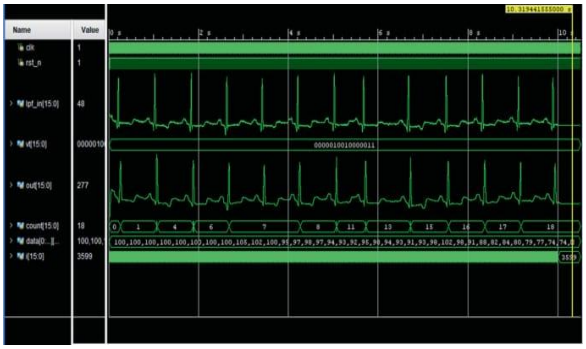


Fig 3. Simulated ECG output waveform obtained from FPGA implementation

VIII. FUTURE SCOPE

Future enhancement includes wireless connectivity multi lead ECG acquisition signal processing algorithms, wearable integration and compliance with medical certification standard. AI-Based Arrhythmia Detection: Implementation of a neural network-based arrhythmia classifier in Verilog using FPGA's DSP resources, enabling automated detection of atrial fibrillation, ventricular tachycardia, and other rhythm disorders. • On-Board LCD Display: Integration of a graphical LCD (SPI-based, e.g., ST7735) for standalone ECG display without PC connection, enhancing portability for point-of-care use. • ASIC Implementation: Migration of the verified Verilog design to an Application-Specific Integrated Circuit (ASIC) for ultra-low-power wearable applications, targeting sub-1 mW power consumption. • SD Card Data Logging: Implementation of an SPI-based SD card interface for local ECG data storage, enabling offline analysis and Holter-style 24-hour monitoring. • Signal Quality Indicator: Addition of a real-time signal quality assessment module that detects lead-off conditions, motion artifacts, and noisy signals, automatically alerting the user to poor recording quality. • Battery-Powered Operation: Design of a dedicated power management circuit using the FPGA's dynamic power management features to achieve battery-powered operation with run times exceeding 24 hours on a standard Li-ion cell

IX. CONCLUSON

This paper presents the design and implementation of a low-power ECG-on-chip system using FPGA and Verilog HDL. The proposed system successfully acquires and processes ECG signals in real time, enabling accurate detection of QRS complexes and reliable heart rate calculation.

The use of FPGA technology provides significant advantages such as parallel processing, reduced latency, and high computational efficiency compared to conventional microcontroller-based systems. Additionally, low-power design techniques such as clock gating and optimized resource utilization help in minimizing energy consumption, making the system suitable for portable and wearable healthcare applications.

The simulation results demonstrate that the system effectively removes noise and preserves important ECG features, ensuring accurate signal analysis. The clear identification of ECG waveform components validates the performance of the proposed design.

Overall, the developed ECG-on-chip system offers a compact, efficient, and scalable solution for real-time biomedical signal processing and has strong potential for future integration into advanced healthcare monitoring devices.

REFRENCES

[1] J. Pan and W. J. Tompkins, "A real-time QRS detection algorithm," IEEE Trans. Biomed. Eng., vol. BME-32, no. 3, pp. 230–236, 1985.
[2] S. Silvestri et al., "FPGA implementation of a low-power QRS extractor for ECG analysis," IEEE Trans. Instrum. Meas., vol. 67, no. 5, pp. 1156–1165, 2018.
[3] A. Kasture et al., "FPGA adaptive filter for power line interference removal in ECG signal," in Proc. IEEE ICSPC, 2019, pp. 1–5.
[4] S. P. Kripa and R. M. Jebastine, "FPGA-based design for detecting cardiac dysrhythmias," Procedia Comput. Sci., vol. 171, pp. 1842–1850, 2020.
[5] M. Desai et al., "Low-latency, low-power FPGA implementation of ECG characterization using Hermite polynomials," Biomed. Signal Process. Control, vol. 68, p. 102767, 2021.
[6] A. Gon and R. Mukherjee, "An efficient FPGA architecture for R-peak detection using lifting-based DWT," IEEE Access, vol. 10, pp. 5652–5663, 2022.
[7] MIT-BIH Arrhythmia Database, PhysioNet. [Online]. Available: https://physionet.org/content/mitdb/