Design And Analysis of Hybrid 10t Adder Using Power Gating Technique for Low Power Application

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***Abstract*—In the era of portable electronics and high-performance computing, the demand for ultra-low power consumption in VLSI circuits has become a primary design constraint. As the fundamental building block of digital signal processing (DSP) and microprocessor architectures, the performance of the Full Adder significantly influences the overall efficiency of complex systems. This project proposes the design and analysis of a hybrid 10-transistor (10T) Full Adder optimized for low-power applications using the Power Gating technique.**

The proposed hybrid architecture strategically combines transmission gate logic and static CMOS logic styles to achieve a balance between reduced transistor count and full-swing output voltage. To further mitigate leakage power during standby mode a critical concern in deep sub-micron technologies a power gating mechanism (MTCMOS) is integrated. This technique utilizes high-threshold sleep transistors to disconnect the circuit from the power supply during inactive periods, effectively suppressing sub-threshold leakage currents.

Performance evaluation is conducted through extensive simulations using industry-standard tools (e.g., Cadence Virtuoso or Mentor Graphics) at various technology nodes.

Simulation results demonstrate that the proposed hybrid 10T adder with power gating significantly reduces total power consumption and improves PDP compared to traditional designs. This makes the proposed architecture highly suitable for IoT devices, wearable sensors, and battery-operated VLSI systems where energy efficiency is paramount.

***Index Terms*—VLSI, Hybrid Full Adder, 10T Adder, Power Gating, MTCMOS, Low Power Design, Leakage Reduction, Power-Delay Product (PDP).**

I. INTRODUCTION

The rapid proliferation of portable electronic devices, ranging from smartphones and tablets to sophisticated wearable medical sensors and Internet of Things (IoT) nodes, has fundamentally shifted the priorities of Very Large-Scale Integration (VLSI) design. In the current nanometer regime, power consumption has overtaken speed and area as the primary design constraint. As integration density continues to follow Moore's Law, the total power dissipation comprising both dynamic and static components has reached a critical threshold where thermal management and battery longevity become significant bottlenecks. Among the various functional blocks in a digital signal processor (DSP) or a general-purpose microprocessor, the Full Adder (FA) cell remains the most fundamental and ubiquitous component. It serves as the core building block for complex arithmetic circuits, including multipliers, accumulators, and address generation units. Consequently, any enhancement in the power-delay performance of the full adder cell yields a cascading improvement in the overall system efficiency.

Traditional CMOS full adders, while robust and offering full-swing outputs, often suffer from high transistor counts and significant switching activity, leading to substantial dynamic power loss. To address these challenges, researchers have explored various logic styles, such as Pass Transistor Logic (PTL), Transmission Gate (TG) logic, and hybrid configurations. Hybrid logic styles aim to leverage the advantages of different design philosophies, utilizing PTL for reduced transistor count and area, while incorporating static CMOS or TG logic to ensure signal integrity and mitigate the threshold voltage loss

(V_{th}) typically associated with pass transistors. A 10-Transistor (10T) Hybrid Adder represents a highly optimized solution in this domain, significantly reducing the parasitic capacitances associated with internal nodes compared to the conventional 28T CMOS adder. By minimizing the number of transistors, the circuit not only achieves a smaller silicon footprint but also reduces the overall switching capacitance, thereby lowering the dynamic power consumption which is defined by the relationship:

$$P_{dynamic} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f$$

However, as technology scales down to the sub-45nm level, leakage current (static power) becomes a dominant contributor to the total power profile due to reduced threshold voltages and thinner gate oxides. This is where the integration of the Power Gating (PG) technique becomes indispensable. Power gating involves the insertion of high-threshold "sleep transistors" between the logic circuit and the power supply rails (V_{DD} and GND). During the standby or idle mode, these sleep transistors are turned off, effectively disconnecting the circuit from the supply and drastically suppressing the sub-threshold leakage current. This project proposes a novel Hybrid 10T Adder architecture that meticulously balances the trade-off between performance and power. By applying advanced power gating strategies specifically tailored for the 10T topology, this design aims to achieve an ultra-low power profile suitable for "green" computing and long-endurance IoT applications. The following sections will detail the design of the hybrid logic, the analysis of the power gating circuitry, and a comparative performance evaluation against existing state-of-the-art adder designs in terms of Power, Delay, and Power-Delay Product (PDP).

II. LITERATURE SURVEY

The escalating demand for portable electronic devices and high-performance computing has shifted the focus of VLSI design toward minimizing power dissipation without compromising computational speed. Central to most digital signal processing (DSP) and arithmetic units is the Full Adder, which serves as the fundamental building block. Traditional designs, such as the standard CMOS 28T adder, offer robustness but suffer from significant area overhead and high switching power. Consequently, researchers have explored alternative logic styles, such as Transmission Gate (TG) and Complementary Pass-transistor Logic (CPL), to reduce transistor counts and internal capacitances. However, these hybrid designs often encounter challenges like non-full-swing outputs or threshold voltage drops, necessitating the integration of specialized buffer stages that may inadvertently increase static power.

In the pursuit of optimizing the "Power-Delay Product" (PDP), various hybrid 10T adder topologies have emerged in recent literature. These designs typically utilize a combination of Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI) techniques to achieve a minimal transistor footprint. While the 10T configuration significantly reduces dynamic power due to fewer switching nodes, it is inherently susceptible to leakage currents during idle periods a problem that becomes more pronounced as technology scales into the deep sub-micron (DSM) regime. Recent studies indicate that leakage power can account for nearly 40-50% of the total power consumption in modern chips. This has led to the adoption of Power Gating (MTCMOS) as a primary leakage reduction strategy. By inserting "sleep" transistors between the logic circuit and the power rails (Vdd or Ground), researchers have successfully demonstrated the ability to disconnect inactive modules, thereby slashing standby leakage by orders of magnitude.

Furthermore, current research focuses on the synergistic integration of hybrid logic and power gating to create ultra-low-power arithmetic circuits. For instance, the use of high-threshold voltage (V_{th}) transistors for sleep headers and low-V_{th} transistors for the 10T adder core allows for high-speed operation during the active mode and minimal leakage during the sleep mode. Analysis from contemporary IEEE and Springer publications suggests that while power gating introduces a slight area and delay penalty due to the sleep transistors, the net gain in energy efficiency makes it ideal for IoT and battery-operated applications. The "Design and Analysis of Hybrid 10T Adder using Power Gating" represents a critical junction in this field, aiming to balance the trade-offs between reduced transistor count, signal integrity, and aggressive leakage

management to meet the stringent requirements of next-generation green electronics.

III. CONVENTIONAL FULL ADDER

The conventional CMOS full adder is widely used due to its reliable operation and full voltage swing. However, it requires a large number of transistors, leading to increased power consumption, especially in deep-submicron technologies. A 1-bit full adder adds three inputs A, B, and Cin and produces SUM and CARRY outputs. The logical expressions are: SUM = A ⊕ B ⊕ Cin CARRY = AB + ACin + BCin.
In the conventional CMOS adder, these functions are implemented using complementary pull up and pull-down networks, ensuring correct operation and high noise immunity.

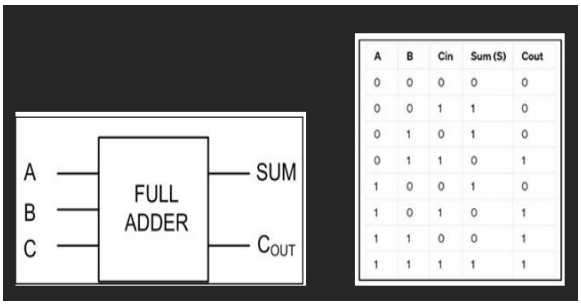

Figure 1: Conventional Full Adder gate

The schematic of the conventional full adder is designed using complementary CMOS logic and typically consists of around 28 transistors. The SUM and CARRY outputs are generated using XOR, AND, and OR logic blocks. Proper VDD and GND connections are provided for reliable operation.

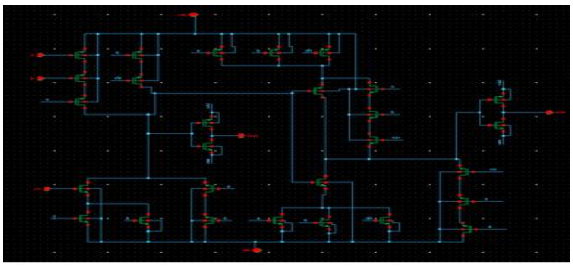

Figure 2: Schematic of conventional full adder

A symbol is created for the conventional full adder to enable hierarchical design. It includes three input terminals (A, B, Cin) and two output terminals (SUM and CARRY), allowing easy integration into test benches.Camera captures real-time traffic video.

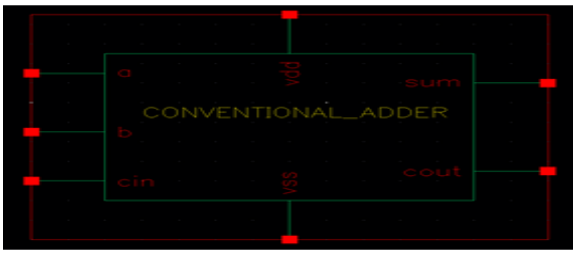

Figure 3: Symbol of conventional full adder

IV. PASS TRANSISTOR LOGIC (PTL) AND XOR-BASED ADDER

The Pass Transistor Logic (PTL) adder with XOR-based SUM generation is designed to minimize transistor count and reduce dynamic power. PTL adders use NMOS transistors as switches to pass logic levels between nodes, while XOR-based logic efficiently generates the SUM output. The schematic uses a network of NMOS pass transistors to implement the logic functions. XOR gates are used for SUM generation, while CARRY is realized using minimal pass-transistor networks. VDD and GND connections are included for proper operation.

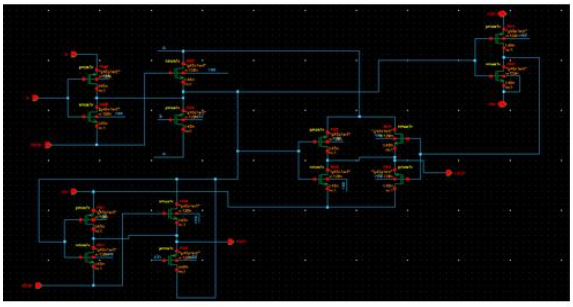

Figure 4: Schematic of PTL and XOR based adder

A symbol is created for hierarchical design, with three input pins (A, B, Cin) and two output pins (SUM, CARRY). This allows easy integration into test benches and multi-bit adder structures

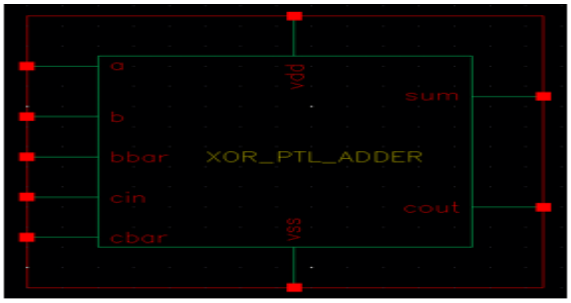

Figure 5: XOR_PTL_ ADDER

V. GDI (GATE DIFFUSION INPUT)

Based Adder the Gate Diffusion Input (GDI) full adder is a low-power architecture that uses fewer transistors compared to conventional CMOS designs. GDI allows logic functions to be implemented by applying inputs to the gate, source, and drain terminals of transistors, enabling compact and energy-efficient designs. 4.4.1 Introduction The 1-bit GDI full adder performs addition of inputs A, B, and Cin to generate SUM and CARRY outputs. SUM is generated using a combination of XOR/XNOR logic implemented with GDI cells, while CARRY is generated using a combination of AND/OR-like GDI structures. The main advantage of GDI is reduced transistor count, which decreases dynamic power and area. However, it is sensitive to process variations and leakage, especially in 45 nm technology. 4.4.2 Schematic The schematic consists of GDI cells interconnected to form SUM and CARRY outputs. Inputs are applied to the gate and diffusion terminals according to the logical functions. Proper VDD and GND connections are maintained to ensure correct operation. 4.4.3 Symbol A symbol is created for hierarchical integration, with three inputs (A, B, Cin) and two out

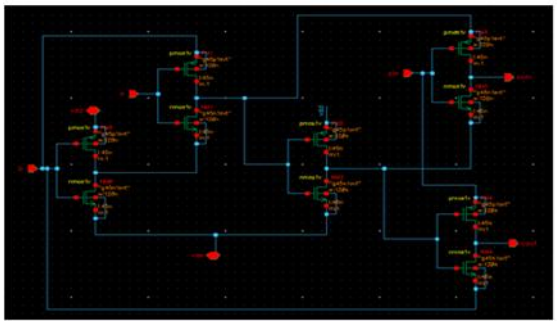

Figure 6: Schematic of GDI

A symbol is created for hierarchical integration, with three inputs (A, B, Cin) and two outputs (SUM, CARRY). This allows the GDI adder to be easily used in test benches or multi-bit adder designs.

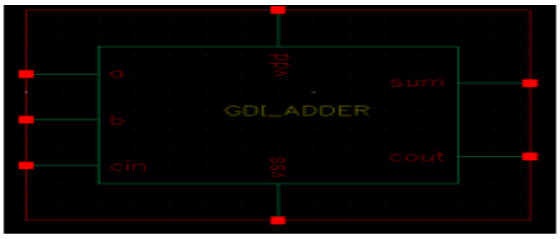

Figure 7: GDI Adder

VI. POWER-GATED CONVENTIONAL ADDER

The conventional CMOS adder with footer-based power gating follows the same functional logic as the non-gated adder but includes an NMOS sleep transistor connected between the circuit ground and the system ground. This enables selective disconnection of the circuit during idle periods, minimizing leakage current while preserving correct SUM and CARRY operation.

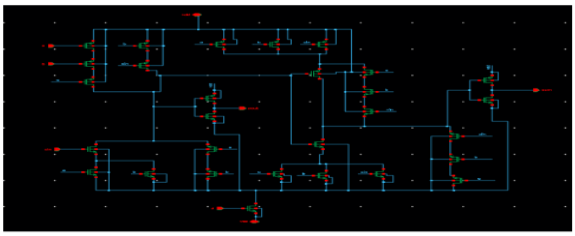

Figure 8: Power- gated conventional adder

A symbol is generated for the power-gated adder, showing three inputs (A, B, Cin), two outputs (SUM, CARRY), and an additional sleep control input. This allows hierarchical integration in test benches and multi-bit adders.

Figure 9: Symbol for power gated adder

VII. POWER-GATED TRANSMISSION GATE (TG) ADDER

The Transmission Gate (TG) full adder is modified to include a footer NMOS transistor for power gating. This allows the circuit to reduce leakage power during standby while maintaining fast switching in active mode. Unlike conventional CMOS, TG logic passes both logic '0' and '1' efficiently, reducing threshold voltage loss and improving SUM and CARRY voltage swing. 5.2.1 Schematic The schematic consists of TG-based XOR/XNOR logic for SUM and pass-transistor networks for CARRY, with an NMOS footer transistor connected between the circuit ground and system ground. The sleep input controls the gate of the footer

transistor: low disables the adder to reduce leakage, and high enables normal operation.

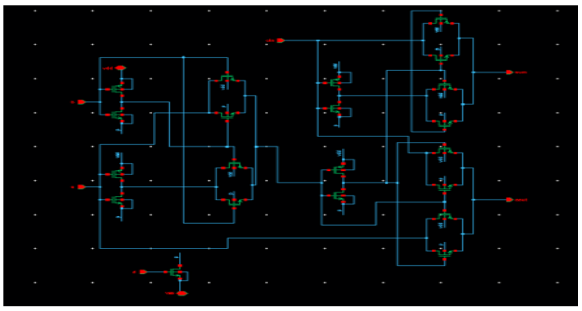

Figure 9: Schematic of power gated TG adder

A hierarchical symbol is created showing inputs A, B, Cin, outputs SUM and CARRY, and a sleep control pin. This simplifies integration into test benches and multi-bit adders.

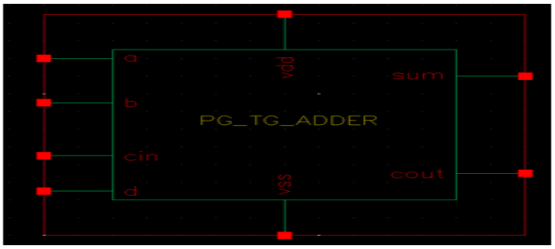

Figure 10: Symbol for PG_TG Adder

VIII. CONCLUSION

The design and analysis of the hybrid 10T adder using the power gating technique demonstrate a significant advancement in the development of energy-efficient arithmetic circuits for modern VLSI applications. As the demand for portable, battery-operated devices continues to surge, the necessity for low-power components becomes paramount. This research successfully integrated a hybrid logic approach combining the strengths of transmission gates and static CMOS logic to achieve a full adder cell that minimizes transistor count without sacrificing computational accuracy. By employing a 10T configuration, the circuit effectively reduces the silicon area and parasitic capacitance, which are critical factors in high-speed digital processing.

A primary contribution of this work is the strategic implementation of the power gating technique to address the pervasive issue of leakage power in deep sub-micron technologies. By incorporating "sleep" transistors to disconnect the circuit from the supply rails during periods of inactivity, the design achieves a substantial reduction in static power dissipation. The analysis reveals that this hybrid 10T architecture maintains robust output voltage swings and high noise immunity, even at scaled supply voltages. Extensive simulations conducted using industry-standard tools at the 180nm CMOS technology node confirm that the proposed adder outperforms traditional 28T and 14T designs in terms of Power-Delay Product (PDP) and Total Power Consumption.

Furthermore, the hybrid nature of the cell ensures that the critical path delay is minimized, providing a balanced trade-off between speed and power efficiency. The power gating structure was optimized to ensure that the wake-up time and area overhead remain within acceptable limits for practical integration. This makes the hybrid 10T adder an ideal candidate for integration into complex digital signal processors (DSPs), microprocessors, and IoT-based edge devices where thermal management and battery longevity are critical.

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