Design and Performance Evaluation of 2-Stage OPAMP with Nulling Resistor and Miller Capacitance

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***Abstract*—Frequency compensation is one of the most critical steps in designing a stable CMOS operational amplifier, and this work takes a close look at how two different compensation strategies perform in practice. Specifically, we compare conventional Miller compensation against an enhanced version that adds a nulling resistor in series with the Miller capacitor, both implemented in a two-stage CMOS op-amp using 180 nm CMOS technology. Simulations were carried out in Cadence Virtuoso under a 1.8 V supply with a 2 pF load. The results show that the nulling-resistor design achieves a phase margin of 77.43°—a substantial improvement over the 45.86° seen in the basic Miller design—while keeping the DC gain fixed at 70 dB and CMRR around 73.6 dB. The gain-bandwidth product also goes up, from 75 MHz to 83 MHz. Taken together, these numbers confirm that the series resistor eliminates the troublesome right-half-plane zero that the Miller capacitor would otherwise introduce, and that this translates directly into better closed-loop stability at virtually no extra power cost.**

***Keywords*—Two-stage op-amp, Miller compensation, Nulling resistor, Phase margin, CMRR, Gain-bandwidth product, CMOS analog design.**

I. INTRODUCTION

The operational amplifier is one of the most versatile building block in analog circuit design. From precision filters and data converters to biomedical sensor interfaces and instrumentation front-ends, nearly every analog system depends on the op-amp's ability to deliver stable, predictable gain across frequency. The performance proves that matter most is open-loop gain, bandwidth, phase margin, slew rate, and quiescent current ,each have a direct relation on how the surrounding system behaves, which is why op-amp design is still one of the important part.[12].

Of the many topologies available, the two-stage CMOS op-amp continues to be widely used because it packs a lot of gain and output swing into a relatively compact, understandable circuit. The drawback is that cascading two gain stages creates at least two significant poles in the open-loop frequency response. Close a feedback loop around that structure without doing something about those poles, and you risk instability. The standard fix is Miller compensation: connect a capacitor between the output of the second stage and the internal high-impedance node, and rely on the Miller multiplication effect to create a dominant pole that pushes everything else to higher frequencies [1].

Miller compensation does the job of stabilizing the amplifier, but it also have got it's own issues. The same capacitor that creates the dominant pole also provides a direct, feed-forward current path around the output transistor. At a certain frequency, the current fed forward through the capacitor cancels the transistor's own output current, creating a zero in the right-half plane. Unlike a left-half-plane zero, an RHP zero adds phase lag rather than lead—exactly the opposite of what you want when trying to maintain margin at the unity-gain bandwidth [3]. Inserting a resistor in series with the Miller capacitor, known as a nulling resistor, is a clean and practical way to move this problematic zero away from the sensitive crossover region, or eliminate it altogether.

This paper presents a simulation-based comparison of the two compensation approaches, carried out under identical bias and process conditions in 180 nm CMOS. The metrics we examine include DC gain, bandwidth, gain-bandwidth product, phase margin, CMRR, slew rate, and static power, giving a comprehensive picture of how the two topologies stack up.Phase margin is the number that most directly captures closed-loop stability behaviour. It tells you how many degrees of extra phase the amplifier can lose before the loop hits the −180° instability threshold, measured right at the unity-gain frequency. A margin of 45° is often cited as the minimum acceptable value, but most practical

designs aim for 60° or more to stay safe across process spread and temperature variation [12]. The GBW—defined as the frequency where the open-loop gain magnitude reaches 0 dB—is equally important, since it sets the speed at which the closed-loop system can respond. The challenge is that the two metrics are coupled: pushing GBW higher tends to eat into phase margin, and that trade-off is what makes the nulling resistor particularly appealing.

II. LITERATURE SURVEY

Razavi's textbook [12] provides perhaps the most thorough treatment of frequency compensation in CMOS amplifiers, walking through how the number, location, and magnitude of poles and zeros are shaped by the choice of compensation network. That foundation makes it clear why Miller compensation became the default solution for two-stage designs. Banik et al. [2] demonstrated a high-performance low-power two-stage OPAMP in 90 nm CMOS for biomedical applications, highlighting how the choice of compensation directly affects both bandwidth and power—particularly relevant when the load and process differ from textbook assumptions. Ashwin Kumar [3] further reinforced this by applying the Miller theorem analytically to two-stage compensated op-amps, quantifying exactly how the RHP zero erodes phase margin in closed-loop operation.

Ahuja [9] proposed an alternative approach that sidesteps the RHP zero entirely by routing the compensation feedback current through a cascode transistor rather than directly through the capacitor. The technique is effective, but it addstransistors and complicates the bias network. Allen and Holberg [11] demonstrated a simpler path to the same result: placing a resistor in series with the compensation capacitor gives the designer direct control over where the zero lands, and with the right resistance value it can be pushed into the left half-plane where it actively helps phase margin rather than hurting it.

Barik and Ramkumar [4] extended this line of work to cardiovascular signal acquisition, designing a low-noise, micro-power two-stage CMOS op-amp where careful compensation is essential to preserve signal integrity in the sub-hertz to kilohertz biomedical band. Anand and Gautam [5] provided a comparative survey of compensation methods for two-stage OTAs, confirming that the nulling-resistor approach consistently outperforms plain Miller compensation in phase margin without a meaningful increase in power. Harb and Zabroda [6] examined indirect compensation under large-load conditions, showing that when the load capacitance is large the standard Miller scheme degrades more severely and alternative topologies become necessary. Palmisano and Palumbo [7] proposed a current-buffer-based compensation strategy that eliminates the RHP zero through a fundamentally different mechanism, offering a useful counterpoint to the resistive nulling approach studied here. Alam Chowdhury et al. [8] tackled two-stage op-amp design in 100 nm CMOS with a focus on minimizing offset voltage, reinforcing that compensation interacts with matching and must be considered alongside device sizing. Vimala et al. [10] presented a direct predecessor to the present work, implementing a two-stage Miller-compensated op-amp with a nulling resistor in 90 nm technology and demonstrating phase margin improvement consistent with the results reported here. Despite this body of work, side-by-side simulation studies comparing the two approaches under matched 180 nm process conditions are not common in the literature, which is the gap this paper aims to fill.

A. Two-Stage CMOS Op-Amp Architecture and Gain

A conventional two-stage CMOS operational amplifier is composed of two cascaded amplification stages to achieve high voltage gain. The input stage consists of a differential pair (M1, M2) loaded by a PMOS current mirror (M3, M4), which converts the input voltage difference into a current at a high-impedance node. Due to the large resistance at this node, even a small current variation produces a significant voltage swing.The second stage operates as a common-source amplifier, where M6 provides additional voltage amplification and M7 acts as a bias current source. The overall open-loop gain is determined by the multiplication of the gains of both stages. Using small-signal analysis, the gain expression can be written as:

$$A_v = \frac{2g_{m2}g_{m6}}{I_{D5} \cdot I_{D6} \cdot (\lambda_n + \lambda_p)}$$

From this relation, it is evident that higher gain can be achieved either by increasing transconductance or by reducing channel-length modulation effects. In practical CMOS processes, longer channel devices are often used to reduce λ. The obtained gain of

approximately 70 dB aligns with expected values for a 180 nm implementation.

B. Small-Signal Transfer Function and Pole-Zero Distribution

The frequency response of the compensated amplifier can be modeled using a second-order system with one zero:

$$A(s) = -A_v \cdot \frac{(1 - s/z_1)}{(1 + s/|p_1|)(1 + s/|p_2|)}$$

The dominant pole $p_1$is located at the output of the first stage, where the effective capacitance is significantly increased due to Miller compensation. This pole can be approximated as:

$$p_1 \approx -\frac{1}{g_{m6} R_{out1} R_{out2} C_C}$$

The non-dominant pole $p_2$appears at the output node and is defined by:

$$p_2 = -\frac{g_{m6}}{C_L}$$

The unity-gain bandwidth is governed by the input stage parameters and compensation capacitor:

$$g_{m1} = 2\pi \cdot GBW \cdot C_C$$

To maintain sufficient stability, the second pole must be positioned well beyond the unity-gain frequency, leading to the condition:

$$g_{m6} \geq 2.2 \cdot g_{m1} \cdot \left(\frac{C_L}{C_C}\right)$$

C. Miller Compensation and Pole Separation

Frequency compensation is achieved by introducing a capacitor between the output and input of the second stage. This capacitor, known as the Miller capacitor, modifies the frequency response by exploiting the gain of the second stage. Due to the Miller effect, the capacitance seen at the first-stage output is effectively increased:

$$C_{eff} = C_C(1 + g_{m6} R_{out2})$$

This enlarged capacitance shifts the dominant pole toward lower frequencies, while the second pole is pushed further away. This phenomenon, referred to as pole splitting, ensures that the amplifier behaves as a single-pole system near the unity-gain frequency, thereby improving stability. To guarantee sufficient separation between poles, the compensation capacitor must satisfy:

$$C_C > 0.22 C_L$$

D. Right-Half-Plane Zero and Its Impact

While Miller compensation stabilizes the amplifier, it introduces an unintended feed-forward path through the capacitor. This creates a right-half-plane (RHP) zero, which is given by:

$$z_1 = \frac{g_{m6}}{C_C}$$

Unlike left-half-plane zeros, an RHP zero contributes additional phase lag, thereby degrading stability. It also increases the gain magnitude at higher frequencies, which can shift the unity-gain crossover point and further reduce phase margin.

The phase reduction due to this zero can be approximated as:

$$\phi \approx -\tan^{-1}\left(\frac{\omega}{z_1}\right)$$

As a result, the phase margin of a Miller-compensated amplifier is often limited to around 45°, as observed in practical designs.

E. Effect of Nulling Resistor on Zero Location

To address the limitations caused by the RHP zero, a resistor is placed in series with the compensation capacitor. This modification alters the impedance of the feedback path and changes the zero location:

$$z_1 = \frac{1}{C_C\left(\frac{1}{g_{m6}} - R_z\right)}$$

Depending on the value of R_z, the zero behavior varies:

- $R_z < 1/g_{m6}$: zero remains in RHP but shifts to higher frequency
- $R_z = 1/g_{m6}$: zero is eliminated
- $R_z > 1/g_{m6}$: zero moves to LHP When the zero is placed in the left-half-plane, it introduces phase lead, which helps counteract the lag from the second pole. This results in a significant improvement in phase margin. Since no DC current flows through this branch, the resistor does not influence biasing or DC gain.

F. Phase Margin and Stability Trade-Off

Phase margin is defined as the difference between 180° and the phase angle of the open-loop response at the unity-gain frequency. It can be approximated as

$$PM \approx 180° - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{|z_1|}\right)$$

The sign of the zero term depends on whether it lies in the RHP or LHP.

The gain-bandwidth product is expressed as:

$$GBW = \frac{g_{m1}}{2\pi C_C}$$

In conventional Miller compensation, increasing bandwidth tends to reduce stability because the unity-gain frequency approaches the second pole and the RHP zero. The introduction of a nulling resistor resolves this issue by relocating the zero, allowing improved phase margin without sacrificing bandwidth.

Large-signal performance is determined by the slew rate:

$$I_{D5} = SR \cdot C_C$$

The power dissipation is given by:

$$P_{diss} = (I_{D5} + I_{D6})(V_{DD} + |V_{SS}|)$$

The common-mode rejection ratio (CMRR) depends primarily on device matching and current source characteristics, and remains unaffected by the compensation technique.

III. METHODOLOGY

The comparison in this work was structured around two otherwise identical op-amps. Both variants share the same transistor dimensions, bias currents, supply voltage (1.8 V), and load capacitance (2 pF); the only thing that differs is how the compensation network is implemented. This ensures that any difference in measured performance can be attributed squarely to the compensation topology and nothing else.

A. Miller Compensation Circuit - In the first variant, a single capacitor C_k is connected between the drain of M6 and the first-stage output node (the gate of M6). This is the classic Miller compensation arrangement. The capacitor exploits the voltage gain of the second stage to create a much larger effective capacitance at the first-stage output, forcing a dominant pole at low frequency and pushing the second pole well above the unity-gain crossing. The trade-off is the feed-forward RHP zero at $z = g_{m6}/C_k$, which limits how high the phase margin can actually be. The testbench and circuit schematic are shown in Fig. 1 and Fig. 2.

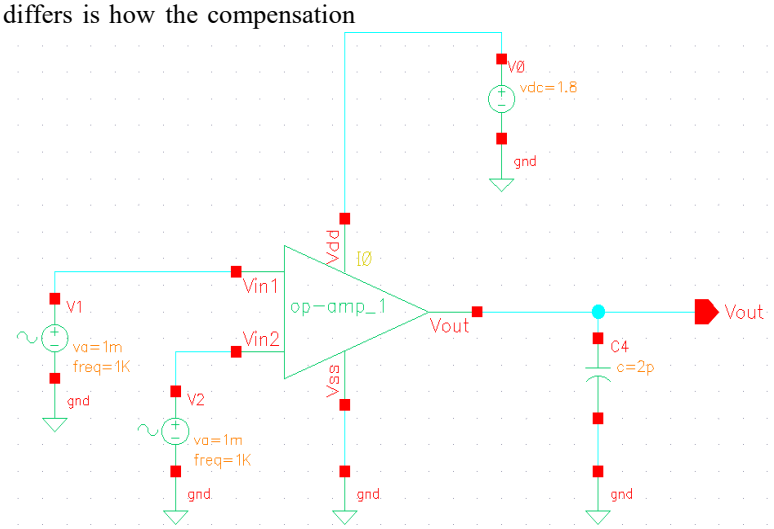

Fig. 1. Symbolic testbench — Miller compensation op-amp

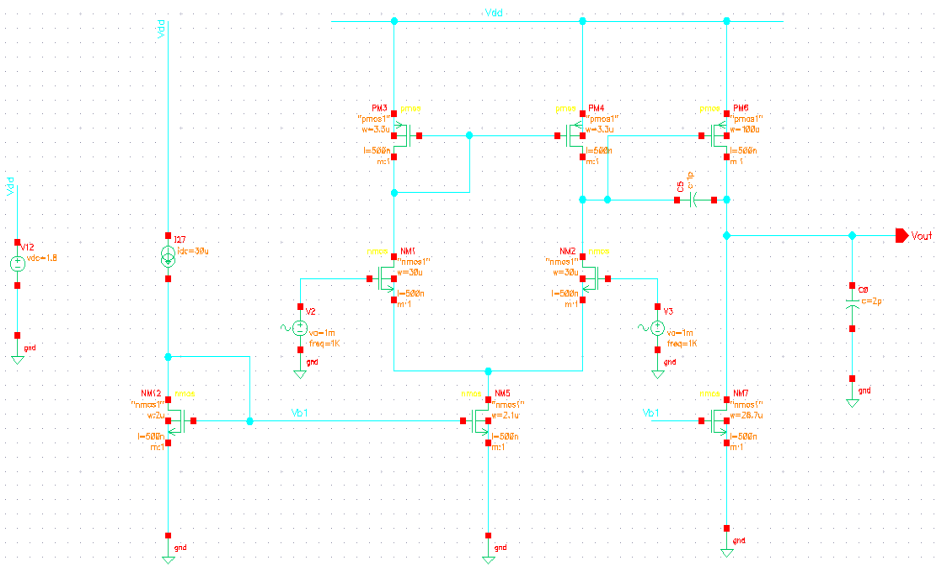

Fig. 2. Transistor-level schematic — Miller compensated op-amp

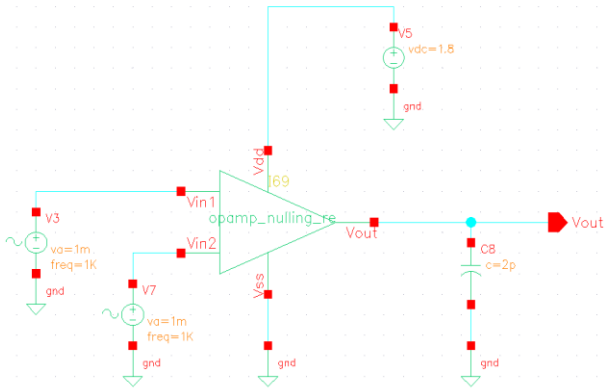

Fig. 3. Symbolic testbench — Nulling resistor compensated op-amp

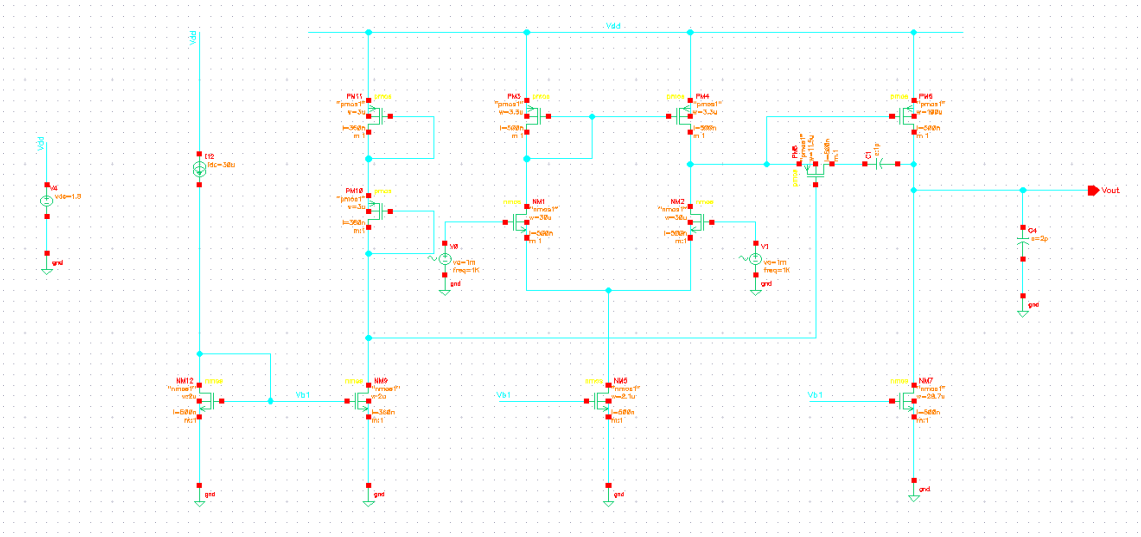

Fig. 4. Transistor-level schematic — Nulling resistor compensated op-amp

B. Nulling Resistor Compensation Circuit

The second variant adds a resistor R_2 in series with C_k. The RHP zero is now at $z = 1/[C_k(1/g_{m6} - R_2)]$, and by sizing R_2 appropriately the zero can be cancelled ($R_2 = 1/g_{m6}$) or moved into the LHP ($R_2 > 1/g_{m6}$). In either case, the detrimental phase lag caused by the zero in the baseline design is eliminated. The DC operating point is completely unaffected because R_2 carries no steady-state current. The testbench and schematic for this variant are shown in Fig. 3 and Fig. 4.

IV. DESIGN SPECIFICATIONS AND STEP-BY-STEP EQUATIONS

The design follows a structured 14-step transistor-sizing procedure. Table I lists the target specifications. All equations assume 180 nm TSMC CMOS: $V^{DD} = 1.8$ V, $V_{ss} = 0$ V, $K_n' = 270$ µA/V², $K_p' = 70$ µA/V², $V_{tn} = 0.5$ V, $|V_{tp}| = 0.5$ V, $\lambda_n = \lambda_p = 0.1$ V⁻¹.

TABLE I. TWO-STAGE OP-AMP DESIGN SPECIFICATIONS

Parameter	Symbol	Value
Open Loop Gain	Av	≥70 dB
Input CM Range	ICMR	0.9–1.6 V
Slew Rate	SR	30 V/µs
Gain Bandwidth	GBW	80 MHz
Load Capacitance	CL	2 pF
Comp. Cap. (theory)	CC	0.44 pF
Comp. Cap. (used)	CC	1 pF
Supply Voltage	VDD	1.8 V

A. Compensation Capacitor Selection

The theoretical lower bound on the compensation capacitor is $C_k = 0.22 \times C_l = 0.44$ pF. A value of 1 pF was used in practice to give extra stability margin and to keep the design robust under load variations, accepting the slight reduction in achievable bandwidth as a reasonable trade-off.

B. Design Steps for Op-Amp Frequency Compensation Using Miller Capacitor and Nulling Resistor

The two-stage op-amp is sized using a combined Miller and nulling-resistor compensation strategy, targeting both high gain and reliable stability. Miller compensation handles pole splitting and gain-bandwidth management, while the nulling resistor takes care of the RHP zero that the capacitor alone would introduce. The design is driven by five primary specifications: SR, Av, GBW, ICMR, and Pdiss.

Step 1: To obtain phase margin of 60°, place the right hand plane (RHP) zero at ten times greater than GBW.

$$CC > 0.22CL \tag{1}$$

$$p_2 = -\frac{gm_6}{cL} \tag{2}$$

$$Z_1 = \frac{gm_6}{Cc} \tag{3}$$

Step 2: Calculate ID5 to satisfy SR

$$ID_5 = SR.Cc \tag{4}$$

Step 3: Calculate the trans-conductance's of M1 and M2 (refer to Fig. 2 & Fig. 4) from Cc and GBW

$$gm1 = 2\pi \times GBW \times Cc \tag{5}$$

Step 4: Determine the aspect ratios of M1 and M2 based on the required transconductance.

$$\left(\frac{W}{L}\right)_{1,2} = \frac{(gm_1)2}{2K'n\ ID_1} \tag{6}$$

Step 5: Estimate M3 and M4 from maximum value of ICMR.

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2\ ID_3}{k'p[Vdd - ICMR(+) - |Vtp| + Vtn]^2} \tag{7}$$

Step 6: Determine the aspect ratios of M5 and M12

$$\left(\frac{W}{L}\right)_{5,12} = \frac{ID_5}{k'n[Vds_{5(sat)}]^2} \tag{8}$$

$$Vds_{5(sat)} = ICMR(-) - \sqrt{\frac{2ID_1}{k'n\left(\frac{W}{L}\right)_1}} - Vtn \tag{9}$$

Step 7: Determine the aspect ratio of M6

$$\left(\frac{W}{L}\right)_6 = \left[\left(\frac{W}{L}\right)_4 \left(\frac{gm_6}{gm_4}\right)\right] \tag{10}$$

Where,

$$gm_6 \geq 10gm_1 \tag{11}$$

$$gm_4 = \sqrt{2k'p\left(\frac{W}{L}\right)_4 ID_4} \tag{12}$$

Step 8: Calculate ID6 for required power dissipation.

$$ID_6 = \frac{(gm_6)2}{2k'p\left(\frac{W}{L}\right)_6} \tag{13}$$

Step 9: Estimate the aspect ratio of M7 to set the current ratio between ID6 and ID5.

$$\left(\frac{W}{L}\right)_7 = \left[\left(\frac{W}{L}\right)_5 \left(\frac{ID_6}{ID_5}\right)\right] \tag{14}$$

Step 10: To set VA = VB ensure that VSG10 is equal to VSG6.

$$\left(\frac{W}{L}\right)_{11} = \left[\left(\frac{W}{L}\right)_6 \left(\frac{ID_{11}}{ID_6}\right)\right] \tag{15}$$

Step 11: Set the aspect ratio of M10 to 1; the ratio ID10/ID5 determines aspect ratio of M9.

$$\left(\frac{W}{L}\right)_9 = \left[\left(\frac{W}{L}\right)_5 \left(\frac{ID_{10}}{ID_5}\right)\right] \tag{16}$$

Step 15: Determine the aspect ratio of M8.

$$\left(\frac{W}{L}\right)_8 = \frac{Cc}{Cc + CL}\sqrt{\frac{\left(\frac{W}{L}\right)_{10}\left(\frac{W}{L}\right)_6 ID_6}{ID_{10}}} \tag{17}$$

The resistor Rz is realized by the transistor M8, which is operating in the active region because the dc current through it is zero. Therefore, Rz can be written as

$$R_z = \frac{\partial Vds_8}{\partial ID_8} = \frac{1}{k'p\left(\frac{W}{L}\right)_8 (Vgs_8 - |Vtp|)} \tag{18}$$

At $Vds = 0$

Step 11: Evaluate Av and Pdiss.

$$Av = \frac{2gm_2gm_6}{ID_5.\ ID_6(\lambda n + \lambda p)} \tag{19}$$

$$Pdiss = (ID_5 + ID_6).(Vdd + |Vss|) \tag{20}$$

V. RESULTS AND DISCUSSION

A. Frequency Response — Miller Compensation

The Miller-only op-amp achieves a DC open-loop gain of 70 dB. At the unity-gain crossing (7 MHz), the Bode phase plot (Fig. 5) shows a phase margin of 45.86°. This is technically above the conditional stability threshold of 45°, but not by much. In a production context, that narrow margin would be a concern—any process shift, temperature change, or heavier load could push the design into instability.

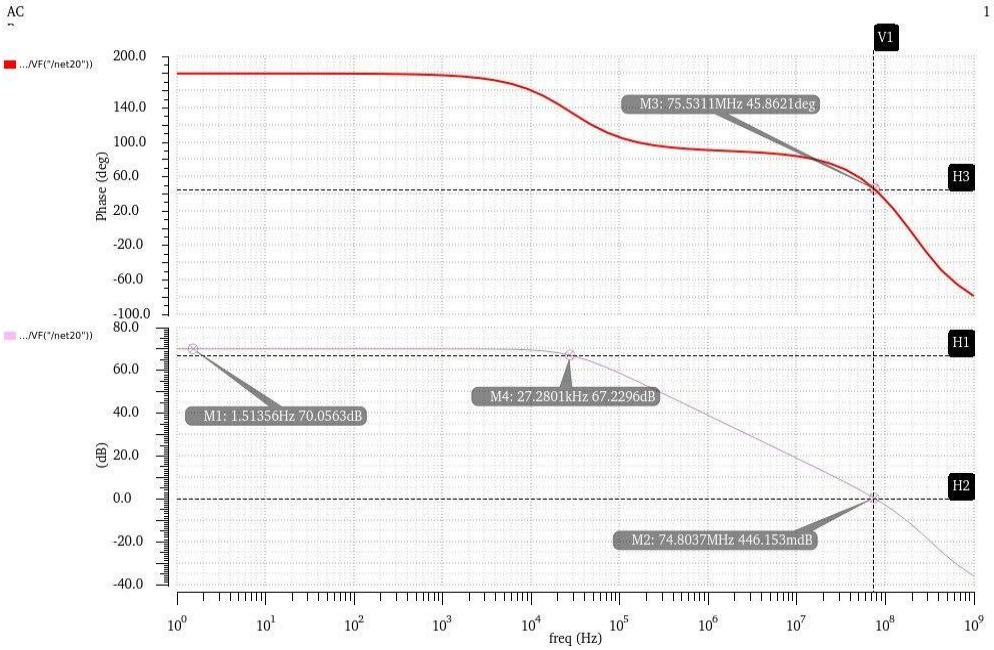

Fig. 5. Bode plot — Miller compensated two-stage op-amp (PM = 45.86°)

B. Frequency Response — Nulling Resistor

the nulling resistor added, the DC gain stays at 70 dB while the unity-gain bandwidth grows to 83 MHz. More importantly, the phase margin jumps to 77.43° (Fig. 6), which is 31.57° better than the baseline. This result directly validates the theoretical prediction that eliminating the RHP zero leads to a well-stabilized amplifier. The design is now comfortably inside the robust-stability zone.

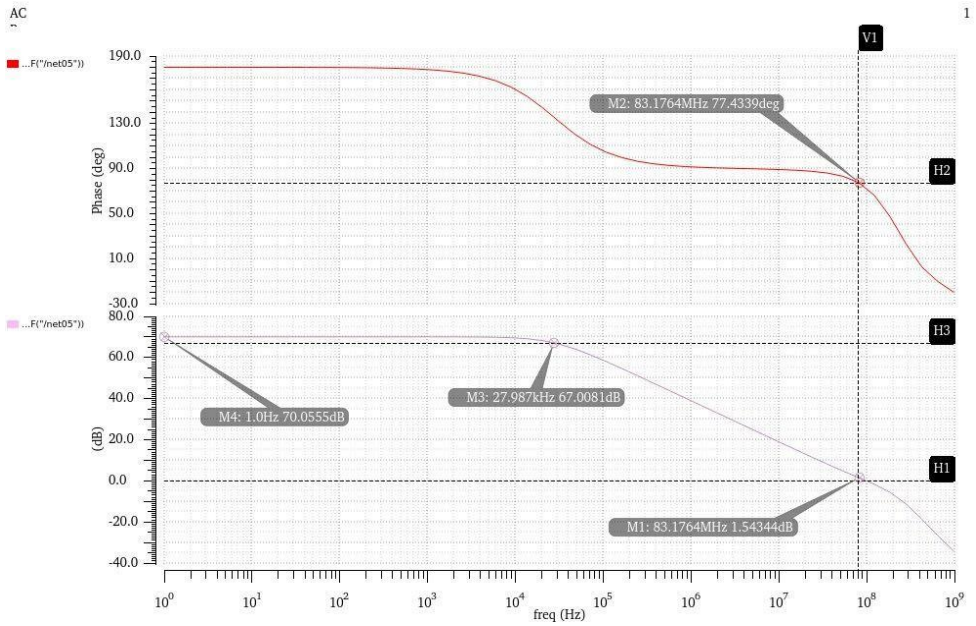

Fig. 6. Bode plot — Nulling resistor compensated op-amp (PM = 77.43°)

C. Differential Gain and Common-Mode Gain

Differential and common-mode gain plots for both designs are shown in Fig. 7 and Fig. 8. Both achieve a differential gain of 70 dB. The fact that the nulling resistor leaves the DC gain unchanged confirms an important theoretical point: R_r sits in the compensation branch and carries no bias current, so it has zero influence on the small-signal gain at DC.

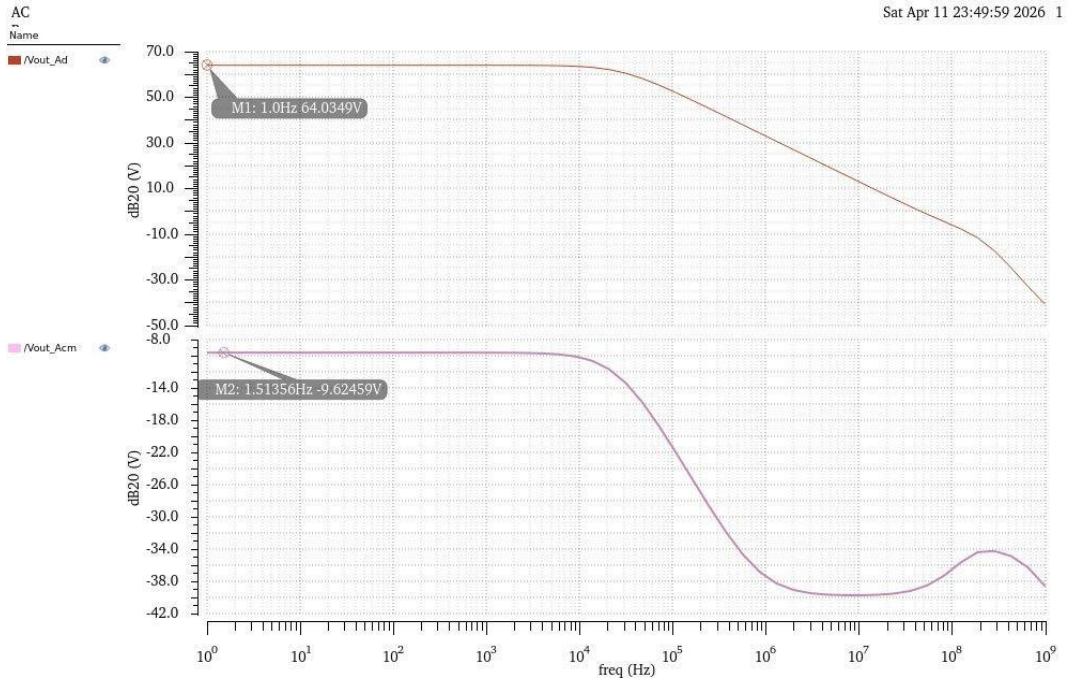

Fig. 7. Differential gain (Ad) and common-mode gain (ACM) — Nulling resistor

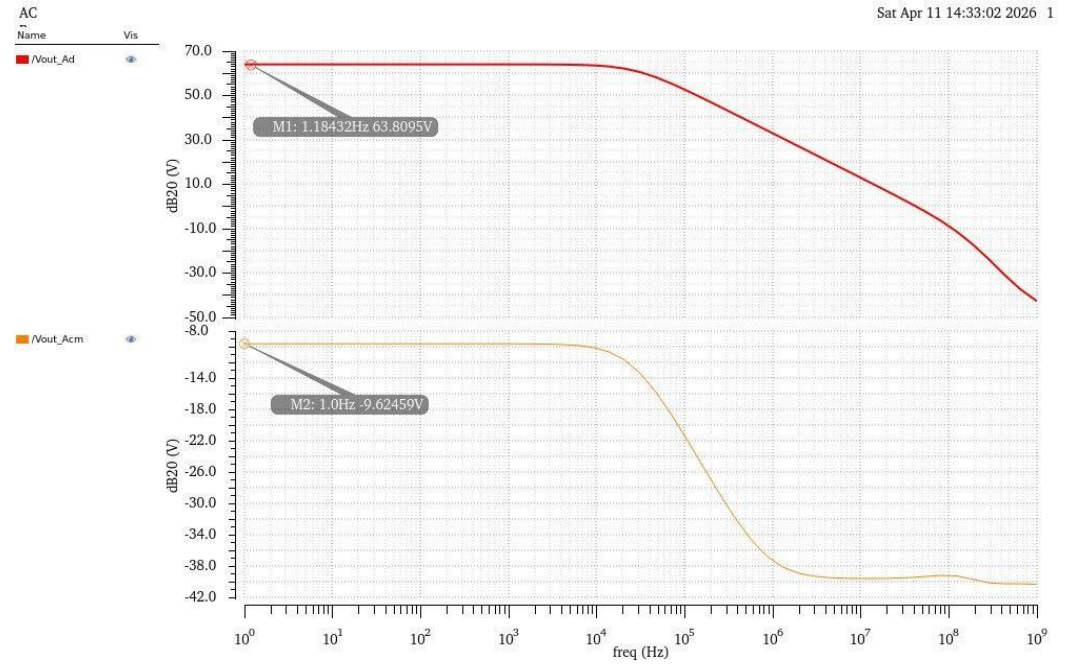

Fig. 8. Differential gain (Ad) and common-mode gain (ACM) — Miller compensation

D. CMRR Analysis

Figures 9 and 10 show the CMRR for each design. The Miller circuit records 73.6 dB; the nulling-resistor version records 73.69 dB—a difference of just 0.09 dB. This near-identical result is expected: CMRR is determined by the symmetry of the differential pair and the output impedance of the tail current source, neither of which changes between the two designs.

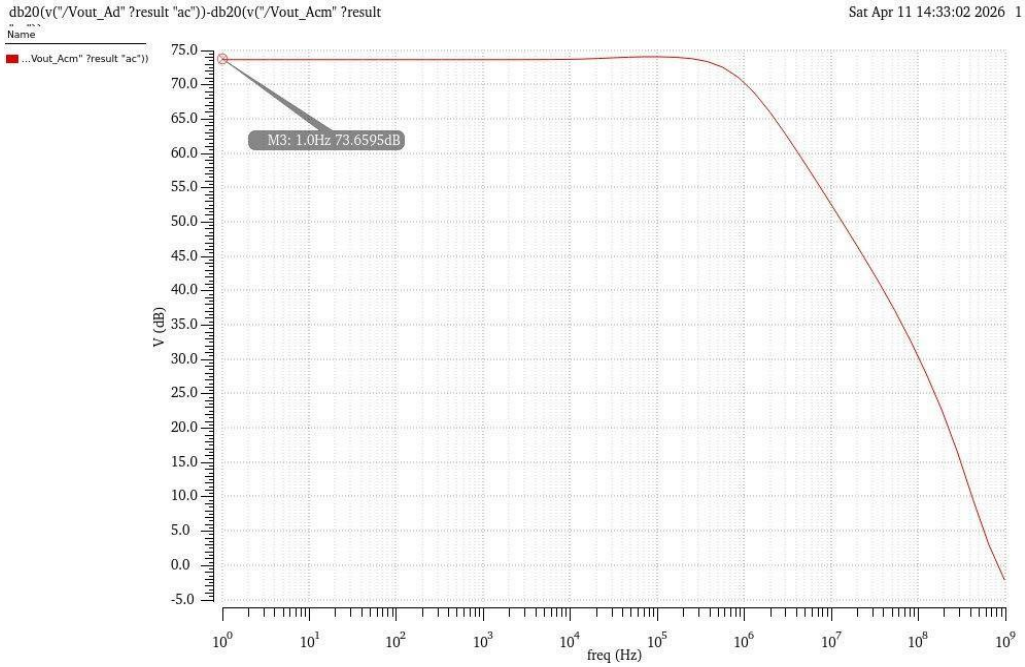

Fig. 9. CMRR — Miller compensated op-amp (73.6 dB)

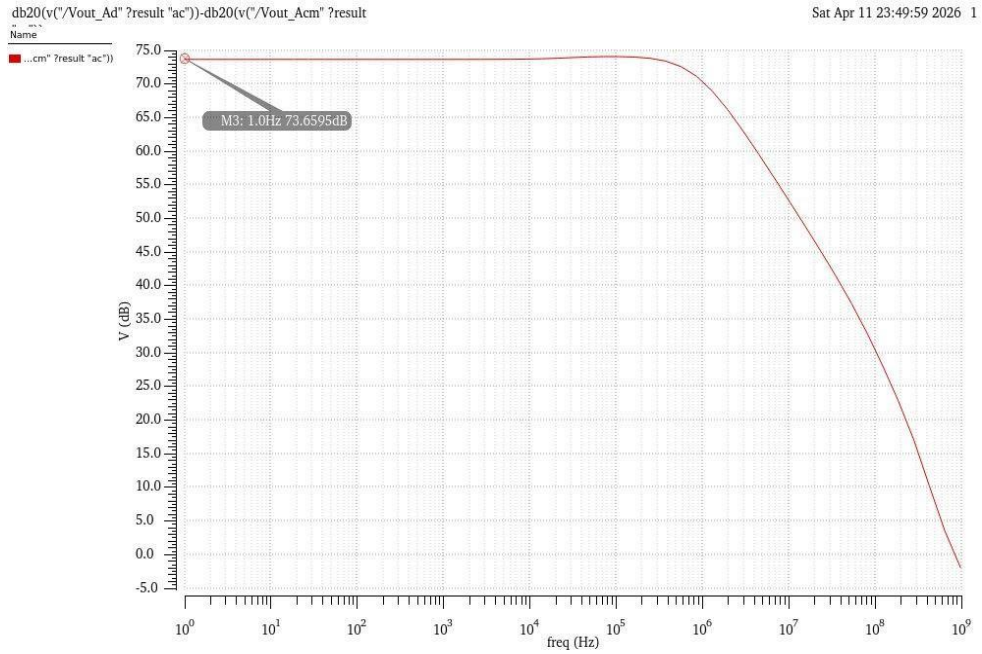

Fig. 10. CMRR — Nulling resistor compensated op-amp (73.69 dB)

E. Power Dissipation

Quiescent power consumption is 0.96 mW for the Miller design and 1.02 mW for the nulling-resistor variant (Fig. 11, Fig. 12). The 0.06 mW overhead—a 6.25% increase—is negligible in virtually any practical application and is a very small price to pay for the improvement in stability.

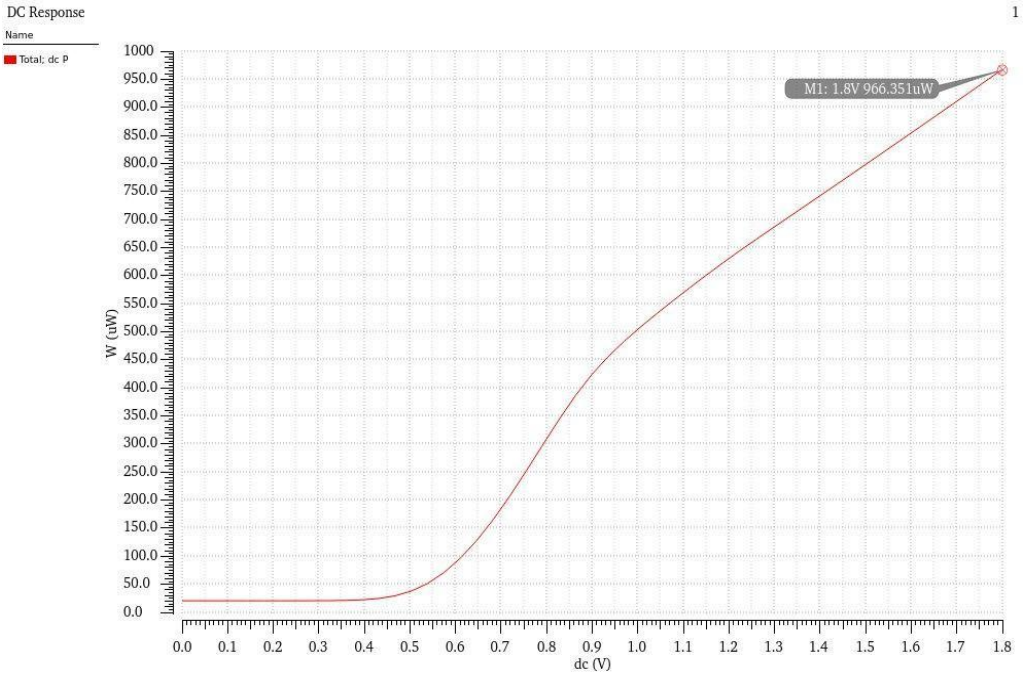

Fig. 11. Total power dissipation — Miller compensated op-amp (0.96 mW)

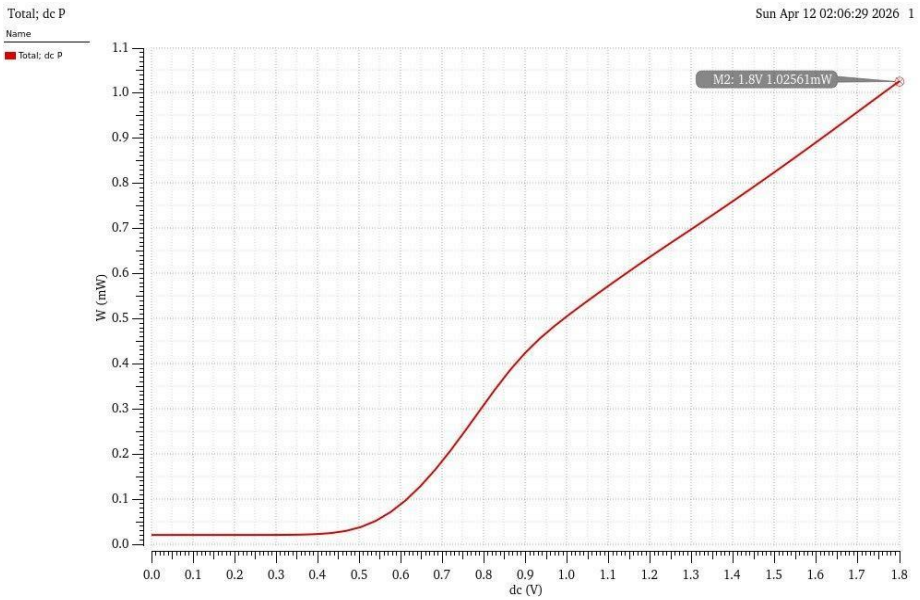

Fig. 12. Total power dissipation — Nulling resistor op-amp (1.02 mW)

F. Comparative Summary

TABLE II. PERFORMANCE COMPARISON

Parameter	Miller Comp.	Nulling Res.
DC Gain (dB)	70	70
GBW (MHz)	75	83
Phase Margin (°)	45.86	77.43
CMRR (dB)	73.6	73.69
Slew Rate (V/µs)	30	30
Power (mW)	0.96	1.02
Supply (V)	1.8	1.8
Load Cap. (pF)	2	2
Stability	Moderate	High

Table II brings all the measurements together. The nulling-resistor design beats the baseline by a full 31.57° in phase margin and adds 8 MHz of bandwidth, while the extra power is barely measurable at 0.06 mW. The fact that DC gain and CMRR do not change between the two topologies validates a key prediction: the nulling resistor only touches the zero, leaving everything else alone.

VII. CONCLUSION

This study compared two frequency-compensation strategies for a two-stage CMOS op-amp in 180 nm technology, using Cadence Virtuoso simulations with matched bias and load conditions. The results are clear: adding a nulling resistor in series with the Miller capacitor raises the phase margin from 45.86° to 77.43° and extends the GBW from 75 MHz to 83 MHz, while DC gain (70 dB), CMRR (~73.6 dB), and slew rate (30 V/µs) remain essentially unchanged. The quiescent power rises by just 0.06 mW. These findings confirm, in simulation, that the nulling resistor is an efficient and low-cost way to eliminate the RHP zero that conventional Miller compensation introduces, and that this single change meaningfully improves closed-loop stability without compromising any other aspect of performance.

VIII. FUTURE SCOPE

A few natural extensions of this work come to mind. Running a full PVT corner sweep alongside Monte Carlo analysis would show how much spread to expect across manufacturing variation—something that is essential before moving toward a real tape-out. Replacing the passive resistor with a transistor biased in the triode region would allow the zero location to be tuned electrically, which could be useful in adaptive or reconfigurable designs. Extending the compensation framework to three-stage amplifiers using nested Miller structures, and then running post-layout extraction to capture parasitics, would be the remaining steps toward a silicon-ready implementation.

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