Design Optimization and Evaluation of Comparative Analysis of Multi-Stage CMOS Ring Oscillators for Radio Frequency Applications

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***Abstract*— In today's technology dependent world, oscillators have been the center piece of the electronics. Its application ranges from clock generation in microprocessors to cellular telephones and mobile communication. Each of these need vastly different oscillator topologies and performance parameters neatly balanced. Robust and high-performance oscillator design in CMOS technology has been an emerging and efficient form of oscillators; however, it poses interesting challenges. This paper deals with analysis and design of CMOS ring oscillators. It begins with a general overview of oscillations in feedback systems; further ring oscillators are brought to light along with methods of varying the oscillation frequency. Specifically, this paper talks about 3-stage, 5-stage and 7-stage configurations on the Cadence Virtuoso tool. The circuits were simulated and analyzed leading to the evaluation of key performance parameters such as oscillation frequency, propagation delay, power dissipation and phase shift. The relationship between the number of stages and different parameters are studied, demonstrating for various uses we can have specific configurations of CMOS Ring Oscillator.**

***Index Terms*—CMOS ring oscillator, oscillation frequency, propagation delay, power dissipation, Cadence simulation**.

I. INTRODUCTION

Oscillators have been a fundamental part of electronic systems, which have provided stable reference frequencies for signal generation, synchronization and modulation since its genesis. Now in RF applications like Bluetooth (2.4 GHz), GSM and Wi-Fi Transceivers (2.4 GHz, 5 GHz), Quartz Crystal Oscillators have been a preferred choice due to its capability of harnessing the piezoelectric effect. It produces the electrochemical resonance modeled by the equivalent RLC circuit. Its Quality Factor (Q) which ranges from 20K to nearly 10^6 yields exceptional frequency stability of around ±10–50 ppm, also its phase noise is as low as 150 dBc/Hz at 1 kHz offset; this level of stability is critical in RF

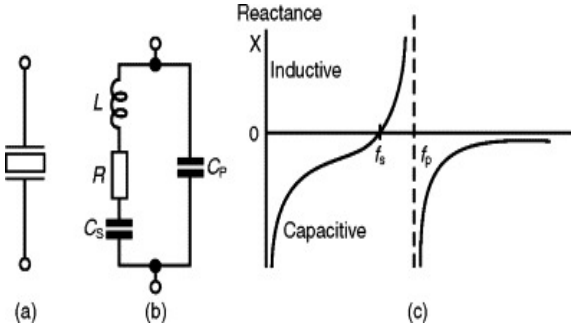

Fig. 1: Equivalent circuit and reactance characteristics of a crystal oscillator

Crystal oscillators operate across a broad range from 32.768 kHz in real-time clocks to beyond 200 MHz in radar and satellite systems.

In spite of these advantages, the crystal oscillators present certain critical limitations as follows:

1) Incompatibility with modern CMOS monolithic integration technology
2) Requirement of discrete off-chip components (3.2×2.5 mm SMD packages)
3) Relatively high-power consumption (1–20 mW)
4) Limited frequency tunability (typically less than±100 ppm)

Here comes CMOS ring which overcomes these constraints by just cascading N inverting stages in a closed feedback loop, which achieves oscillations at [2]:

$$f_{osc} = \frac{1}{2 \cdot N \cdot t_{pd}} \quad (1)$$

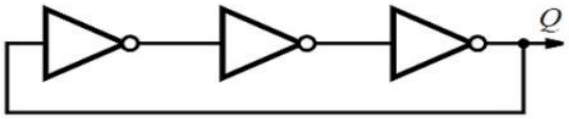

Fig. 2: 3-stage Ring Oscillator

Also, it offers voltage-controlled frequency tunability exceeding ±30 Power consumption is in the order of μW, the on-chip area reduces below 50 μm^2. However, the phase noise is typically in the range of 80 to 110 dBc/Hz at 1 MHz offset which is well within limits for RF applications. These let us have 10× reduction in area and power as compared to crystal-based solution at the cost of moderate phase noise trade-off [2][5].

II. LITERATURE SURVEY

In early years, the rapid advancement in VLSI Technology has significantly increased the challenge for concise, low- power design, and high-speed timing & switching circuits in modern communication systems. Oscillators are the centre piece of digital electronics where it generates the periodic signals essential for synchronization, clock generation, and radio frequency (RF) communication. Conventionally, crystal oscillators have been widely used as they exhibit excellent frequency stability and low phase noise characteristics.

Apart from this, crystal oscillators require the external components that occupy the larger physical space, and offer bounded tunability, making them less suitable for highly integrated system-on-chip (SoC) applications. Several studies have explored different design techniques to improve the performance of ring oscillators in terms of power consumption, phase noise, jitter, and frequency stability.

Early work by Aman Shivhare and M. K. Gupta [1] illustrated the design of a low-power CMOS ring oscillator implemented in 180 nm CMOS technology. Their study addresses the challenges of excessive power consumption in conventional oscillator circuits by optimizing the configuration of the inverter that employs efficient feedback mechanisms to reduce switching losses. Similarly, Behzad Razavi [2] showcases the fundamental principles of oscillator circuit design in integrated systems, emphasizes the importance of scalable architectures capable of operating reliably under environmental and process conditions. His work proven the theoretical foundation for integrating oscillator circuits directly onto semiconductor chips to improve reliability of the overall circuit and reduce the complexity of the system. Phase noise and signal stability are critical performance parameters in RF oscillator design, particularly for communication systems where timing accuracy directly affects signal integrity and data transmission quality. Research conducted by Liang Dai and Ramesh Harjani [4] investigated different ring oscillator configurations to minimize phase noise through improved delay cell linearity and optimized load design. Their analysis demonstrated that increasing voltage swing and reducing device nonlinearity significantly improved oscillator stability and reduced noise levels. Additional studies by Behzad Razavi [5] further examined the noise behavior of CMOS oscillators and identified key noise sources such as thermal noise, flicker noise, and power supply variations that contribute to phase fluctuations in oscillator outputs. These findings provided valuable insights into the design of low-noise oscillator circuits suitable for high-frequency applications.

Power consumption remains another critical design in consideration of oscillator circuits, particularly in battery- powered and portable devices. Researchers including S. Priyadarshini and colleagues performed comparative studies on ring oscillators implemented in advanced technology nodes such as 45 nm and 90 nm CMOS technologies [8] [6]. Their work focused on analyzing the effect of technology scaling on oscillator performance parameters, including frequency, propagation delay, and power dissipation. The results demonstrated that reducing transistor dimensions leads to higher operating frequencies and lower dynamic power consumption due to reduced capacitance and improved switching speed. Additional research on voltage-controlled oscillators in nanoscale technologies [9] [7] highlighted the importance of optimizing supply voltage and transistor sizing to achieve ultra-low-power operation while maintaining stable oscillation characteristics.

Periodic steady-state (PSS) analysis has become an essential simulation technique for evaluating oscillator performance under steady operating conditions. Studies on oscillator simulation methods have shown

that PSS analysis enables accurate prediction of oscillation frequency, output waveform stability, and power consumption in nonlinear circuits [11]. These techniques allow designers to analyze oscillator behavior over multiple cycles and determine steady-state performance parameters such as amplitude, phase noise, and harmonic distortion. Furthermore, researchers investigating tuning mechanisms in CMOS oscillators have explored the use of variable control voltages to adjust oscillation frequency over a wide range, enabling flexible operation in communication systems that require frequency agility and dynamic signal control [12][13].

III. METHODOLOGY

The proposed CMOS ring oscillator were designed and simulated using Cadence Virtuoso design suite. Two process technology nodes were employed in this study, 180nm and 45 nm CMOS technology to analyze and compare the performance of CMOS ring oscillators at different technology scales. For each technology node, three ring oscillator configurations were designed namely, 3-stage, 5-stage and 7-stage topologies. Each ring oscillator was designed by cascading an odd number of CMOS inverter stages with the output of the last stage feedback to the input of the first stage to form a closed loop feedback system. The condition for sustained oscillations requires the total phase shift around the loop equals 360◦ with each inverter contributing 180◦ of phase shift satisfying Barkhausen's Criteria [2] Proposed Designs of CMOS Ring Oscillators using 180nm and 45 nm Technology Nodes

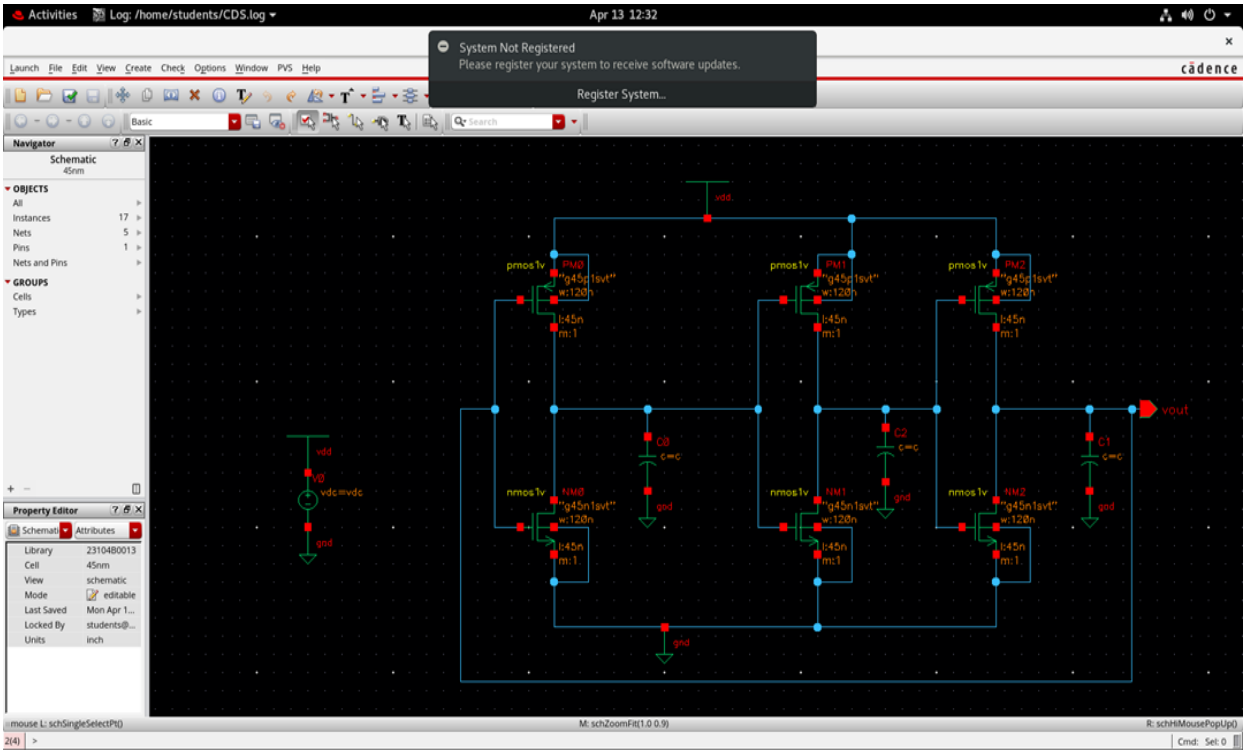

Fig. 3: 3-stage CMOS Ring Oscillator Schematic

The 3-stage oscillator shown in Fig. 3 consists of three CMOS inverter stages connected in a closed loop. The signal propagates through each stage creating a propagation delay that determines the oscillation frequency. Since the number of stages is minimal (3), the total propagation delay is very small, resulting in higher oscillation frequency.

Fig. 4: Performance analysis of 3-stage CMOS ring oscillator

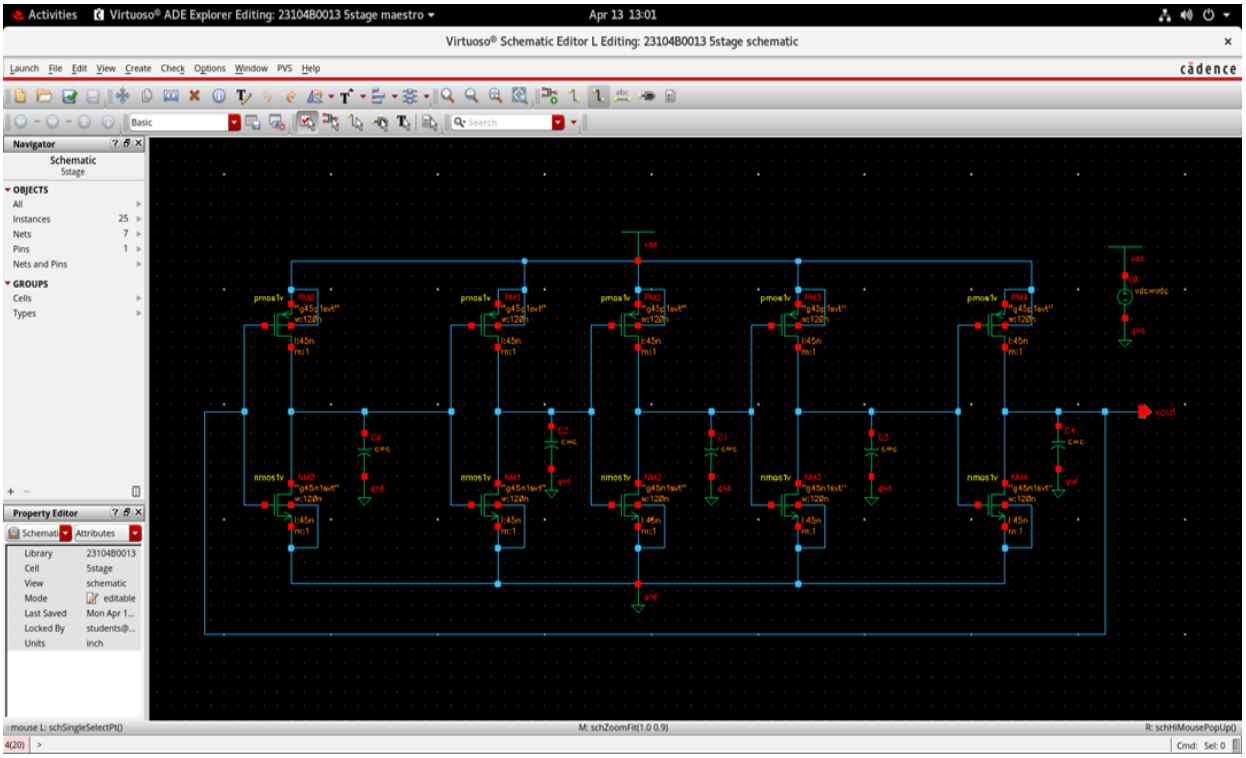

Fig. 5: 5-stage CMOS Ring Oscillator Schematic

In the 5-stage configuration shown in Fig. 5, it is observed that increasing the number of stages increases the overall propagation delay. This results in a reduction in oscillation frequency.

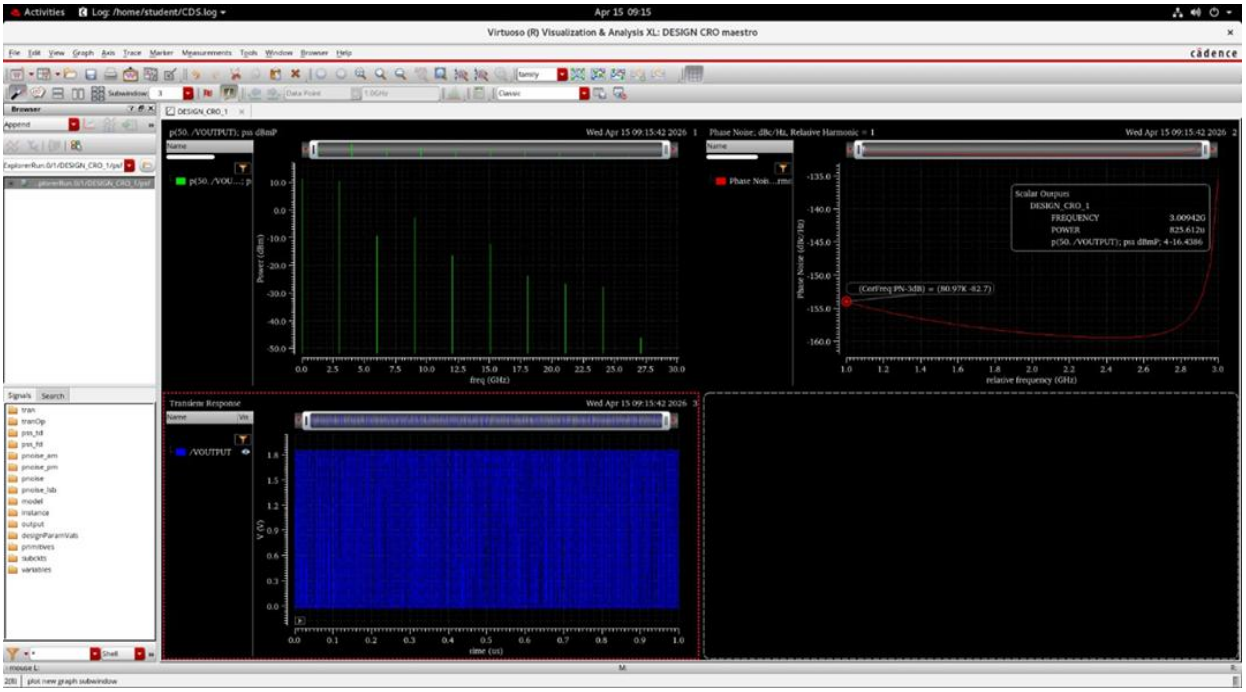

Fig. 6: Performance analysis of 5-stage CMOS ring oscillator

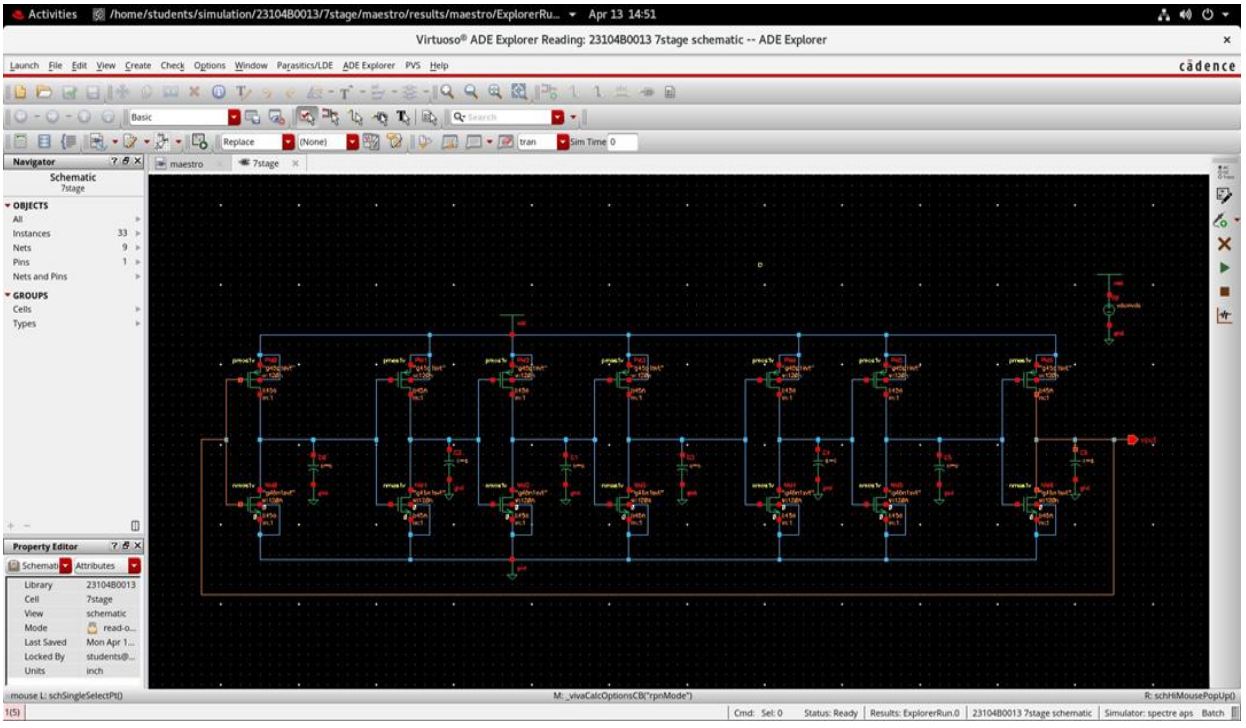

Fig. 7: 7-stage CMOS Ring Oscillator Schematic

In the 7-stage configuration shown in Fig. 7, seven CMOS inverters are cascaded in a closed loop. It is observed that increasing the number of stages results in higher cumulative delay, leading to lower oscillation frequency.

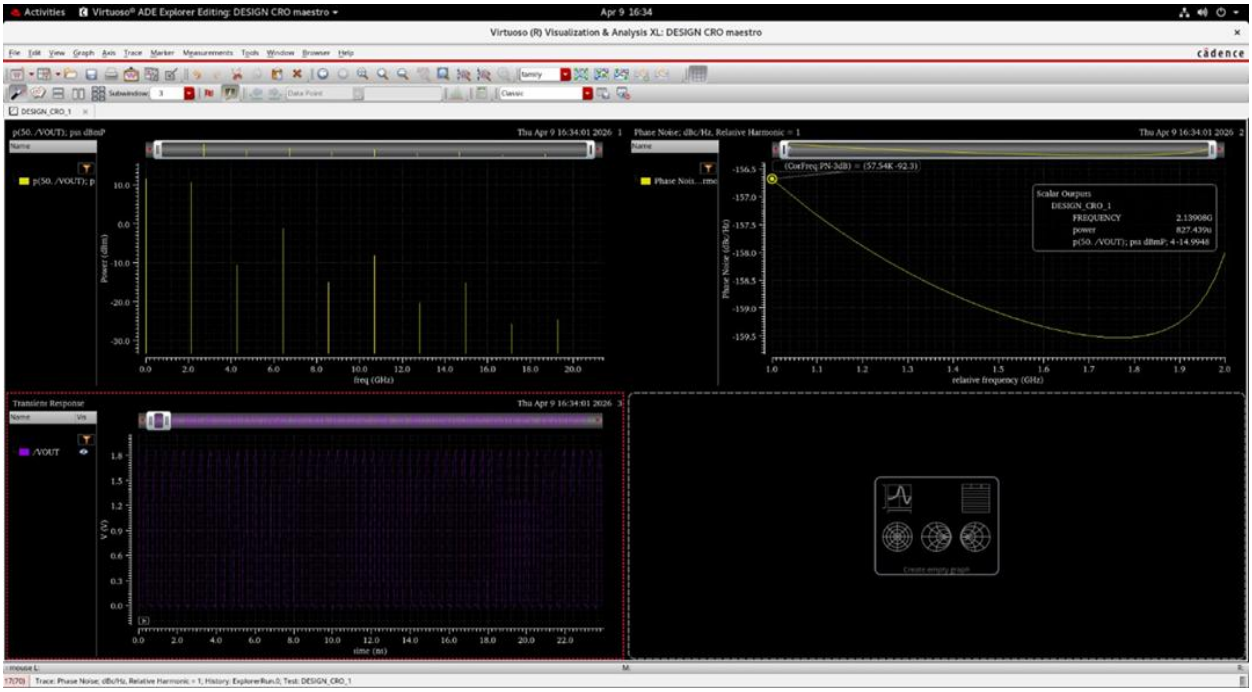

Fig. 8: Performance analysis of 7-stage CMOS ring oscillator

Table I: Frequency Analysis of 3-Stage CMOS Ring Oscillator

Technology Node: 180 nm	Technology Node: 45 nm
Frequency obtained: 5.401 GHz	Frequency obtained: 5.88 GHz

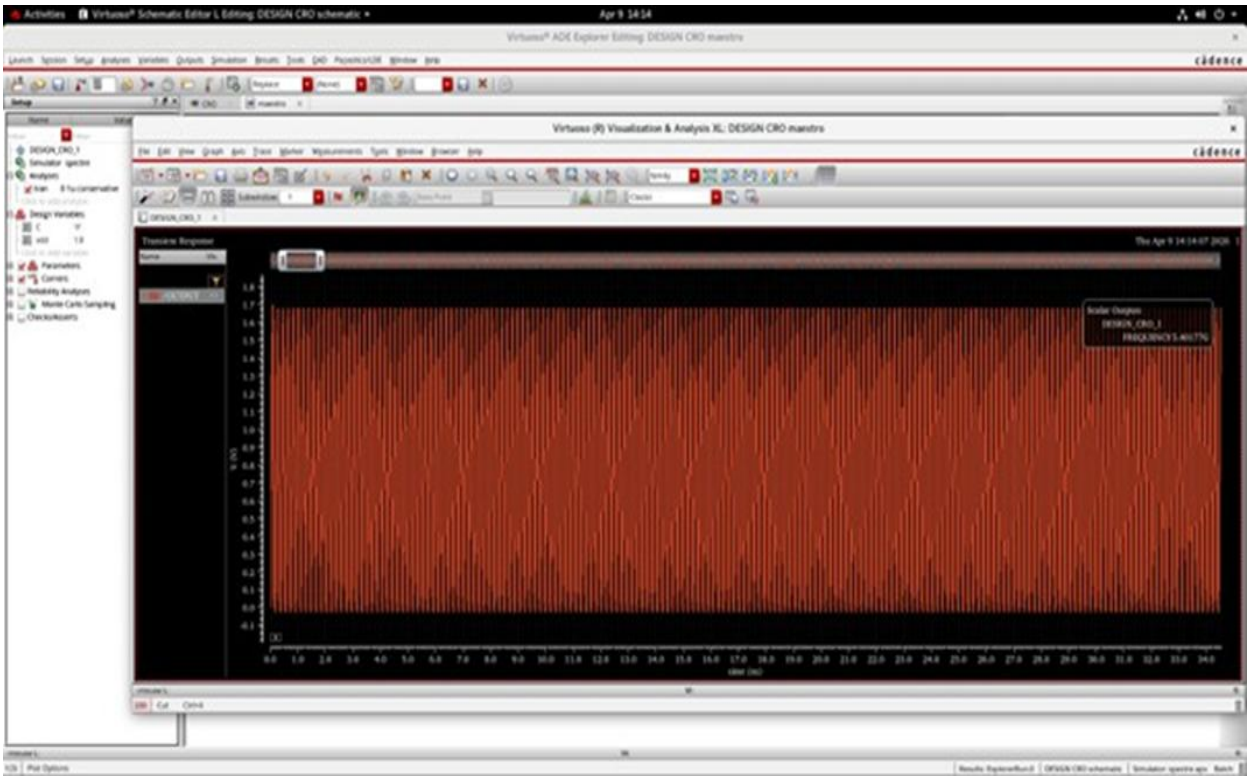

Fig. 9: Frequency response of 3-stage CMOS ring oscillator (180nm)

Fig. 10: Frequency response of 3-stage CMOS ring oscillator (45nm)

Table II: Frequency Analysis of 5-Stage CMOS Ring Oscillator

Technology Node: 180 nm	Technology Node: 45 nm
Frequency obtained: 3.009 GHz	Frequency obtained: 3.484 GHz

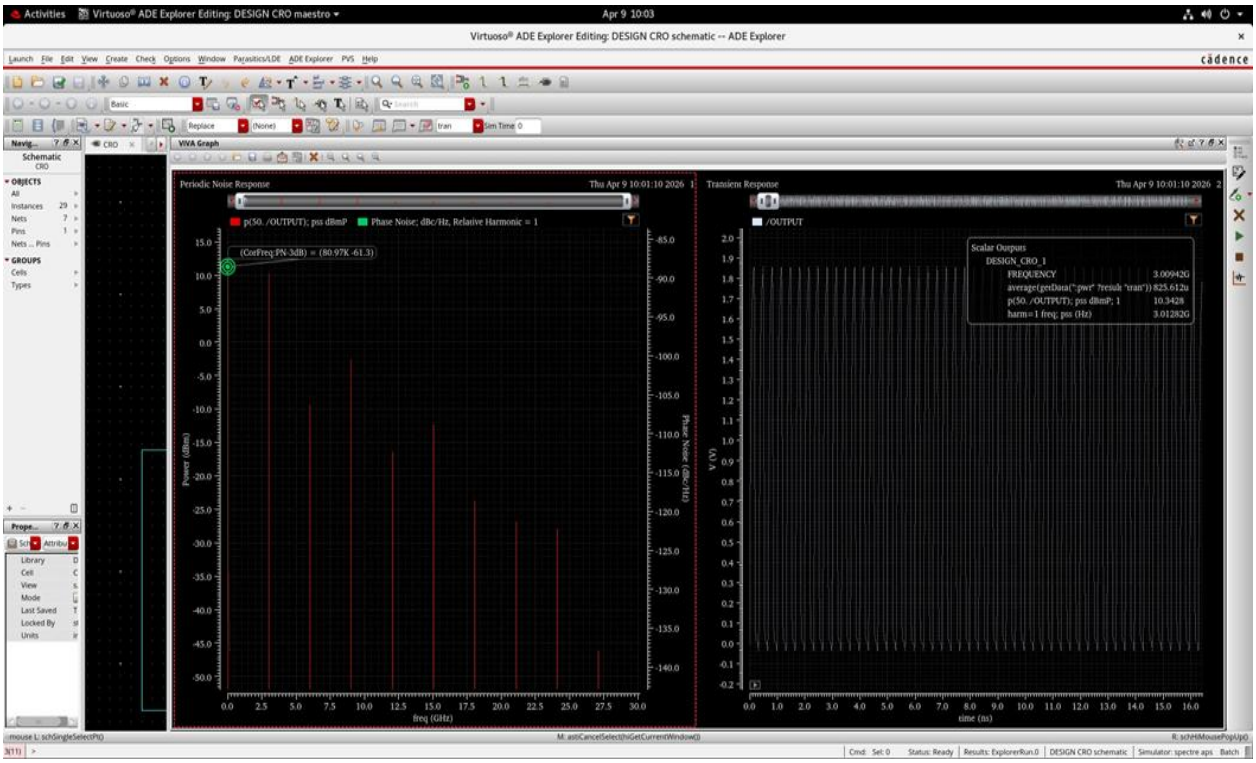

Fig. 11: Frequency response of 5-stage CMOS ring oscillator (180nm)

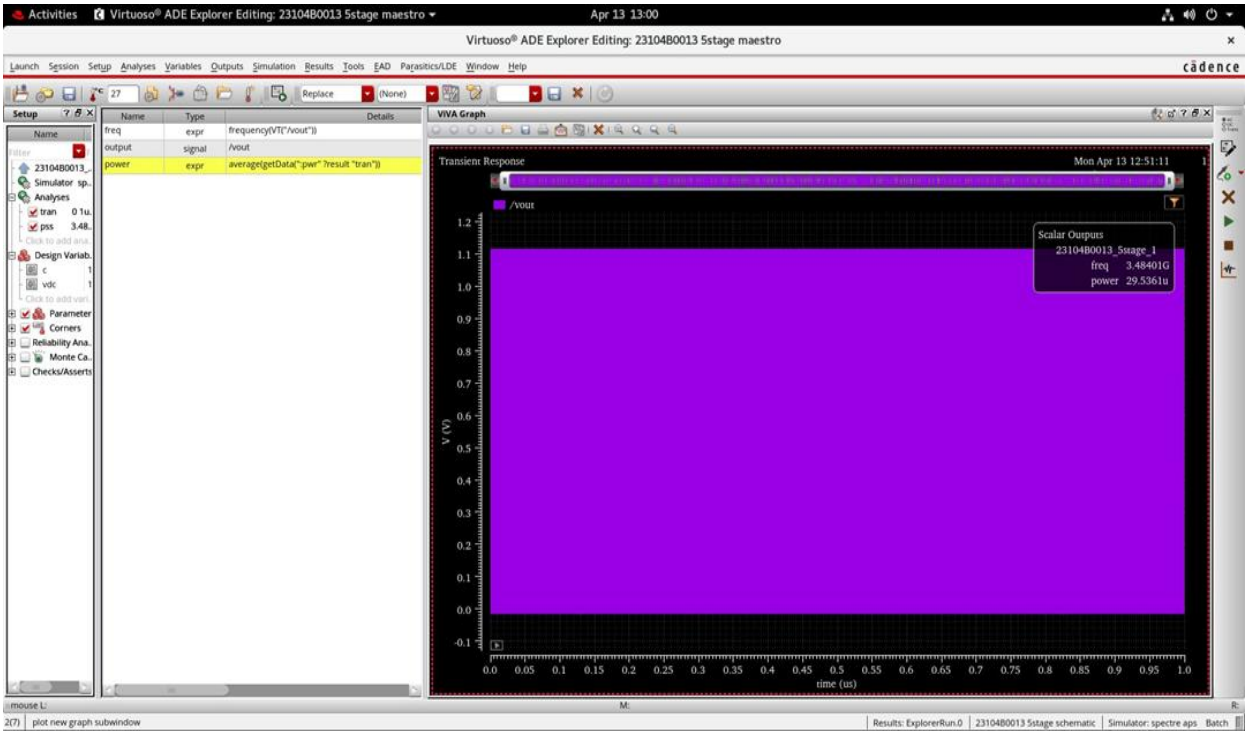

Fig. 12: Frequency response of 5-stage CMOS ring oscillator (45nm)

Table III: Frequency Analysis of 7-Stage CMOS Ring Oscillator

Technology Node: 180 nm	Technology Node: 45 nm
Frequency obtained: 2.13 GHz	Frequency obtained: 2.49 GHz

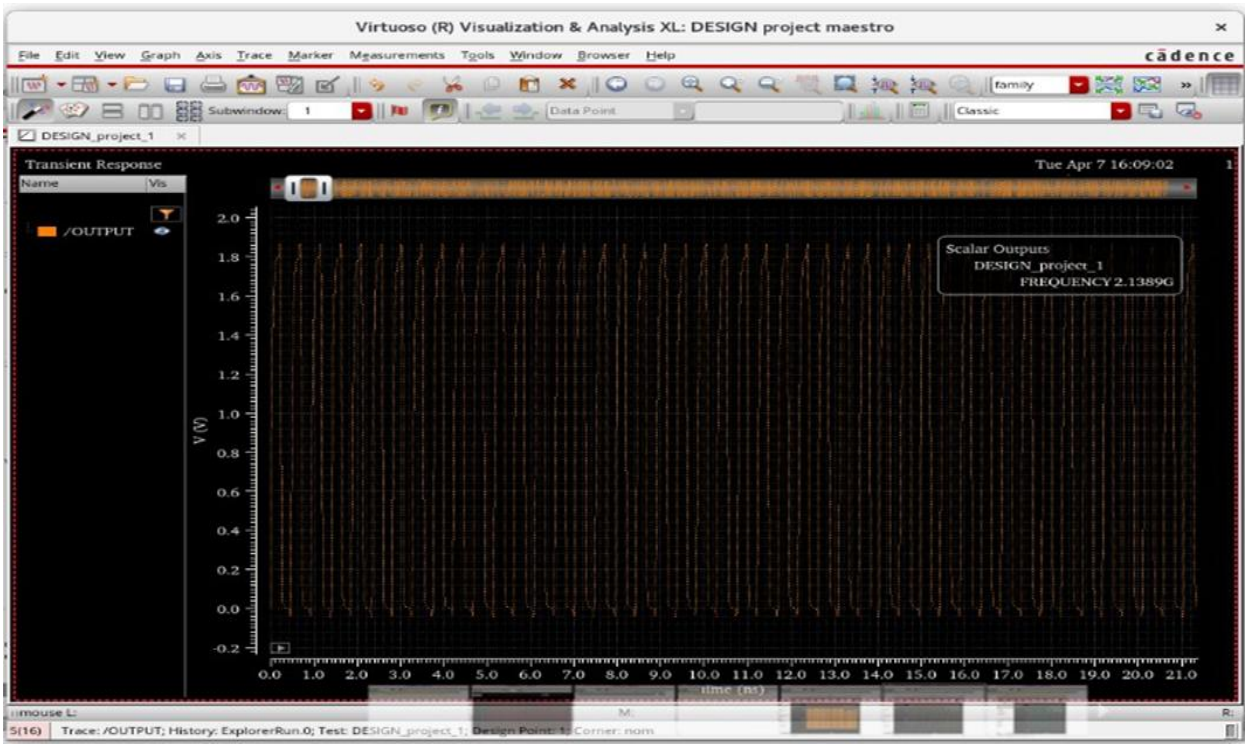

Fig. 13: Frequency response of 7-stage CMOS ring oscillator (180nm)

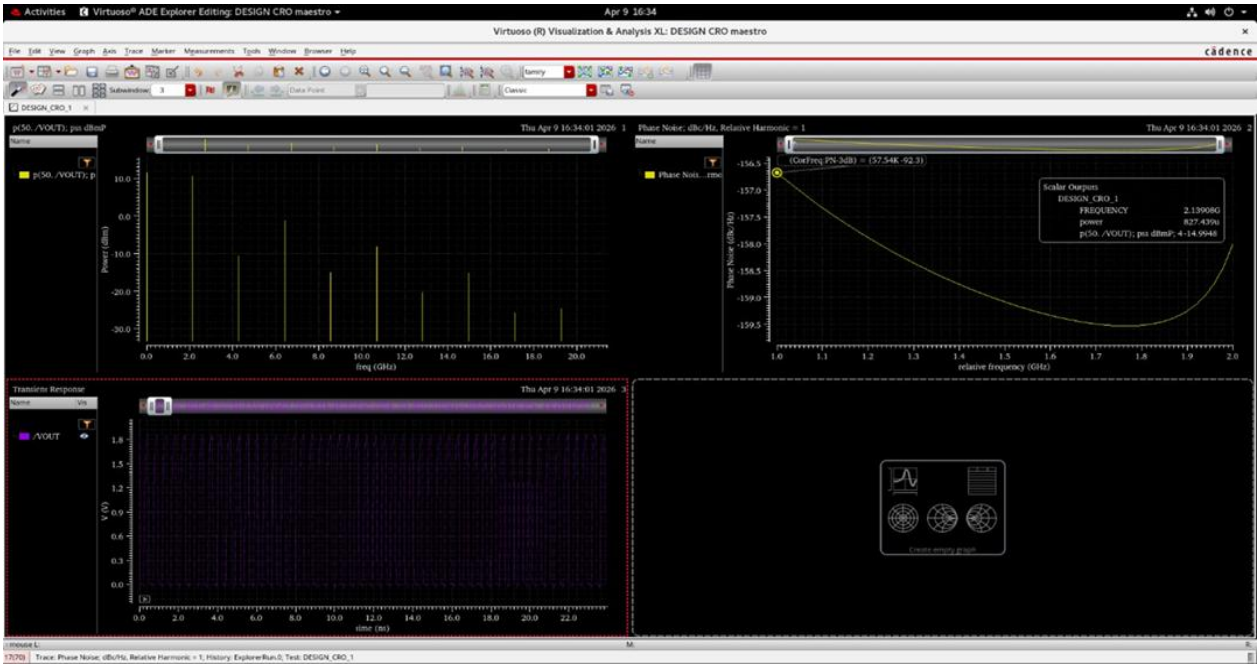

Fig. 14: Frequency response of 7-stage CMOS ring oscillator (45nm)

A. Performance Evaluation Parameters

Propagation Delay: Propagation delay is defined as the operating frequency of a CMOS Ring Oscillator. It states the time required for the transition of a signal that propagates through a single inverter stage that frequently measured the 50% of voltage level between the input and the output wave forms. The propagation delay is affected by various determi- nant factors such as load capacitance, processing parameters, supply voltage etc.

The total time determined for one complete oscillation cycle is twice the gradual propagation delay for all the stages. Since full period includes translations of both the rising and falling time

$$t_p = \frac{t_{PLH} + t_{PHL}}{2} \qquad (2)$$

where tp is the average propagation delay, tP LH is the low- to-high transition delay, and tP HL is the high-to-low transition delay.

Power dissipation: Power dissipation defines the amount of power consumed by the oscillator during the operation. This is considered as most important aspect which is critical for low power designs [1] [9].

$$P = N \cdot C \cdot V_{DD}^2 \cdot f \qquad (3)$$

where N is the number of stages, C is the total nodal capacitance, VDD is the supply voltage, and f is the oscillation frequency.

Periodic Steady State Response (PSS): It is an equivalent of DC analysis but as the name suggests it is applied for periodic circuits which locate the periodic steady state response of a circuit and computes the periodic operating point [11].

There are two PSS methods:

- Harmonic Balance (ADS): – Frequency Domain Analysis
- Shooting Method (Cadence Spectre-RF): – Time Domain Analysis

Since the proposed design of CMOS Ring Oscillator operates in the time domain, thus the shooting method is implemented for periodic steady state analysis [11]. It evaluates the steady state response by iteratively solving the circuit's differential equation over one period of oscillation. It evaluates and compares all the voltages and current at the start and to end of the shooting interval

$$F(x_0, T) = x(T; x_0) - x_0 = 0 \qquad (4)$$

where x0 represents the initial state vector (node voltages), T is the oscillation period, and x (T; x0) represents the state of the system after one period obtained through numerical integration [11]. noise [5]. In the proposed designs, the noise performance of the oscillator is computed across the wide range of offset frequencies from the carrier signal.

To calculate the phase noise, we consider a unit bandwidth at offset Δω from the carrier frequency ω_0. The noise power which is within this 1 Hz bandwidth is calculated and normalized with respect to the total signal power [5].

$$L(\Delta\omega) = 10 \log_{10} \frac{P_{noise}(\omega_0 + \Delta\omega,\ 1\ Hz)}{P_S} \quad (5)$$

where Pnoise is the noise power in a 1 Hz bandwidth, Psig is the carrier signal power, and Δω is the offset from the carrier frequency [5]. Jitter: It is defined as the variation in the timing of the signal's rising or falling edge from its ideal position. It is the method that describes the stability of an oscillator in the time domain. It integrates all the noise sources together with respect to time [17].

IV. RESULTS

A. Summary Table

Table IV: Performance Parameters of CMOS Ring Oscillator (180 nm)

Parameter	3-Stage	5-Stage	7-Stage
Frequency (GHz)	5.401	3.009	2.13
Dynamic Power(μW)	785.7	825.6	827.4
PSS (dBm)	-22.68	-16.44	-14.99
Phase Noise (dBc/Hz)	-78.5	-83.7	-92.3
Voltage	0.6–1.2	0.6–1.2	0.6–1.2
Jitter (fs)	63.04	76.59	53.32

Table V: Performance Parameters of CMOS Ring Oscillator (45 nm)

Parameter	3-Stage	5-Stage	7-Stage
Frequency (GHz)	5.88	3.484	2.49
Dynamic Power(μW)	29.11	29.54	29.55
PSS (dBm)	-30.03	-28.43	-29.73
Phase Noise (dBc/Hz)	-88.2	-91.4	-92.08
Voltage	0.6–1.1	0.6–1.1	0.6–1.1
Jitter (fs)	278.2	274.2	253.7

random fluctuations in the output phase. These fluctuations lead to spread out around the center frequency, creating sidebands. This spreading of the spectral line is called phase

V. CONCLUSION

This Paper gives the design and simulation of 3-stage, 5-stage, and 7-stage CMOS ring oscillators at 180 nm and 45 nm technology nodes using Cadence Virtuoso, comprehensively evaluating parameters like oscillation frequency, dynamic power dissipation, PSS, phase noise, tuning voltage range and jitter.

In both these technology nodes, it was consistent that the increasing number of inverter stages reduces the oscillation frequency because of the increased propagation delay, simultaneously the dynamic power dissipation also increased as a result of higher switching activity. At 180 nm, the oscillation frequency dropped from 5.401 GHz (3-stage) to 3.009 GHz (5-stage) and further to 2.13 GHz (7-stage), while the dynamic power rose from 785.7 μW to 825.6 μW and 827.4 μW respectively. A very same pattern was observed for 45 nm, where frequency increased from 5.88 GHz down to 3.484 GHz and 2.49 GHz across the three configurations, however the power remained almost constant at approximately 29.11 μW, 29.54 μW, and 29.55 μW which was a reduction of approximately 27 times as compared to 180 nm node, this was the result of lower supply voltage (0.6–1.1 V vs. 0.6–1.2 V) and the decreased switching capacitance for smaller geometry. For Phase Noise, the 7-stage configuration consistently demonstrated the best spectral purity in both 45 nm and 180 nm, to be precise −92.3 dBc/Hz at a 57.5 kHz offset (180 nm) and −92.08 dBc/Hz at a 1.092 MHz offset (45 nm), as compared to−78.5 dBc/Hz at 206.2 kHz and −88.2 dBc/Hz at 3.906 MHz for the 3-stage designs respectively. This improvement is the result of increased number of stages which averages out the uncorrelated thermal and flicker noise contributions each stage, resulting for 7-stage topology at 45 nm to operate at 2.49 GHz with −92.08 dBc/Hz phase noise with only 29.55 μW power dissipation. This makes it the most suit-able candidate to work as Voltage-Controlled Oscillator (VCO) in the Phase-Locked Loops (PLLs) in Bluetooth (2.4 GHz band) and for IoT communication front-ends, as these applications require constrained spectral purity and power budget. For the clock generation application where time-domain stability is the core figure of merit. The 7-stage 180 nm oscillator achieves the lowest jitter of 53.32 fs, overpowering the 5-stage (76.59 fs) and 3-stage (63.04 fs) configurations at the same node.

Though the 45 nm node exhibited much higher jitter values 253.7–278.2 fs across all stages), because of the increased sensitivity to the supply and substrate noise for the lower geometries, its lower power advantages make it a preferable option in energy-constrained systems where the moderate jitters can be allowed.

To summarize, the 7-stage 45 nm design offers the optimal balancing between phase noise and power for PLL based RF applications: also, the 7-stage 180 nm design is preferred option for low-jitter clock generations. The 3-stage 45 nm design is the best option for the high-frequency and ultra- low power RF carrier generation. This makes the CMOS ring oscillators a versatile and technologically-scalable building block for the next-generation VLSI (on-chip) and RF Integrated Systems.

VI. FUTURE SCOPE

If we scale the proposed CMOS ring oscillator to now-in- research sub-7 nm FinFET and Gate-All-Around (GAA) technology, it is expected power consumption will be reduced by a factor of 3–5×. At the same time the oscillation frequencies will reach beyond 10 GHz, which is a viable frequency for 5G NR mmWave and also for the emerging 6G pre-standard frequency bands.

As said earlier, ring oscillators can be used as on-chip VCOs for on-chip PLLs, mixers and also Low Noise Amplifiers (LNAs). This enables a complete monolithic transceiver front- end for both Bluetooth 5.x and Wi-Fi 6E standards. It will reduce the system-level form factor and off-chip component dependency.

If we adopt the digitally controlled biasing and adaptive body- biasing techniques, it can enhance the frequency stability across the PVT corners, thus improving the noise performance to closer to −120 dBc/Hz. Crystal oscillators work with this level of noise performance in radar and precision RF applications.

Power scalability of the oscillator with sub-μW will make it well suited for duty-cycled clock generation in IoT sensor nodes and also for low-power edge computing platforms which operate below 1 V supply.

Post-layout parasitic capacitance extraction and Spectre RF P-Noise simulation will provide the silicon-accurate validation of jitter and phase noise metrics.

Differential ring oscillator topologies in advanced nodes will suppress common-mode noise and power supply rejection, which will directly improve the jitter performance to sub- picosecond levels. This is required in high-speed serial links and radar pulse timing in automotive ADAS systems.

Extending the design toward a VCO architecture by incorporating varactor-loaded stages can widen the tuning range, enabling frequency agility across multiple RF bands including sub-6 GHz 5G, ISM, and UWB spectrums.

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