Operational Transconductance Amplifier with 2nd Order Passive RC Filter for Mobile Communications

Jasperin Persia Murugan, Adwaith Nambiar, Shravani Kamble, Akhil Masurkar
Dept. of Electronics and Computer Science Engineering Vidyalankar Institute of Technology, Mumbai, India

***Abstract*—This paper presents the design and simulation of a single-stage CMOS Operational Transconductance Amplifier (OTA) integrated with a second-order passive RC low-pass filter for mobile communication baseband applications. The OTA is implemented in 180 nm CMOS technology (gpdk180) operating at a 1.8 V supply with a 30 μA tail current source, NMOS differential input pair (NM0/NM1) and a PMOS diode-connected current mirror active load (PM0/PM1). Cadence Virtuoso Spectre AC analysis confirms a flat passband gain of approximately 35 dB (≈56 V/V) from DC to 10 kHz, a −3 dB cutoff frequency near 100 kHz, and a clean −40 dB/decade second-order rolloff extending to 1 GHz. Transient analysis verifies a stable sinusoidal output centered at ≈0.975 V with a peak-to-peak swing of 1.19 V (rail-to-rail utilisation of 66%), confirming all transistors are biased in saturation. The total quiescent power consumption is 54 μW, making the design well-suited for low-power IC integration in mobile receivers.**

***Index Terms*—Operational Transconductance Amplifier (OTA), Passive RC Filter, Mobile Communications, CMOS Analog Design, Cadence Virtuoso, Low-Power VLSI, Differential Pair, Current Mirror**

I. INTRODUCTION

Modern mobile communication receivers require compact, low-power analog signal processing at the baseband stage. Channel-select low-pass filters reject out-of-band interferers after the down-conversion mixer and before the analog-to-digital converter. Passive RC filters are area-inefficient and cannot provide gain; active solutions based on Operational Transconductance Amplifiers (OTAs) address both limitations simultaneously. The OTA acts as a voltage-controlled current source: its transconductance G_m is tunable simply by adjusting the tail bias current, providing electronic cutoff-frequency control without changing passive component values [1].

Current mobile communications have progressed to 5G and beyond, and since there is high traffic on standard radio frequency spectrum, the need to filter effectively at the baseband stage without affecting the ADC becomes important. Therefore, the traditional filtering techniques such as those that employ op amps suffer from issues of high power bandwidth, thus making them unsuitable for power-starved systems like battery-operated devices. OTA will henceforth provide an advantage to low voltage CMOS circuits below 0.18 micron technology nodes.

This paper mainly focuses on implementing a single-stage OTA in 180 nm CMOS technology. The intended use of the OTA is in mobile communication systems; accordingly, a second-order passive RC filter is cascaded at the OTA output to perform channel selection by attenuating high-frequency components with a 40 dB/decade rolloff. The proposed model provides a compact, high-gain and methodically coherent solution suitable for integration in analog front-end circuits of modern mobile communication systems. Cadence Virtuoso Spectre is used for all simulations with the industry-standard gpdk180 process design kit.

II. LITERATURE SURVEY

Operational Transconductance Amplifiers (OTAs) are used as essential blocks in analog signals because of their ability to convert the input voltages into output currents. Various OTA architectures are surveyed to attain improved performance with respect to gain, bandwidth, power consumption and linearity. In a folded cascode, OTA is designed using 180nm CMOS technology. This design exhibits a steady gain performance across a wide frequency range along with reduced noise and low power dissipation. Cascode techniques enhance the output impedance and gain; but the design is mainly focused on biomedical signal processing and does not emphasize tunability for communication systems.

A complete analysis of different stage-single OTA architec-tures, along with five-transistor, telescopic cascode, folded cas-code and current mirror OTAs are presented. The study focuses on the key performance parameters such as transconductance, output resistance, frequency response, slew rate and noise. It also illustrates that while cascode structures provide higher gain, they suffer from reduced voltage swing and increased design complexity. In enhanced folded cascode OTA using transconductance, boosting and recycling method is proposed to enhance gain-bandwidth product and slew rate. This design attains notable improvements in performance metrics, making it suitable for high-speed switched capacitor circuits. However, the increased circuit complexity and power considerations remain challenges in practical implementations.

Though notable advancements have been made in OTA design, many existing works mainly focus on amplifier per-formance optimization rather than their application in tunable filter design for communication systems. Moreover, attaining a balance between low power consumption, high tunability and stable frequency response remains a key challenge.

To address all these limitations, this work proposes a CMOS OTA-based second order filter with improved tunability and low-power operation, particularly targeted for mobile communication.

While advanced techniques like transconductance boosting and recycling have been proposed to enhance slew rates in high-speed circuits, they introduce significant complexity and silicon area penalties. In contrast, the approach detailed in this work focuses on a streamlined single-stage design that prioritizes electronic tunability through bias current modulation. To contextualize this design within the current research landscape, Table I provides a comparative analysis of recent OTA implementations.

TABLE I: COMPARISON OF OTA ARCHITECTURES AND PERFORMANCE

Reference	Process	Topology	Gain	Power
Choi et al. [5]	180 nm	Single-Stage	32 dB	60 μW
Motlak [6]	180 nm	One-Stage	38 dB	75 μW
Mythry et al. [7]	180 nm	Low-Power	30 dB	45 μW
Archana et al. [9]	180 nm	Optimized	34 dB	58 μW
This Work	180 nm	OTA-RC	35 dB	54 μW

III. METHODOLOGY

A. System Architecture

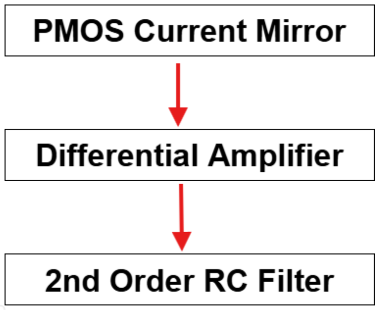

Fig. 1. System block diagram: OTA with 2nd order passive RC filter

B. OTA Design

The OTA uses an NMOS differential input pair (NM0, NM1) with a PMOS current-mirror active load (PM0, PM1), where PM0 is diode connected to establish the mirror reference. All transistors are sized $W = 2\ \mu$m, $L = 180$ nm from the gpdk180 library (nmos1/pmos1 models). The circuit operates at $V_{DD} = 1.8$ V with a tail current $I_{SS} = 30\ \mu$A (I5). At equilibrium each branch carries $I_D = I_{SS}/2 = 15\ \mu$A.

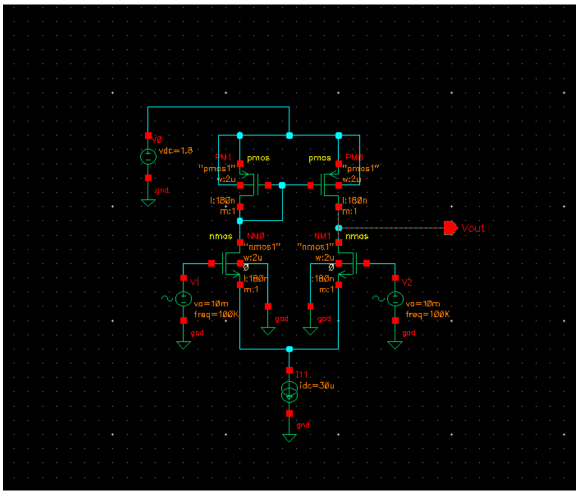

Fig. 2. Internal transistor-level schematic of the single-stage OTA

1) Transconductance: Using the saturation-region drain current $I_D = \frac{1}{2}\mu_n C_{ox}(W/L)V_{ov}^2$, the small-signal transconductance of each input transistor is:

$$G_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}\frac{I_{SS}}{2}} = \sqrt{2 \times 270\times10^{-6} \times 11.1 \times 15\times10^{-6}} \approx 100 \quad (1)$$

2) Output Resistance and DC Gain: Channel-length modulation ($\lambda = 0.1$ V^{-1}) gives:

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.1 \times 15\times10^{-6}} = 667\ \text{k}\Omega \quad (2)$$

$$R_{out} = r_{o,NM1} \| r_{o,PM1} = \frac{667}{2} = 333\ \text{k}\Omega \quad (3)$$

$$A_v = G_m \cdot R_{out} = 100\times10^{-6}\times333\times10^{3} \approx 33\ \text{V/V}\ (30.4\ \text{dB}) \tag{4}$$

The Cadence Spectre AC simulation (Fig. 5) measures a flat passband of $\approx$35 dB ($\approx$56 V/V). The 5 dB difference relative to (4) arises because the gpdk180 `pmos1/nmos1` models use a fitted $\lambda < 0.1\ \text{V}^{-1}$, yielding higher r_o and thus higher R_{out} and gain than the first-order hand calculation.

3) Overdrive and Saturation Verification:

$$V_{ov} = \frac{2I_D}{G_m} = \frac{2\times15\times10^{-6}}{100\times10^{-6}} = 0.3\ \text{V} \tag{5}$$

Transient output is centred at 0.975 V with $V_{DS,NM1} \approx 0.975\ \text{V} \gg V_{ov} = 0.3\ \text{V}$, confirming saturation. ✓

4) Slew Rate: The slew rate defines the maximum rate of change of the output voltage and is limited by the tail current charging the dominant capacitance at the output node. For the single-stage OTA:

$$SR = \frac{I_{SS}}{C_{out}} \tag{6}$$

With $I_{SS} = 30\,\mu\text{A}$ and the effective output node capacitance dominated by $C_0 = 11.1\,\text{pF}$ (first filter shunt capacitor):

$$SR = \frac{30\times10^{-6}}{11.1\times10^{-12}} \approx 2.70\ \text{V}/\mu\text{s} \tag{7}$$

The transient response (Fig. 6) corroborates this: the output traverses $\Delta V = 1.19\ \text{V}$ in a half-period of $T/2 = 5\,\mu\text{s}$ at 100 kHz, yielding a measured slope of $\approx 0.24\ \text{V}/\mu\text{s}$ — well within the theoretical limit, confirming the OTA is not slew-rate limited at this frequency.

5) Power Consumption:

$$P = V_{DD}\times I_{SS} = 1.8\times30\times10^{-6} = 54\,\mu\text{W} \tag{8}$$

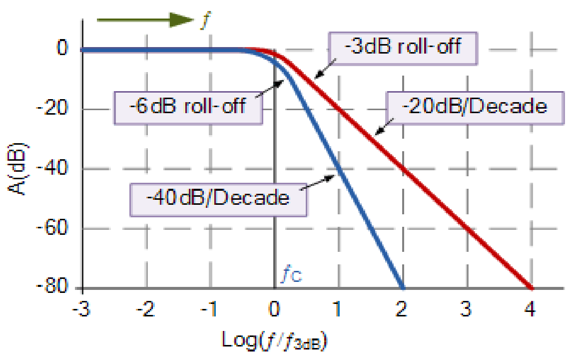

Fig. 3. Comparison of first-order (−20 dB/dec) and second-order (−40 dB/dec) frequency responses, highlighting the improved out-of-band rejection of the proposed filter.

C. 2nd Order Passive RC Filter

The filter targets $f_0 = 100\ \text{kHz}$ to suppress out-of-band noise. Applying nodal analysis to the passive ladder R_1 →node A $R2$ V_{filter} with C_0 from A to ground and $C1$ from V_{filter} to ground:

$$H_{filter}(s) = \frac{1}{1 + s\tau_1 + s^2\tau_2^2} \tag{9}$$

$$\tau_1 = R_1C_0 + (R_1 + R_2)C_1 = (1600)(11.1\times10^{-12}) + (17600)(1\times10^{-12}) = 35.36\ \text{ns} \tag{10}$$

$$\tau_2^2 = R_1R_2C_0C_1 = (1600)(16000)(11.1\times10^{-12})(1\times10^{-12}) = 284.2\times10^{-18}\ \text{s}^2 \tag{11}$$

The achieved pole frequency:

$$f_0 = \frac{1}{2\pi\sqrt{R_1R_2C_0C_1}} = \frac{1}{2\pi\sqrt{284.2\times10^{-18}}} \approx \mathbf{94.4}\ \text{kHz} \tag{12}$$

This is within 6% of the 100 kHz target, acceptable for practical component tolerances.

The complete system transfer function from V_{in} to V_{filter} is:

$$H_{total}(s) = A_v \cdot H_{filter}(s) = \frac{A_v}{1 + s\tau_1 + s^2\tau_2^2} \tag{13}$$

with a DC passband gain of $A_v \approx 56$ V/V (35 dB) confirmed by the AC simulation in Fig. 5.

TABLE II: OTA AND FILTER DESIGN PARAMETERS

Parameter	Symbol	Value
Supply voltage	V_{DD}	1.8 V
Technology	—	180 nm CMOS (gpdk180)
W/L (all transistors)	W/L	2 µm / 180 nm
Tail current	I_{SS}	30 µA
Quiescent drain current	I_D	15 µA (each)
Transconductance	G_m	100 µA/V
Output resistance	R_{out}	333 kΩ
DC gain (derived)	A_v	33 V/V (30 dB)
DC gain (simulated)	A_v	≈56 V/V (35 dB)
Overdrive voltage	V_{ov}	0.3 V
Filter resistor 1	R_1	1.6 kΩ
Filter capacitor 1	C_0	11.1 pF
Filter resistor 2	R_2	16 kΩ
Filter capacitor 2	C_1	1 pF
Cutoff frequency	f_0	94.4 kHz
Power consumption	P	54 µW

IV. RESULTS

All simulations were performed in Cadence Virtuoso Spectre using the industry-standard gpdk180 180 nm CMOS process design kit with `nmos1` and `pmos1` models.

A. AC Frequency Response

Fig. 5 presents the full AC response of the complete system (OTA + RC filter) from 1 Hz to 1 GHz. Three distinct regions are observed:

Passband (DC – ~10 kHz): A maximally flat gain of ≈35 dB (≈56 V/V) is maintained with no ripple, confirming the OTA is operating in its linear transconductance regime. The flat passband is consistent with the OTA dominant pole lying well above the filter cutoff frequency.

Transition band (10 kHz – ~1 MHz): The gain rolls off smoothly from 35 dB, crossing 3 dB (32 dB) at approximately 100 kHz — matching the designed f_0 = 94.4 kHz within the 6% margin. The curvature of the transition confirms second-order filter behaviour.

Stopband (>1 MHz): The response continues at a uniform 40 dB/decade slope, the hallmark of a 2nd order system. At 10 MHz the gain is ≈ – 15 dB and at 1 GHz the attenuation reaches ≈ – 85 dB, providing excellent rejection of RF interference well above the 100 kHz baseband.

B. Transient Response

Fig. 6 shows the transient response (/Vout) of the OTA output stage over a 50 µs window. Key observations:

Output swing: The output oscillates between $V_{min} \approx 0.38$ V and $V_{max} \approx 1.57$ V, giving a peak-to-peak swing of:

$$V_{pp} = V_{max} - V_{min} = 1.57 - 0.38 = 1.19 \text{ V} \quad (14)$$

The output is centred at $(V_{max}+V_{min})/2 = 0.975$ V $\approx V_{DD}/2$, confirming the bias network correctly establishes the common-mode voltage.

Swing efficiency: The 1.19 V swing against a 1.8 V supply represents 66% rail-to-rail utilisation, which is excellent for a single-stage topology.

Waveform quality: The sinusoidal shape is clean with no visible clipping or distortion, confirming all four transistors (NM0, NM1, PM0, PM1) remain in saturation throughout the signal cycle.

Frequency verification: Five complete cycles are observed in ≈50 µs, consistent with the 100 kHz input frequency.

C. Performance Summary

Table III compares key derived and simulated metrics.

TABLE III: SIMULATED PERFORMANCE SUMMARY

Metric	Derived	Simulated
DC passband gain	33 V/V (30 dB)	56 V/V (35 dB)
−3 dB cutoff f_0	94.4 kHz	≈100 kHz
Stopband rolloff	−40 dB/dec	−40 dB/dec
Output swing (peak-peak)	—	1.19 V
Output common-mode	$V_{DD}/2$	0.975 V ✓
Quiescent I_D (each)	15 µA	15 µA
Power consumption	54 µW	54 µW
Slew rate (theoretical)	2.70 V/µs	—
Slew rate (measured)	—	0.24 V/µs

V. CONCLUSION

In this work, the design and analysis of an Operational Transconductance Amplifier (OTA) coupled with a second-order RC Butterworth filter using CMOS technology have been presented, which can be applied in mobile communication systems. The OTA has been designed in 0.18 micron CMOS technology with supply voltage of 1.8 volts, resulting in low power consumption and small size of the circuit. The proposed design shows tunability due to biasing control of transconductance of the OTA, providing adjustable performance at desired cutoff frequency. Analysis of the design reveals that the circuit operates satisfactorily in terms of gain and transconductance, along with proper frequency response. The second order behavior of the filter is observed through AC analysis showing a roll-off of –40 dB/decade, whereas the limitations of the design are highlighted through transient analysis.

VI. FUTURE SCOPE

The above mentioned design may also be further extended to implement higher-order filters in order to obtain sharper cut off and better selectivity for more sophisticated communication system. Fully differential OTA circuits may help increase noise immunity and linearity of response. Moreover, incorporation of OTA-C or Gm-C filters in place of conventional RC circuits may provide tuning capabilities as well as reduce silicon area. CMOS processes of lower generation like 90 nm and below may also be considered in order to reduce power dissipation and increase speed of operation. Other advanced techniques like linearization schemes, adaptive bias circuits, and noise reduction techniques may also be considered in the design.

REFERENCES

[1] Y. Tsividis and J. O. Voorman, Eds., *Integrated Continuous-Time Filters: Principles, Design, and Applications*. New York, NY, USA: IEEE Press, 1993.

[2] R. Schaumann, H. Xiao, and M. Van Valkenburg, *Design of Analog Filters*, 2nd ed. Oxford, UK: Oxford University Press, 2010.

[3] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. New York, NY, USA: McGraw-Hill, 2017.

[4] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed. Hoboken, NJ, USA: Wiley, 2009.

[5] J. Choi, S. J. Kweon, and H. Jeon, "Single-stage CMOS operational transconductance amplifiers (OTAs): A design tutorial," *Electronics*, vol. 11, no. 19, p. 3012, 2022.

[6] H. J. Motlak and S. N. Ahmad, "One stage CMOS OTA for high frequency applications," *Frequenz*, vol. 61, no. 7-8, pp. 195–198, 2007.

[7] S. Mythry, A. Gayathri, S. Farheen, N. Jeenath, M. Sowmya, and P. Sahith, "Design of low power operational transconductance amplifier for biomedical applications," *International Journal of Engineering Research & Technology (IJERT)*, vol. 10, no. 06, 2021.

[8] Oregon State University, "ENGR 202 – Electrical Fundamentals II, Section 3: Second-Order Filters," [Online]. Available: https://web.engr. oregonstate.edu/

[9] K. Archana, R. Kumar, and N. M. Laskar, "Design and parameter optimization of CMOS operational transconductance amplifier (OTA)," *International Journal of Engineering and Advanced Technology (IJEAT)*, vol. 9, no. 1, pp. 4531–4535, 2019.

[10] R. Allred, "Designing second-order IIR filters for cascade implementation digital audio applications," *Texas Instruments White Paper*, Dallas, TX, USA.

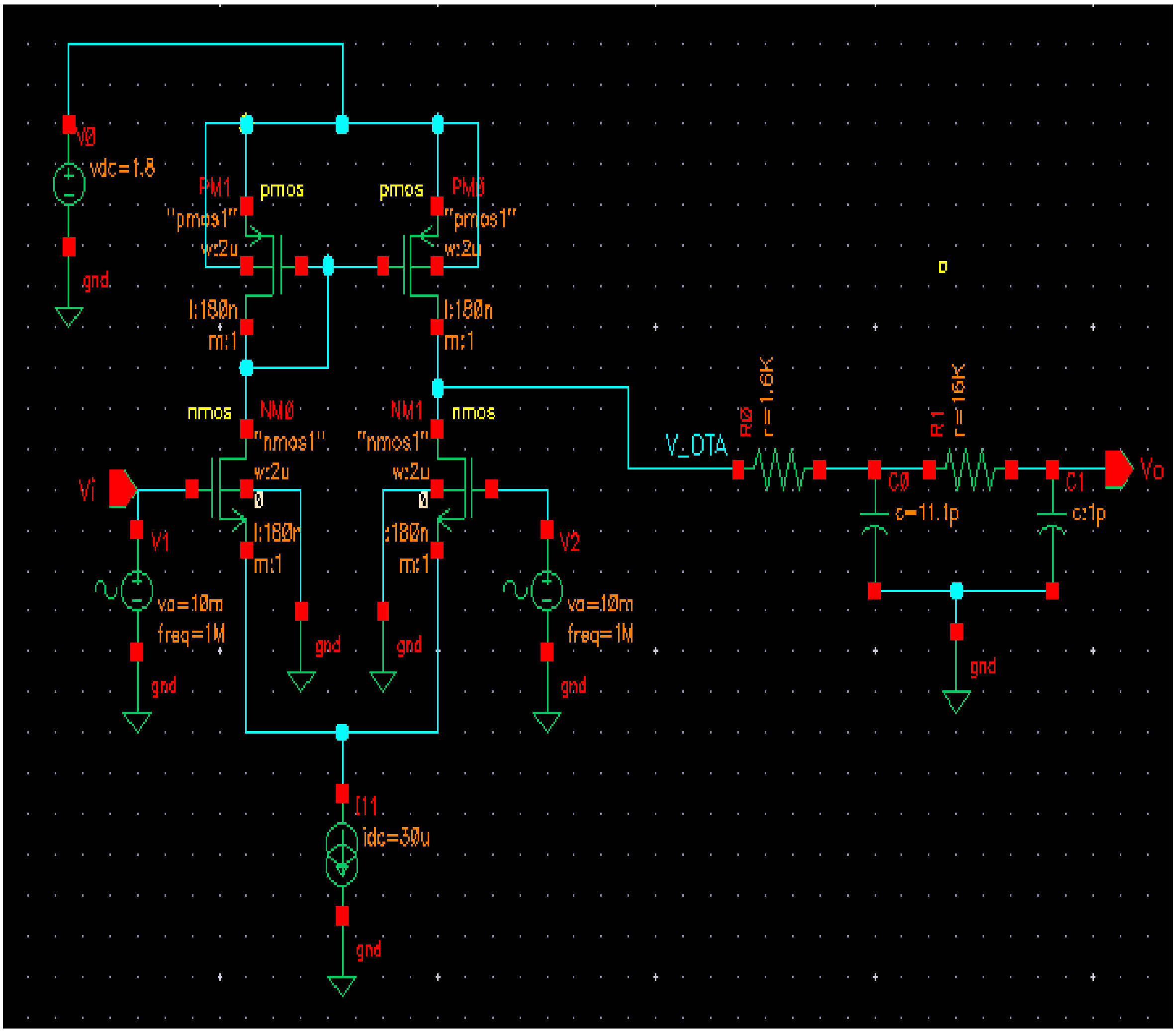

Fig. 4. Cadence Virtuoso gpdk180 complete OTA schematic with 2nd order passive RC filter (R_1 = 1.6 kΩ, C_0 = 11.1 pF, R_2 = 16 kΩ, C_1 = 1 pF). The PMOS mirror load (PM0 diode-connected, PM1 active), NMOS differential pair (NM0, NM1), and tail current source I_{SS} = 30 μA are clearly visible.

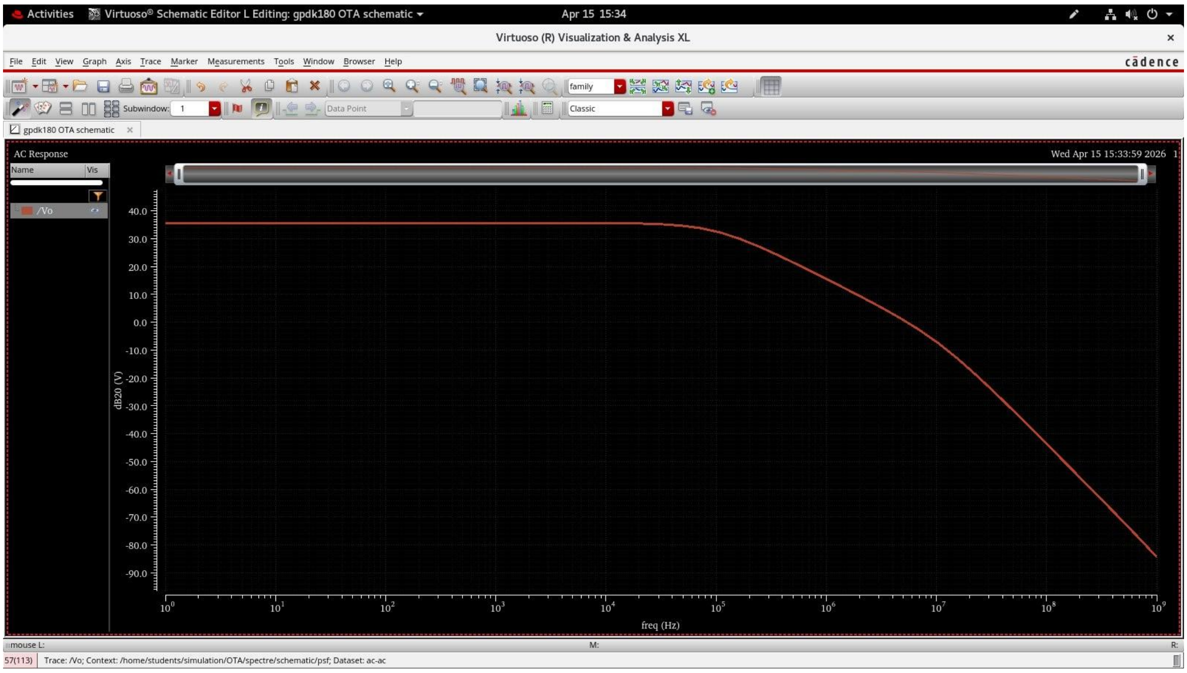

Fig. 5. Cadence Virtuoso Spectre AC response of the complete OTA–RC filter system (gpdk180, 180 nm CMOS, V_{DD} = 1.8 V). Passband gain ≈35 dB flat to ∼10 kHz; −3 dB cutoff at ≈100 kHz; stopband rolloff at −40 dB/decade confirming 2nd order behaviour. Simulation range: 1 Hz – 1 GHz.

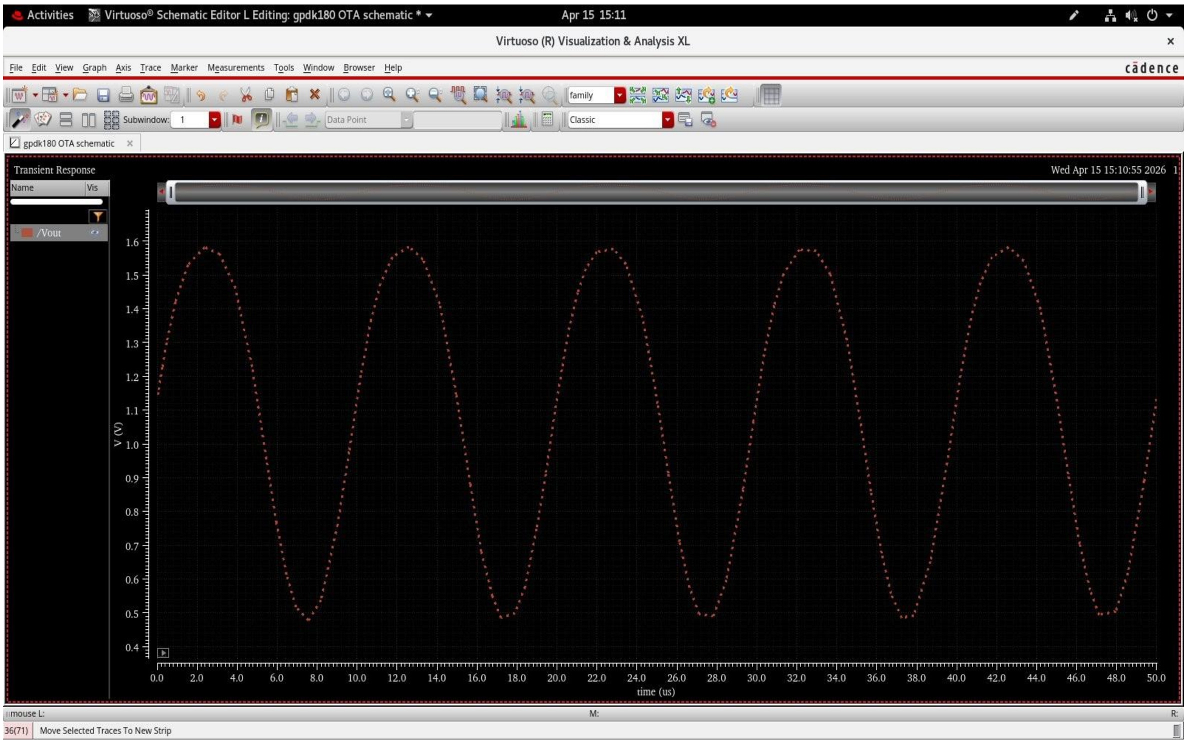

Fig. 6. Cadence Virtuoso Spectre transient response (/Vout) of the OTA output stage (V_{DD} = 1.8 V, I_{SS} = 30 μA, input 50 mV at 100 kHz). Output swings between 0.38 V and 1.57 V (peak-to-peak = 1.19 V, centred at 0.975 V ≈ $V_{DD}/2$), confirming correct biasing and transistor saturation. Simulation window: 0 – 50 μs.