Enhanced Gain and Power Efficiency in CMOS Amplifiers for DAC Applications Using Cascode Current Mirror in 180nm Technology

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***Abstract*—This paper presents the design of low-power, high-gain CMOS amplifiers in 180nm technology using Cadence Virtuoso for Digital to Analog Converter (DAC) interface applications. Various topologies, including common-source stages, cascode structures, and two-stage operational amplifiers, are analyzed. A cascode current mirror is introduced to replace the conventional active load, improving output impedance and voltage gain with minimal power increase. The proposed two-stage operational amplifier achieves a gain of 61.42 dB while consuming 72.61 µW at a 1.8 V supply. Compared to a 130nm baseline design, the proposed implementation offers up to 17 dB higher gain and approximately 89% lower power consumption, making it suitable for DAC and mixed-signal applications.**

***Index Terms*—Common source amplifier, differential amplifier, operational amplifier, resistive load, active load, current mirror, gain, power dissipation.**

I. INTRODUCTION

Growing demand for energy-efficient, high-performance analogue front-ends in mixed-signal systems has placed amplifier design at the forefront of modern IC research. Within data converter architectures — particularly DACs — the output amplifier directly governs key system-level parameters such as signal linearity, output settling behaviour, and overall fidelity. Achieving simultaneously high voltage gain and low power dissipation in scaled CMOS nodes continues to be a non-trivial engineering challenge.

Among the simplest amplifier configurations, the common-source stage with a resistive drain load is fundamentally constrained in gain by the finite load impedance and transistor output conductance. Replacing the passive resistor with an active current mirror load raises the effective output impedance and thus improves gain. A cascode current mirror load overcomes both limitations: the additional stacked transistor substantially raises the output impedance of the mirror, translating directly into enhanced voltage gain with only a marginal impact on power consumption [7]. The present study undertakes a comparative evaluation of five CMOS amplifier topologies within a 180nm process, all realised in the Cadence Virtuoso environment.

II. LITERATURE SURVEY

Low-power, high-gain CMOS amplifier design has been an active area of research. Surabhi S. P. and Deepa [1] analysed common-source amplifiers, differential amplifiers, and operational amplifiers in 130nm CMOS technology, where the two-stage Op-Amp with active current mirror load achieved a gain of 44 dB at 666.475 µW, establishing a baseline for DAC applications. Yang and Lehmann [8] demonstrated high-gain operational amplifiers in 22nm CMOS, achieving 36.77 dB gain. Kothapalli et al. [10] performed a comparative analysis of different Op-Amp configurations using 180nm CMOS technology, reporting up to 40 dB gain. Deo et al. [6] evaluated output impedance characteristics of BiMOS differential stages loaded with various mirror configurations, establishing that cascode-type mirrors offer the highest output resistance. The foundational design principles for all topologies investigated in this work are drawn from Razavi [11].

III. METHODOLOGY

Five amplifier circuits were realised and characterized in Cadence Virtuoso targeting the 180nm CMOS process node, with a 1.8V supply and a 20 µA reference bias current. Technology parameters adopted for device sizing were: $\mu nCox = 200\ \mu A/V^2$, $\mu pCox = 100\ \mu A/V^2$, and $\lambda = 0.1\ V^{-1}$. Time-domain performance was evaluated using a 5mV sinusoidal stimulus at 1 kHz. Across all topologies, the small-signal voltage gain follows $Av = gm \times Rout$, where gm denotes the transistor transconductance and Rout represents the total output impedance seen at the drain terminal.

A. Common Source Amplifier with Resistive Load

The resistive-load CS stage is the baseline MOSFET amplifier configuration. Parameters: gm = 0.72 mS, RD = 35 kΩ. Measured gain from simulation stands at 17.2 dB at a power budget of 55.026 µW. The 130nm counterpart in [1] achieved 10.68 dB while drawing 725.65 µW — confirming substantially better power efficiency in the proposed 180nm realization.

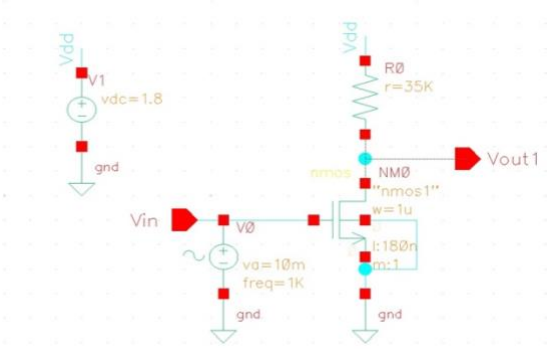


Fig. 1: Schematic of CS Amplifier with Resistive Load

B. Common Source Amplifier with Active Load

Here, the drain resistor is substituted with a PMOS-based current mirror that functions as a high-impedance active load. Parameters: gm = 0.2 mS, Rout = 250 kΩ. The simulated gain is 26.343 dB at 37.62 µW — an improvement over both the resistive-load variant and the 130nm reference (23.74 dB at 500.695 µW).

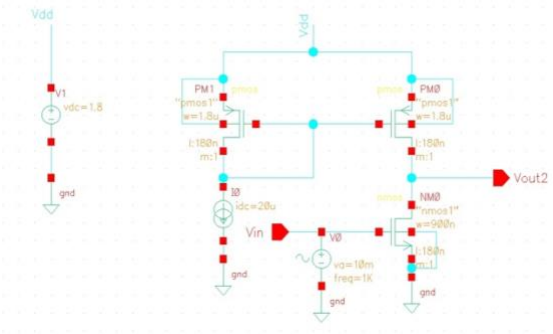


Fig. 2: Schematic of CS Amplifier with Active Current Mirror Load

C. Common Source Amplifier with Cascode Current Mirror

A cascode transistor placed above the standard mirror device elevates the mirror's output impedance by a factor proportional to the intrinsic transistor gain. Parameters: gm = 0.2 mS, Rout = 500 kΩ (elevated via cascode action). Simulation yields 30.89 dB gain at only 35.7 µW — surpassing the simple active-load stage in both gain and power efficiency.

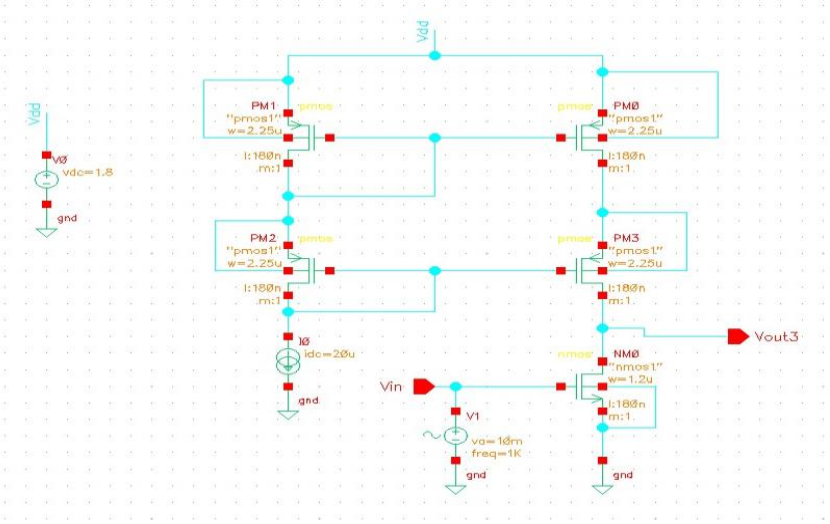


Fig. 3: Schematic of CS Amplifier with Cascode Current Mirror

D. Two-Stage Operational Amplifier with Active Load

A differential pair forms the first gain stage, followed by a CS output stage — both employing current mirror active loads. Parameters: gm1 = 100 µS, Rout1 = 500 kΩ; gm2 = 200 µS, Rout2 = 250 kΩ. The simulated gain is 58.886 dB at 113.616 µW. The 130nm reference in [1] achieved 44 dB at 666.475 µW.

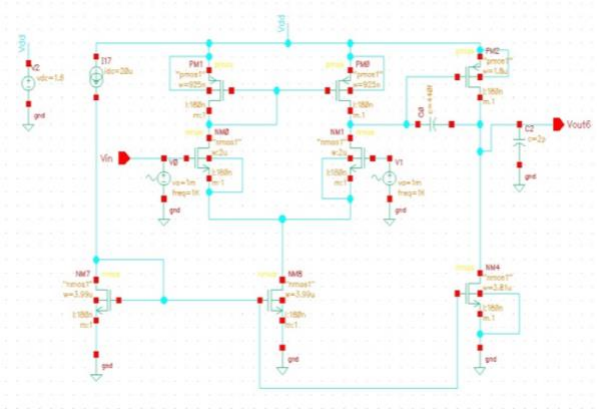


Fig. 4: Schematic of Two-Stage Op-Amp with Active Current Mirror Load

E. Two-Stage Operational Amplifier with Cascode Current Mirror

The highest-performance configuration deploys cascode current mirrors in both amplifier stages, maximizing output impedance at every node. Stage parameters: Rout1 = 1 MΩ; Rout2 = 500 kΩ.

Simulation confirms a gain of 61.421 dB at 72.615 µW.

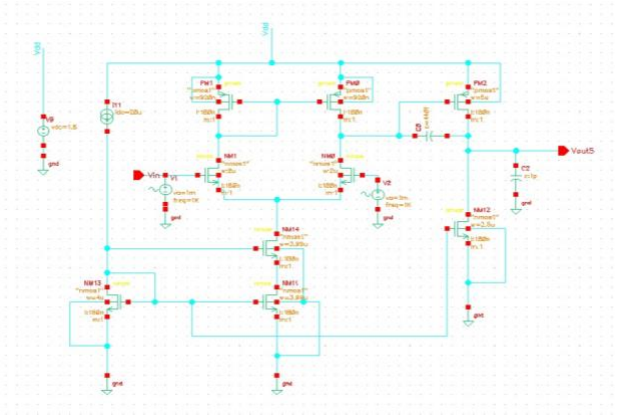


Fig. 5: Schematic of Two-Stage Op-Amp with Cascode Current Mirror

IV. RESULTS AND DISCUSSION

All circuit-level simulations were carried out using the Cadence Virtuoso environment, targeting a 180nm CMOS process with a 1.8V supply. A sinusoidal input signal of 10mV amplitude at 1 kHz was applied for time-domain characterization.

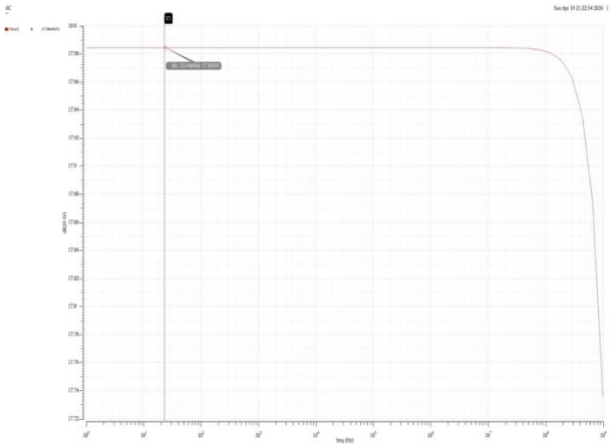


Fig. 6: AC Frequency Response of CS Amplifier with Resistive Load

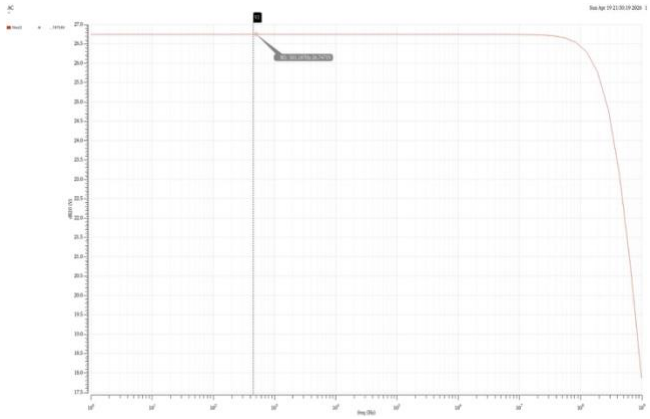


Fig. 7: AC Frequency Response of CS Amplifier with Active Load

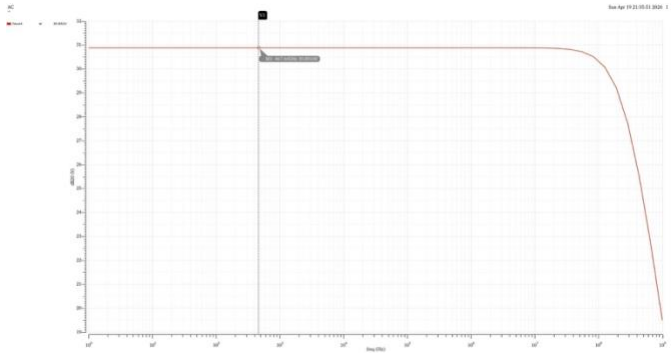


Fig. 8: AC Frequency Response of CS Amplifier with Cascode Current Mirror

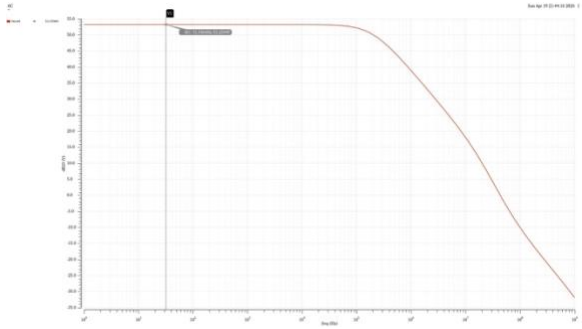


Fig. 9: AC Frequency Response of Operational Amplifier with Active Load

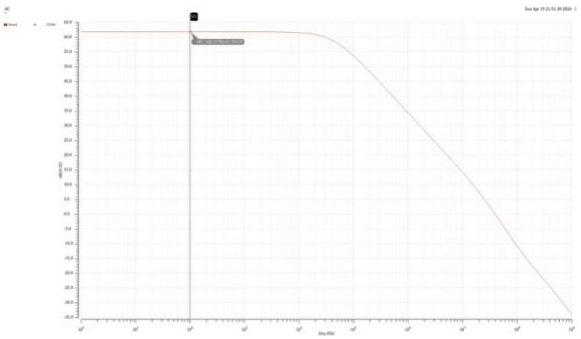


Fig. 10: AC Frequency Response of Operational Amplifier with Cascode Current Mirror

TABLE I: Performance Comparison of CS Amplifier with Previous Works

Specifications	Paper [3]	Paper [13]	Paper [1]	This Work (Active)	This Work (Cascode)
Technology (nm)	90	180	130	180	180
Gain (dB)	27.38	23.5	10.68	26.343	30.89
Power (µW)	1440	56.4	725.65	37.62	35.7
Load	Resistor	Resistor	Resistor	Active Load	Cascode Mirror
Tool	BSIM4	LTSPICE	Mentor Graphics	Cadence	Cadence

TABLE II: Performance Comparison of Operational Amplifier with Previous Works

Specifications	Paper [8]	Paper [10]	Paper [16]	Paper [1]	This Work (Active)	This Work (Cascode)
Technology (nm)	22	180	45	130	180	180
Gain (dB)	36.77	40	47	44	58.886	61.421
Power (µW)	43	10.01	7000	666.475	113.616	72.615
Load	Current Mirror	Wilson Mirror	Current Mirror	Current Mirror	Current Mirror	Cascode Mirror
Stages	1	1	1	2	2	2
Tool	Cadence	Cadence	Tanner	Mentor Graphics	Cadence	Cadence

Discussion

The cascode current mirror topology exhibits a clear advantage over conventional active load designs across both gain and power metrics. The CS amplifier built around a cascode current mirror registers a gain of 30.89 dB at a power draw of just 35.7 µW. Relative to the 130nm active load CS amplifier from [1], this translates to a gain enhancement of 7.15 dB alongside a power saving of approximately 92.9%. The two-stage Op-Amp with cascode current mirror emerges as the top-performing configuration overall, recording 61.421 dB gain while consuming only 72.615 µW. Against the 130nm Op-Amp baseline in [1], the improvement amounts to 17.421 dB in gain and an 89.1% drop in power dissipation.

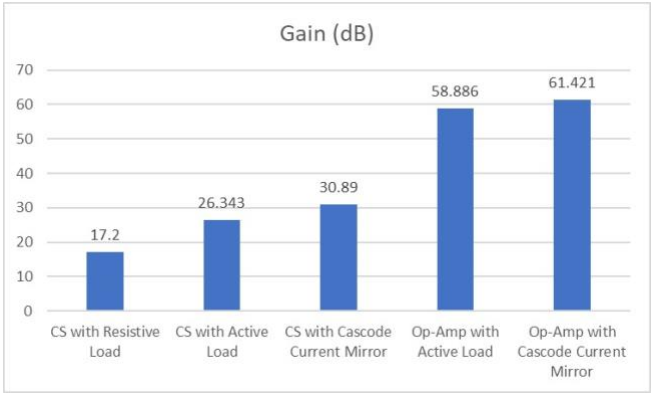
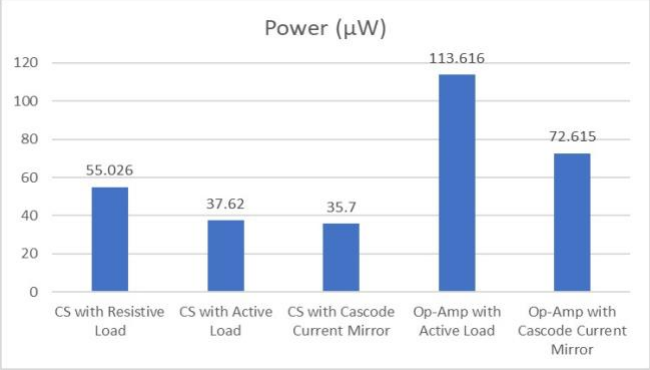


Fig. 11: Comparison of Gain for All Amplifier Topologies

Fig. 12: Comparison of Power Consumption for All Amplifier Topologies

V. IMPLEMENTATION OF DAC USING OP-AMP

Among all the amplifier topologies investigated in this work, the two-stage operational amplifier with cascode current mirror achieved the highest voltage gain of 61.421 dB with the lowest power dissipation of 72.615 µW. This Op-Amp is selected for implementing a 4-bit binary weighted Digital-to-Analogue Converter (DAC) in 180nm CMOS technology using Cadence Virtuoso. The Op-Amp acts as a summing amplifier, combining the weighted input currents to produce a proportional analogue output



voltage. The 4-bit binary weighted DAC accepts four digital input bits (D3, D2, D1, D0) and produces 16 discrete analogue output voltage levels corresponding to all possible binary input combinations from 0000 to 1111.

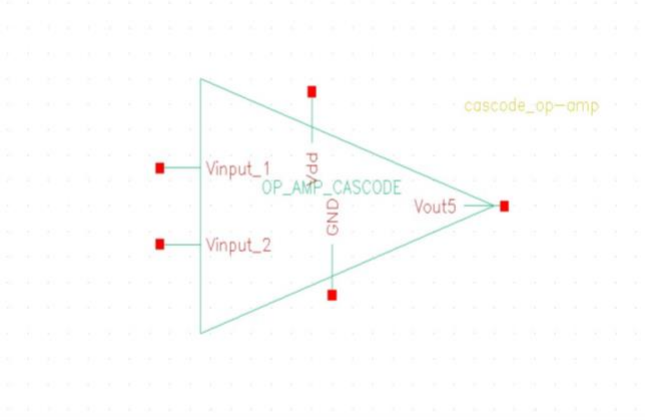


Fig. 13: Symbol of the Op-Amp

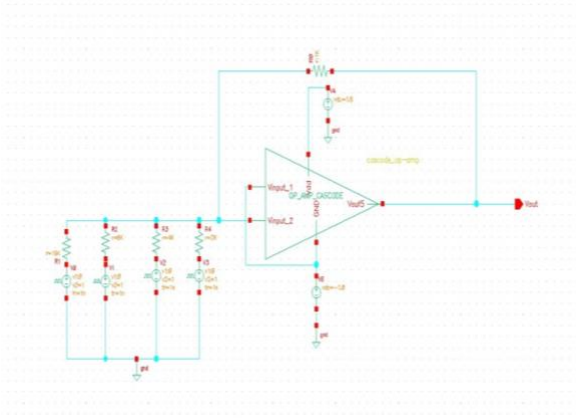


Fig. 14: Test Circuit of 4-bit Binary Weighted DAC

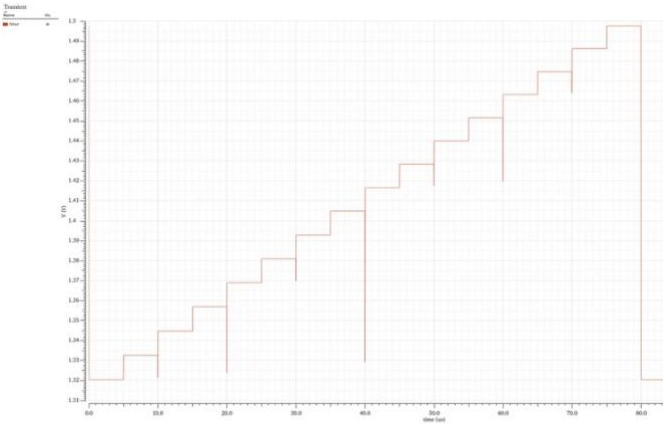


Fig. 15: DAC Output Waveform

VI. CONCLUSION

Five CMOS amplifier architectures were designed, simulated, and benchmarked in 180nm technology using Cadence Virtuoso, to maximize voltage gain while minimizing power consumption for DAC interfacing applications. A consistent finding across all topologies is that operating at a lower supply voltage of 1.8V within the 180nm node yields marked improvements in power efficiency compared to the 2.0V supply required by the 130nm reference. The introduction of cascode current mirror loading further amplifies this advantage by raising the effective output impedance of the gain stage. Among all configurations, the two-stage Op-Amp with cascode current mirror delivered the strongest overall performance: 61.421 dB gain at 72.615 µW, representing a 17.421 dB gain improvement and 89.1% power reduction relative to [1].

VII. FUTURE SCOPE

The proposed cascode current mirror design can be further improved by incorporating advanced gain enhancement techniques such as gain-boosted and telescopic cascode amplifiers. Alternative current

mirror topologies like Wilson and Widlar mirrors can also be explored for comparison. Further optimization using Gm/Id methodology and adaptive biasing can enhance the trade-off between gain, bandwidth, and power efficiency. Additionally, scaling to advanced CMOS nodes (e.g., 90nm or 45nm), implementing higher-resolution DAC architectures, and performing layout and post-layout analysis can improve overall performance, accuracy, and reliability in practical mixed-signal applications.

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