Design and Comparative Analysis of a CMOS Bandgap Voltage Reference Across 180nm, 90nm and 45nm Technologies

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***Abstract*—A stable and temperature-independent voltage reference is a critical requirement in modern mixed-signal CMOS systems. This paper presents the design and optimization of a CMOS Bandgap Reference (BGR) circuit implemented using a self-biased current mirror topology that combines Proportional to Absolute Temperature (PTAT) and Complementary to Absolute Temperature (CTAT) voltage components. The proposed design was initially developed in a 180nm technology node with a 1.8V supply and simulated over a temperature range of −40°C to 200°C. Simulation results show a highly stable reference output with a temperature variation of 11mV and a temperature coefficient of 0.045mV/K under optimized parametric conditions. The design is further migrated to a 90nm technology node where deep-submicron effects, such as channel length modulation, are addressed through the use of non-minimum channel lengths (L = 300nm) and optimized device sizing. This approach achieves improved line regulation and a stable phase margin of 104.03°, ensuring reliability for precision analog applications in scaled CMOS technologies. Additionally, the architecture is extended to a 45nm process where Short Channel Effects play a crucial role, making the simulation more challenging [10].**

***Index Terms*—Bandgap Reference (BGR), CMOS, 180nm, 90nm, Temperature Coefficient, PSRR, Channel Length Modulation.**

I. INTRODUCTION

In modern System-on-Chip (SoC) design, analog and mixed-signal components such as Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs), and power management units require a stable and precise voltage reference to ensure reliable operation. The Bandgap Reference (BGR) circuit is widely adopted for this purpose due to its ability to generate a temperature-independent reference voltage by exploiting the inherent properties of semiconductor devices. A conventional BGR achieves this by combining two voltage components with opposite temperature coefficients: a Complementary to Absolute Temperature (CTAT) voltage, typically derived from the base-emitter voltage of a diode-connected transistor, and a Proportional to Absolute Temperature (PTAT) voltage. By appropriately scaling these components using resistor ratios, a near Zero Temperature Coefficient (ZTAT) reference voltage can be obtained.

However, with the continuous scaling of semiconductor technology into deep-submicron nodes such as 90nm, the design of stable and accurate voltage references has become increasingly challenging. Short-channel effects, particularly Channel Length Modulation (CLM), significantly reduce the output resistance of transistors, thereby degrading the performance of current mirrors used in conventional BGR circuits. As a result, the circuit becomes more sensitive to variations in supply voltage, leading to poor line regulation and a reduced Power Supply Rejection Ratio (PSRR). These issues make traditional BGR architectures less suitable for precision applications in advanced technology nodes.

Existing BGR designs that perform adequately in larger process technologies, such as 180nm, often fail when directly migrated to smaller nodes without appropriate modifications. This is primarily due to changes in device characteristics that are not accounted for in conventional design methodologies. Although several techniques have been proposed to

improve thermal stability and PSRR, they often involve increased circuit complexity, higher power consumption, or additional compensation mechanisms. To address these challenges, this work proposes a robust BGR architecture that maintains consistency in performance across multiple technology nodes, including 180nm, 90nm, and 45nm. The proposed design employs a combination of non-minimum channel lengths to mitigate short-channel effects and restore high output resistance in current mirrors. In addition, optimized resistor ratios and diode scaling are utilized to achieve improved temperature stability and reduced sensitivity to supply variations. The design is validated through simulations, demonstrating stable reference voltage behavior over a wide temperature range. The main objective of this study is to analyze and compare the performance of the proposed BGR circuit across different process technologies using Cadence Virtuoso simulations. This work includes mathematical modeling for parameter optimization, stability analysis using frequency response techniques, and evaluation of noise immunity through AC and transient analyses. Furthermore, design strategies to overcome deep-submicron limitations are discussed, providing practical insights for scalable and reliable voltage reference design [11].

II. LITERATURE SURVEY

2.1 Conventional Bandgap Reference Circuits

Conventional Bandgap Reference (BGR) circuits operate by summing two voltages with opposing temperature coefficients to achieve a stable, temperature-independent output. This technique balances a Complementary to Absolute Temperature (CTAT) component with a Proportional to Absolute Temperature (PTAT) component. CTAT Component the CTAT voltage is typically derived from the base-emitter voltage (VBE) of a forward-biased diode-connected transistor. Temperature Behavior: VBE naturally exhibits a negative temperature coefficient, typically decreasing by approximately -1.5 to -2.0 mV/°C as temperature rises. Observed Range: In a 180nm process, VBE can range from approximately 988 mV at -40°C to 811 mV at 200°C.

PTAT Component the PTAT voltage is generated by calculating the difference (ΔVBE) between the base-emitter voltages of two diode branches operating at different current densities. Generation: This difference is created by using an array of diodes in one branch versus a single diode in the other. Formula: $\Delta VBE = VT \ln(n)$, where VT is the thermal voltage and n is the ratio of the diode areas. Scaling: This voltage is dropped across a resistor (R1) to generate a PTAT current, which is then scaled by another resistor (R2).

Summation and Reference Output (Vref) In legacy technology nodes like 180nm, self-biased current mirrors are used to combine these parts into a stable reference voltage, traditionally aiming for the 1.2V bandgap energy of silicon. Optimization: The final output is governed by the equation: $Vref = VBE + (R2/R1)\, VT \ln(n)$.

Empirical Data: A diode multiplier of n = 10 and a resistor ratio of 8.033 can reduce voltage deviation to about 0.098V over extreme temperature sweeps for a 180nm design with a supply voltage of 1.8V. Precision: A temperature coefficient of 0.045 mV/K can be obtained by reducing overall variance to as small as 11 mV over a range of -40°C to 200°C under well optimized parametric circumstances.

2.2 Advanced BGR Design Techniques

Modern BGR designs focus on sub-1V operation and advanced curvature compensation to handle non-linearities in V_{BE}.

- Structural Improvements: Researchers utilize cascade current mirrors to boost output resistance (r_o) and counter act channel length modulation in deep-submicron nodes like 90nm.
- Optimization: Reaching a Zero Temperature Coefficient (ZTAT) requires precise parametric tuning of the resistor ratio (R_2/R_1) and diode area multiplier (n). Data shows that as n increases the required R_2/R_1 ratio de-creases to maintain stability.
- Stability: Frequency-domain analysis is now a standard requirement (for eg. the 90nm node simulation achieved a Phase Margin of 104.03° at 176.86 MHz) ensuring the circuit does not oscillate under dynamic conditions.

2.3 Challenges in Deep-Submicron CMOS

Moving BGR designs to smaller technologies like 90nm creates difficultly in analog design problems. The biggest issue is Channel Length Modulation. When transistors get shorter their output resistance (r_o) drops significantly. This makes current mirrors less accurate and causes poor line regulation meaning changes in the power supply (V_{DD}) directly affect the reference output (V_{ref}). Meanwhile, smaller nodes have less voltage headroom making it hard to use traditional cascade structures.

2.4 Research Gap and Motivation

While BGR architectures are well-documented for larger nodes a significant gap exists in maintaining the precision during direct implementation to 90nm without excessive circuit complexity. Existing research often prioritizes 180nm designs or highly specialized sub-1V versions that are not suitable for standard 1.8V analog applications. This work is to demonstrate the output of BGR at different technology nodes to see the performance at different size which introduces more problem and how to tackle them.

III. METHODOLOGY

3.1 Theoretical Formulation

A Zero Temperature Coefficient (ZTAT) reference voltage is achieved by intelligently combining a Complementary to Absolute Temperature (CTAT) voltage and a Proportional to Absolute Temperature (PTAT) voltage.

The CTAT component is derived from the base-emitter voltage (VBE) of a forward-biased diode-connected BJT. The temperature variation (slope) of VBE is experimentally known to be negative:

$$\frac{\Delta V_{BE}}{\Delta T} \approx -1.6\ \text{mV/°K} \qquad (1)$$

[1] [3] The PTAT component is generated by the difference in base-emitter voltages (ΔVBE) between two diode branches operating at different current densities. De-rived from the standard diode current equation (ID = ISeVD/VT), the difference is:

$$\Delta V_{BE} = V_T \ln(n) \qquad (2)$$

where n is the ratio of the diode areas and VT = kT/q is the thermal voltage.

This ΔVBE is dropped across resistor R1 to create a PTAT current, which is mirrored and multiplied by resistor R2. The resulting PTAT voltage variation with respect to temperature is defined as:

$$\frac{\Delta V_{R2}}{\Delta T} = \frac{R_2}{R_1} \times \ln(n) \times \frac{k}{q} \qquad (3)$$

Given that k/q ≈ 86.25 μV/◦K, the equation becomes:

$$\frac{\Delta V_{R2}}{\Delta T} = \frac{R_2}{R_1} \times \ln(n) \times 86.25 \times 10^{-6}\ \text{V/°K} \qquad (4)$$

To achieve a temperature-independent output voltage, the magnitudes of the PTAT and CTAT slopes must be perfectly equated:

$$1\frac{\Delta V_{BE}}{\Delta T}1 = \frac{\Delta V_{R2}}{\Delta T} \qquad (5)$$

Substituting the known values yields the foundational de-sign equation:

$$1.6 \times 10^{-3} = \frac{R_2}{R_1} \times \ln(n) \times 86.25 \times 10^{-6} \qquad (6)$$

This formula allows to extract the precise R2/R1 resistor ratio required for any given diode multiplier n. For in-stance, selecting n = 3 yields a required R2/R1 ratio of 16.836 [1] [3] [2].

3.2 Circuit Architecture

The proposed BGR circuit employs a self-biased current mirror to enforce equal current distribution across the two primary branches. Figure 3 illustrates the complete schematic which is used to observe the Parametric Optimization of Resistor Ratios and Corresponding Reference Voltage Variations.

3.2.1 180nm Baseline Architecture

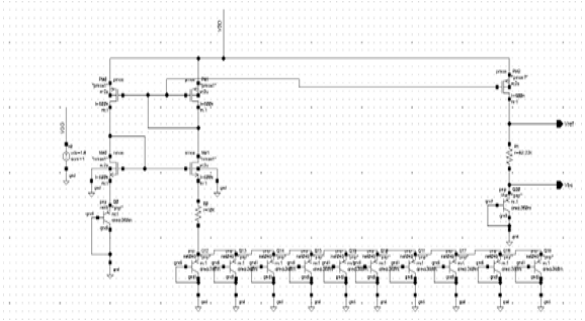

Figure 1: Complete circuit schematic for the 180nm technology node.

3.2.2 90nm Optimized Architecture

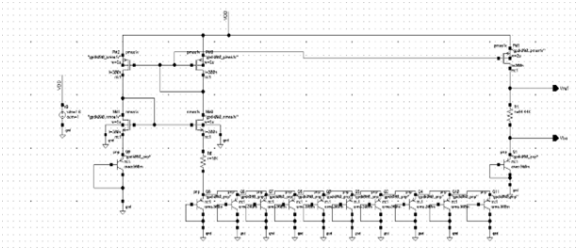

Figure 2: Optimized circuit schematic for the 90nm technology node using non-minimum channel lengths.

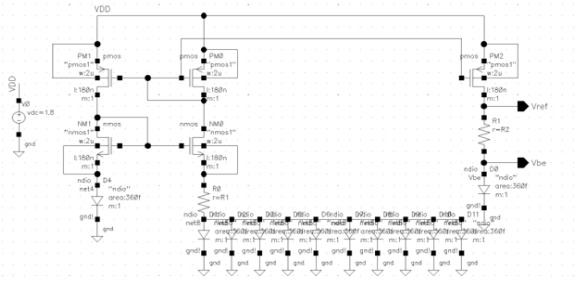

Figure 3: CMOS Bandgap Reference Circuit utilizing a self-biased current mirror and diode arrays.

3.3 Parametric Optimization

Using the derived mathematical model, the R_2/R_1 ratio was systematically calculated for various diode area multipliers ranging from n = 3 to n = 10. The circuit was then simulated to observe the absolute Maximum and Minimum variations in V_{ref} over extreme temperature sweeps. Table 1 summarizes the theoretical ratios and the resulting empirical voltage deviations (ΔV_{ref}).

Table 1: Parametric Optimization of Resistor Ratios and Corresponding Reference Voltage Variations

n	R_2/R_1	V_{ref} MAX (V)	V_{ref} MIN (V)	ΔV_{ref} (V)
3	16.836	1.287	1.076	0.211
4	13.345	1.282	1.106	0.176
5	11.490	1.272	1.121	0.151
6	10.323	1.265	1.130	0.135
7	9.505	1.258	1.137	0.121
8	8.895	1.253	1.141	0.112
9	8.418	1.249	1.145	0.104
10	8.033	1.245	1.147	0.098

As observed in Table 1, the required resistor ratio R_2/R_1 holds an inversely proportional relationship with the diode area multiplier n. Crucially, scaling the diode array up to n = 10 minimizes the total voltage deviation (ΔV_{ref} = 0.098 V), establishing it as the most stable parametric choice for suppressing temperature coefficients.

IV.RESULTS AND DISCUSSION

4.1 Simulation Setup

To evaluate the performance of the BGR architectures simulations were executed using the Cadence Virtuoso Analog Design Environment (ADE). Temperature stability was assessed via DC temperature sweeps ranging from −40°C to 200°C, allowing for the precise value of the Temperature Coefficient (TC) and peak-to-peak V_{ref} variation. Also, AC frequency response (stb) analysis was performed to verify the phase margin and overall feedback loop stability. Then finally, transient simulations were conducted to validate reliable start-up behavior and the dynamic settling of V_{ref} and V_{BE} under varying thermal conditions.

4.2 Results for 180nm Technology

The proposed BGR circuit was initially implemented in a 180 nm CMOS technology with a supply voltage of 1.8 V. The design was analyzed through a sequence of simulations to verify resistor selection, temperature stability, DC operating point, and overall circuit stability.

Resistor Selection: The resistor values were optimized to achieve a near Zero Temperature Coefficient (ZTAT) condition. By tuning the ratio R_2/R_1, the PTAT and CTAT components were properly balanced, resulting in a stable reference voltage.

Parametric Analysis with Respect to Temperature: A temperature sweep from −40°C to 200°C was performed to evaluate thermal stability. The reference voltage varied largely, at a range of around 1.075 V to

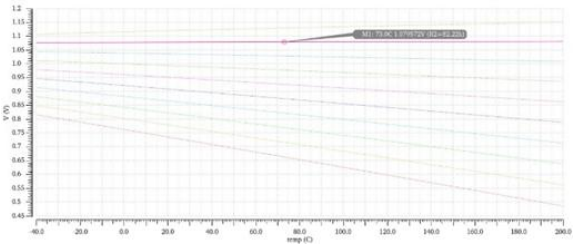

Figure 4: Resistor selection and tuning for optimal V_{ref}

1.0815 V for Vref and 286 mV to 780 mV for VBE this was for checking the variation of Voltage at diffrent par-ticular temperature which helped in finding the min and max value to find the slope.

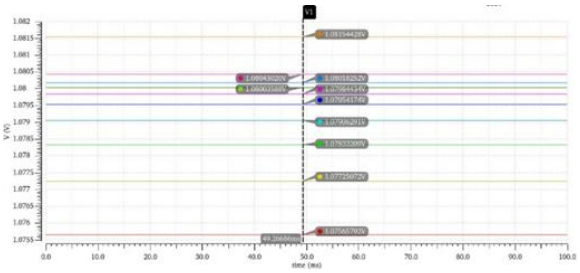

Figure 5: Temperature variation of V_{ref} for 180 nm

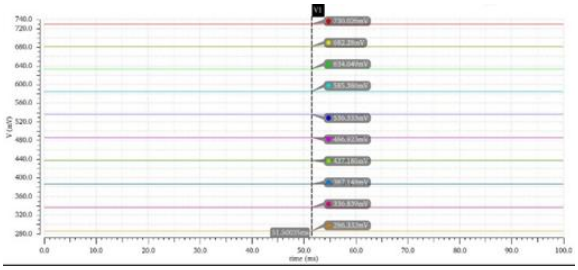

Figure 6: Temperature variation of V_{BE} for 180 nm

DC Analysis: DC simulations confirmed that the circuit operates at the intended bias point, producing a sta-ble reference voltage of approximately 1.1 V under nominal conditions.

Stability Analysis: Frequency response analysis was conducted to evaluate the stability of the circuit. The design exhibited a high phase margin, indicating a stable operation without oscillations.

Results for 90nm Technology

The proposed BGR circuit was migrated to the 90nm technology node using a supply voltage of 1.4V. The performance was evaluated through a sequence of simulations

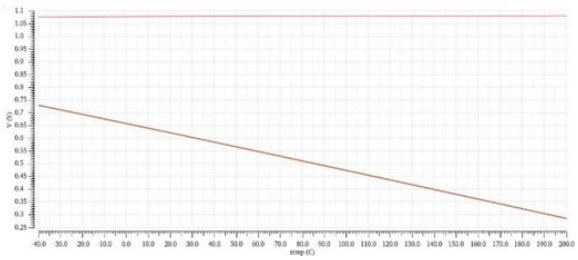

Figure 7: DC analysis of 180nm showing steady-state reference voltage

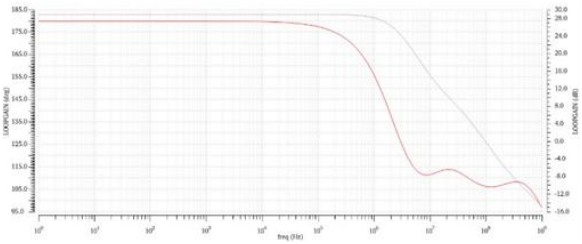

Figure 8: Stability analysis of 180nm showing phase margin of the circuit

to verify resistor selection, thermal stability, and DC operating points.

Resistor Selection: The resistor values were optimized to achieve a near Zero Temperature Coefficient (ZTAT) condition. By tuning the ratio R_2/R_1, the PTAT and CTAT components were properly balanced, resulting
in a stable reference voltage. In this simulation the optimum

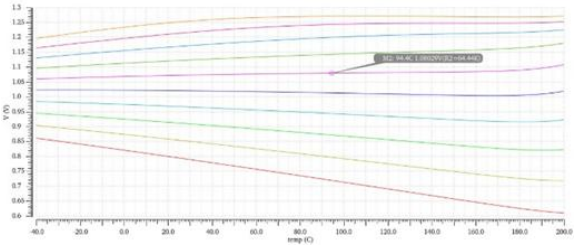

Figure 9: Resistor selection and tuning for optimal V_{ref}

Parametric Analysis with Respect to Temperature: A temperature sweep from −40°C to 200°C was performed to evaluate thermal stability. The reference voltage varied largely, at a range of around 1.060, V to 1.108 V for Vref and 342.8 mV to 756.9 mV for VBE this was for checking the variation of Voltage at different particular temperature which helped in finding the min and max value to find the slope.

DC Analysis: DC simulations confirmed that the circuit operates at the intended bias point, producing a stable reference voltage of approximately 1.07 V under nominal conditions.

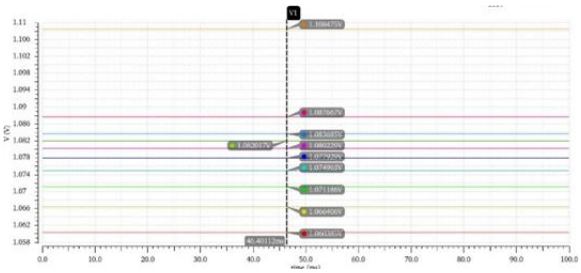

Figure 10: Temperature variation of V_{ref} for 90 nm

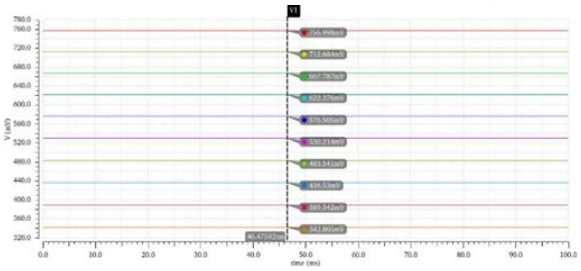

Figure 11: Temperature variation of V_{BE} for 90 nm

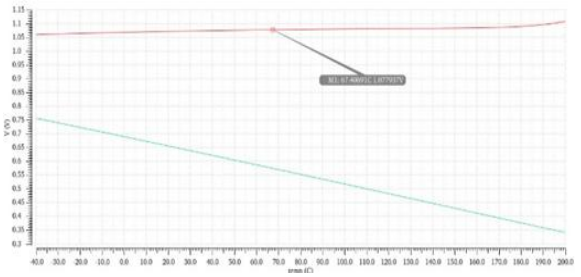

Figure 12: DC analysis of 90nm circuit showing steady-state reference voltage

Stability Analysis: Frequency response analysis was conducted to evaluate the stability of the circuit. The design exhibited a moderate phase margin, indicating a somewhat stable operation without oscillations. Check Figure 13

Results for 45nm Technology

The proposed BGR circuit was migrated to the 45nm technology node using a standard supply voltage of 1.5 V practically you can't give this high input but in Cadence below 1 V all MOSFETs are going in Subthreshold region. The performance was evaluated through a sequence of simulations to verify resistor selection, thermal stability, and DC operating points under deep-submicron constraints.

Parametric Analysis with Respect to Temperature: A temperature sweep from −40°C to 200°C was

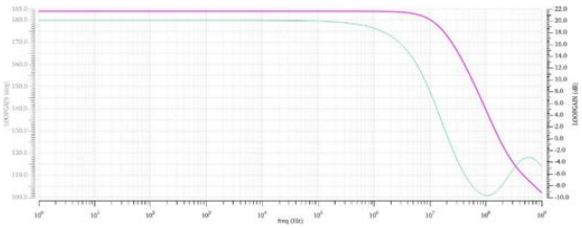

Figure 13: Stability analysis showing phase margin of the 90nm circuit

performed to evaluate temperature stability. The reference voltage (V_{ref}) exhibits excellent regulation, varying by only 11 mV (from approximately 1.06 V to 1.07 V), which shows a highly stable slope of 0.045 mV/K. Also, the base-emitter voltage (V_{BE}) varied linearly from approximately 868.6 mV down to 540.0 mV, demonstrating the expected CTAT behavior across the temperature extremes.

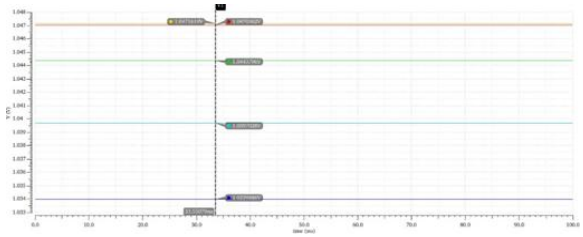

Figure 14: Temperature variation of V_{ref} for 45 nm

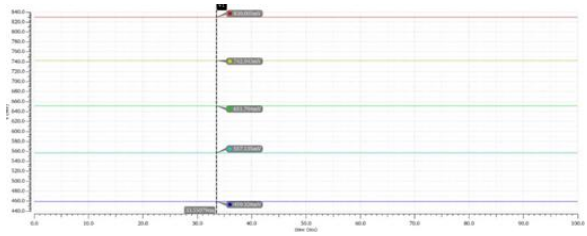

Figure 15: Temperature variation of V_{BE} for 45 nm

DC Analysis: DC Analysis confirmed that the circuit operates exactly at the intended bias point despite the technology node, producing a stable steady-state reference voltage of approximately 1.068 V under nominal conditions.

Transient and Stability Analysis: Transient response and stability simulations were conducted to evaluate the dynamic operation of the circuit. The design exhibited a reliable start-up sequence, settling rapidly to the nominal 1.068 V reference without sustained oscillation, indicating a stable phase margin and robust operation.

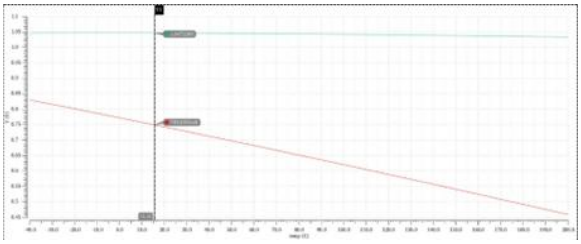

Figure 16: DC analysis showing steady-state reference voltage at 45nm

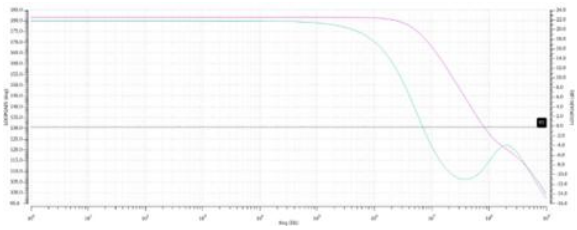

Figure 17: Transient and stability analysis of the 45nm BGR circuit

The stability analysis for the baseline 180nm node demonstrated a robust phase margin and a highly stable feedback loop. Upon migration to the 90nm node, the circuit maintained excellent stability with a Phase Margin of 104.03° at 176.86 MHz. Similarly, the 45nm architecture exhibited a stable, over-damped response with a Phase Margin exceeding 115° at a unity-gain frequency of approximately 80 MHz. Transient analysis across all three nodes showed reliable start-up without sustained oscillations, ensuring robust operation under dynamic conditions.

Table 2: Simulation Results Across Technology Nodes

Node	L	W	Vdd	Bias Current	ΔV_{ref}
180nm	600nm	2µm	1.8 V	5.5µA	5.5 mV
90nm	300nm	2µm	1.5 V	6.8µA	48 mV
45nm	45nm	120nm	1.5 V	5.3µA	14 mV

Results for 90nm & 45nm Technology with VDD 1.8 V

The DC temperature sweeps, conducted from -40°C to 200°C with a unified 1.8V supply voltage (V_{DD}), high-light the successful PTAT and CTAT compensation. In both circuits, the base-emitter voltage (V_{BE}) exhibits a highly linear Complementary to Absolute Temperature (CTAT) profile. As observed in the 45nm node, V_{BE} de-creases uniformly from 836.6 mV at -40°C down to 466.2 mV at 200°C. The 90nm node an equal and linear voltage drop across the same temperature range. The compensated reference voltage (V_{ref}) demonstrates 90nm architecture achieving a highly stable nominal V_{ref} centered at around 1.25V with minimal deviation. Remarkably, the 45nm design, despite utilizing low-threshold-voltage (lvt) devices and facing heightened short-channel effects, maintains excellent thermal immunity. Its V_{ref} is tightly confined between 1.137 V and 1.119 V

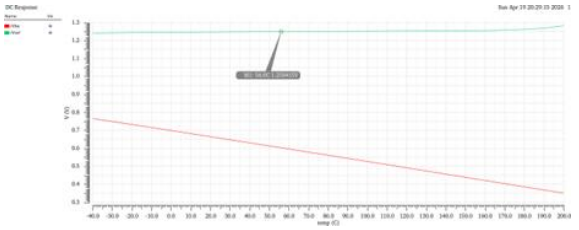

Figure 18: DC Analysis of 90nm circuit with VDD of 1.8V

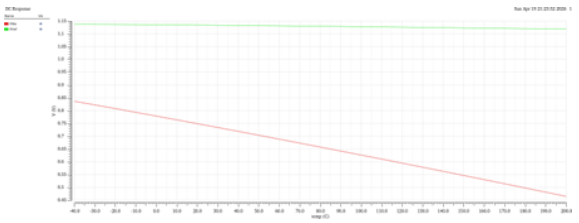

Figure 19: DC Analysis of 45nm circuit with VDD of 1.8V

V. CONCLUSION

This paper successfully demonstrated the design, optimization, and comparative analysis of a CMOS Bandgap Voltage Reference (BGR) circuit across 180nm, 90nm, and 45nm technology nodes. The primary objective of achieving a robust, temperature-independent reference voltage was met by implementing a self-biased cur-rent mirror topology that effectively balanced PTAT and CTAT components. The performance of the BGR circuit was highly consistent across the migration process. In the baseline 180nm node, the circuit produced a standard reference voltage (V_{ref}) of approximately 1.1 V. As the design was scaled down, strategic parametric tuning was required; the 90nm implementation yielded

a stable V_{ref} of approximately 1.07 V, and the 45nm node produced a steady V_{ref} of 1.03 V. Across the wide temperature sweep of -40°C to 200°C, the optimized 45nm architecture maintained a remarkably low peak-to-peak voltage variation of just 14 mV, translating to an excellent temperature coefficient of 0.058 mV/K. The feasibility of migrating the BGR architecture into deep-submicron domain was successfully demonstrated through sequential scaling to the 90nm and 45nm nodes. To overcome the severe voltage headroom constraints inherent in the 45nm process, the design specifically utilized low-threshold-voltage core devices (nmos1vlvt and pmos1vlvt). Despite the short-channel effects associated with operating at minimum channel lengths, the core self-biased topology, combined with precise resistor tuning, successfully preserved the reference stability without com-promising the fundamental architecture.

Furthermore, frequency response analysis confirmed the dynamic robustness of the circuit across these advanced nodes. The 90nm implementation achieved a stable Phase Margin of 104.03°, while the 45nm node exhibited a heavily over-damped feedback loop with a Phase Margin exceeding 115°, ensuring reliable start-up and the complete absence of transient ringing or sustained oscillations.

VI. FUTURE SCOPE

Future work will focus on addressing the voltage head-room limitations encountered in advanced nodes by transitioning to a Current-Mode Bandgap architecture. This shift will enable the circuit to operate reliably on a 0.9V supply, which is a major requirement for true sub-1V, low-power applications.
To further precision, advanced curvature compensation techniques will be checked out. Implementing strategies such as piecewise-linear compensation or beta-compensation will allow for the suppression of the non-linear temperature drift inherent in BJTs, which currently acts as a bottleneck for high-end accuracy. By analyzing the impact of routing resistance, capacitance, and device matching, a more realistic evaluation of the Phase Margin and Power Supply Rejection Ratio (PSRR) can be achieved. This ensures the design re-mains robust against the physical non-idealities of deep sub-micron environments.
Also, adding dedicated start-up circuitry and frequency compensation networks to enhance the transient response of the 45nm BGR represents a critical area for future technological advancement.

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