Design And Simulation of High Speed and Low Power Analog to Digital Converter

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***Abstract*—This paper presents the design and simulation of a high-speed, low-power Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) using RTL modelling. The SAR architecture is chosen for its efficient conversion mechanism and reduced hardware complexity. To support high-speed data transfer, a modified JESD204B interface is incorporated, focusing on simplified control and reduced implementation overhead. The system is described using Verilog HDL and simulated using FPGA design tools. The results confirm accurate analog-to-digital conversion along with improved data transmission efficiency and reduced power consumption. The proposed design is suitable for modern communication and embedded applications.**

***Index Terms*—SAR ADC, RTL Modelling, Low Power Design, Simulation, Modified JESD204B Interface, High-Speed Data Conversion**

I. INTRODUCTION

Analog-to-Digital Converters (ADCs) form a crucial interface between real-world Analog signals and digital processing systems. With the rapid advancement of communication and signal processing applications, there is an increasing demand for ADCs that offer high speed, low power consumption, and reliable performance. Among the various ADC architectures, the Successive Approximation Register (SAR) ADC has gained significant attention due to its balanced trade-off between speed, accuracy, and hardware simplicity. The SAR ADC operates based on a binary search algorithm, where the input signal is approximated in a step-by-step manner from the Most Significant Bit (MSB) to the Least Significant Bit (LSB). This approach eliminates the need for complex parallel structures, thereby reducing power consumption and circuit complexity. As a result, SAR ADCs are widely used in applications requiring efficient data conversion with moderate resolution and speed. However, in high-speed systems, the challenge extends beyond conversion accuracy to efficient data transfer. Traditional parallel data transmission methods increase wiring complexity and may lead to signal integrity issues. To address this, high-speed serial communication techniques are often considered. In this work, a modified JESD204B interface is introduced, where essential features of the standard are adapted to simplify the data transmission process while maintaining effective performance. The proposed work focuses on the design and simulation of a SAR ADC using RTL modelling. The objective is to achieve the accurate Analog-to-digital conversion with reduced complexity while enabling efficient data handling through the modified interface. The simulation-based approach allows detailed analysis of system behaviour, ensuring correctness of operation and validating the effectiveness of the proposed design.

II. METHODOLOGY

The methodology adopted in this work focuses on the design and simulation of a Successive Approximation Register (SAR) ADC using RTL modelling techniques, along with the incorporation of a modified JESD204B interface for efficient data transmission. The design process begins with the mathematical representation of Analog-to-Digital conversion, where the input signal is quantized into discrete digital levels based on the reference voltage and resolution. The core architecture of the SAR ADC consists of a Sample and Hold circuit, comparator, Digital-to-Analog Converter (DAC), SAR register, and control logic. During operation, the input signal is first sampled and held constant. The SAR logic then initiates the conversion process by setting the Most Significant Bit (MSB)

and generating a trial digital code. This code is converted into an Analog voltage using the DAC and compared with the input signal using the comparator. Based on the comparison result, each bit is either retained or reset. This iterative process continues until all bits are determined, resulting in the final digital output. The entire system is modelled at the Register Transfer Level using Verilog HDL. Each functional block is designed in a modular manner to ensure clarity, scalability, and ease of verification. The control logic coordinates the sequence of operations using clock signals, ensuring proper synchronization between sampling, comparison, and bit decision processes. To address the challenges of high-speed data transfer, a modified JESD204B interface is integrated into the system. Unlike the conventional implementation, the modified interface focuses on simplified data framing and reduced control overhead, making it suitable for simulation-based analysis. The parallel digital output of the SAR ADC is converted into a serialized data stream, reducing the number of interconnections and improving data handling efficiency. Simulation is carried out by applying test input signals and observing the corresponding digital outputs. Waveform analysis is used to verify the correctness of the conversion process and to study the timing behaviour of the system. The methodology ensures that the designed SAR ADC operates accurately while maintaining low complexity and efficient data transmission. In addition, the design approach emphasizes systematic verification at each stage to ensure reliable operation of individual modules before integration. The modular structure also allows easy modification and testing of different parameters such as resolution and input range, making the methodology adaptable for various application requirements.

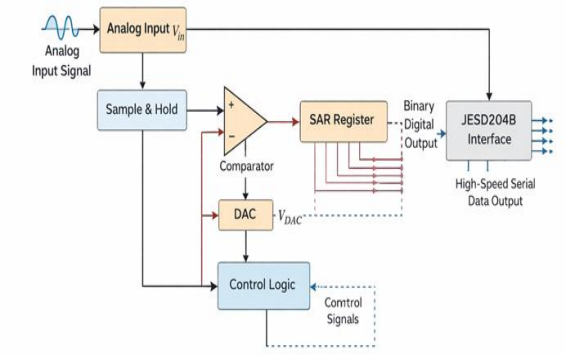


Figure1: Block Diagram of Proposed SAR ADC with Modified JESD204B Interface

III. IMPLEMENTED DESIGN

The proposed SAR ADC system is modelled using Register Transfer Level (RTL) design techniques in Verilog Hardware Description Language. The simulation model is structured into multiple functional blocks, including the Sample and Hold circuit, comparator, Digital-to-Analog Converter (DAC), SAR register, and control logic. Each block is designed independently and then integrated to form the complete ADC System. During simulation, the Analog input signal is represented in digital form and applied to the system. The Sample and Hold circuit capture the input signal, ensuring it remains constant throughout the conversion process. The SAR logic initiates the conversion by setting the Most Significant Bit (MSB) and generating a trial code. The DAC converts this trial code into an equivalent Analog voltage, which is then compared with the input signal using the comparator. Based on the comparator output, the SAR register updates the digital code by retaining or resetting each bit. This process continues sequentially for all bits until the final digital output is obtained. The entire operation is controlled by clock signals, ensuring proper timing and synchronization between all functional blocks. The modified JESD204B interface is included in the simulation model to demonstrate high-speed data transmission. The parallel digital output generated by the SAR ADC is converted into a serialized data stream using simplified control logic. This modification reduces the complexity of standard JESD204B implementation while maintaining efficient data transfer. Simulation is performed using waveform analysis, where input signals and corresponding digital outputs are observed over time. The results confirm that the SAR ADC accurately performs Analog-to-Digital conversion and that the modified JESD204B interface successfully transmits the output data. Additionally, the modular design of the simulation model allows easy verification of individual components as well as the complete system. This approach ensures flexibility for future modifications and enables efficient analysis of system performance under different input conditions. Furthermore, the simulation model is designed to evaluate the dynamic behaviour of the SAR ADC under different input conditions. Various input signal levels are applied to observe the step-by-step bit approximation and convergence of the

digital output. This detailed analysis helps in validating the reliability of the proposed design and confirms that the system performs consistently across different operating scenarios. The simulation also highlights the impact of clock frequency on the conversion process, where each clock cycle corresponds to one bit decision in the SAR logic. Careful observation of the waveform ensures that no timing violations occur during data propagation. This analysis further confirms that the proposed design maintains stable operation and consistent performance under different input conditions.

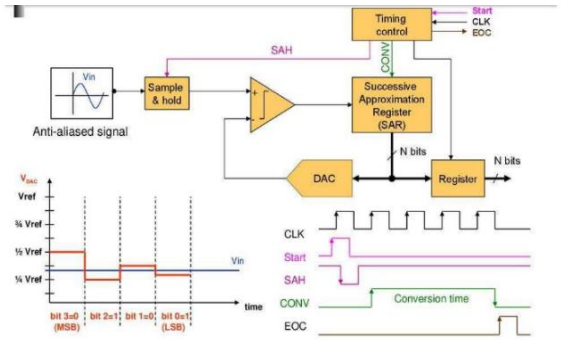


Figure 2: Simulation Model and Timing Diagram of SAR ADC

IV. RESULT&DISCUSSION

The proposed SAR ADC system is analysed through functional simulation to verify its performance and accuracy. Input signals are applied, and the corresponding digital outputs are observed. The waveforms demonstrate the step-by-step approximation process from MSB to LSB, confirming accurate conversion of the input signal. The results show a clear relationship between input and output signals. The staircase behaviour of the DAC output indicates convergence towards the input during each clock cycle, while timing signals ensure proper synchronization and reliable operation. The design also achieves reduced complexity and efficient resource utilization due to the absence of parallel comparator structures, resulting in lower power consumption. The integration of the modified JESD204B interface improves data transmission by converting parallel output into a serialized format, reducing interconnections and enhancing signal integrity. Compared to the traditional SAR ADC, the proposed system provides better data handling, reduced complexity, and improved synchronization, making it suitable for high-speed and low-power applications.

Figure 3: Simulation Waveform of

Proposed SAR ADC

The simulation of the proposed ADC design is performed using Xilinx Vivado. The waveform shows the relationship between the input signal, clock, and digital output. It is observed that the ADC successfully converts the input signal into corresponding digital values. The output follows the variation of the input signal, confirming correct functionality. The results validate the accuracy and reliability of the ADC design.

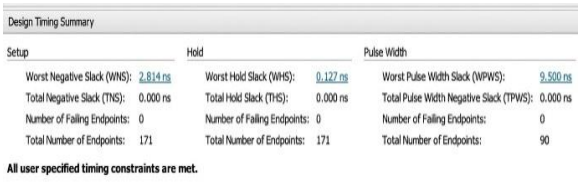
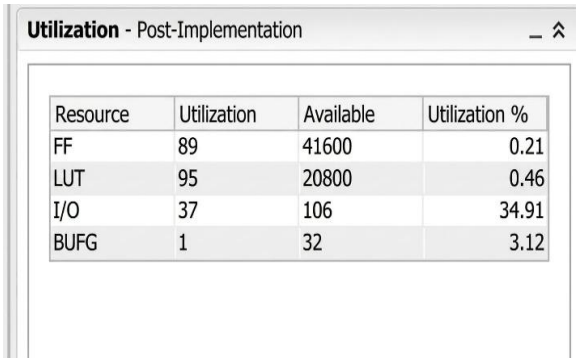


Figure 4: Timing Analysis of Proposed SAR ADC

The timing performance of the proposed ADC is analysed using the design timing summary report. The design achieves a positive Worst Negative Slack (WNS) of 2.814 ns and Total Negative Slack (TNS) of 0 ns, indicating that all timing constraints are satisfied. The hold slack is also positive, ensuring stable operation without timing violations. These results confirm that the design operates efficiently at the required speed.



Resource	Utilization	Available	Utilization %
FF	89	41600	0.21
LUT	95	20800	0.46
I/O	37	106	34.91
BUFG	1	32	3.12

Figure 5: FPGA Resource Utilization of Proposed SAR ADC

The resource utilization of the ADC design is evaluated after implementation. The design uses a minimal number of FPGA resources, including LUTs and flipflops, indicating efficient hardware usage. Thelow utilization percentage demonstrates that the design is area-efficient and suitable for implementation in resource-constrained systems.

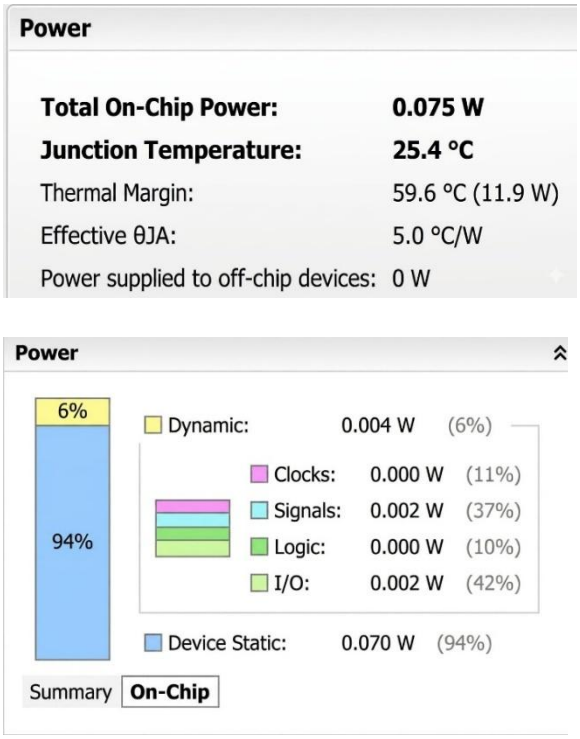


Figure 6: Power Analysis of Propose SAR ADC

The power consumption of the proposed ADC is analysed using Vivado power reports. The total on-chip power consumption is found to be 0.075 W, which is relatively low. The junction temperature is within safe limits, ensuring reliable operation. The results indicate that the design is power-efficient and suitable for low-power applications. The simulation results clearly demonstrate that the SAR ADC performs accurate Analog-to-digital conversion with stable and reliable operation. The step-by-step approximation process is evident from the waveform, confirming correct bit-wise decision making. The integration of the modified JESD204B interface further improves data handling by enabling efficient serial transmission. Overall, the results indicate that the proposed design achieves a good balance between performance, efficiency, and reduced complexity.

V. CONCLUSION

In this work, a high-speed and low-power Successive Approximation Register (SAR) ADC has been designed and analysed through simulation using RTL modelling techniques. The proposed system demonstrates accurate Analog-to-digital conversion with reduced hardware complexity and efficient operation. The step-by-step approximation process ensures reliable performance while maintaining low power consumption. The incorporation of a modified JESD204B interface enhances data transmission by enabling efficient serial communication with reduced interconnection complexity. This modification improves overall system performance and supports high-speed data handling without increasing design overhead. The simulation results validate the correctness of the design and confirm its suitability for modern applications requiring efficient data conversion and transmission. The proposed approach provides a flexible and scalable solution that can be further extended to higher resolutions and advanced system requirements.

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