Design and Simulation of an Efficient Turbo Encoder and Decoder for Error Correction in Communication Techniques

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Abstract**—**Turbo codes are widely used in modern communication systems due to their strong error correction capability, which significantly improves data reliability over noisy channels. This work focuses on the design and implementation of an efficient Turbo encoder and decoder for real-time error correction in communication systems. The encoder consists of two Recursive Systematic Convolutional (RSC) encoders combined with a pseudorandom interleaver to enhance robustness against burst errors. On the decoding side, the architecture employs Soft-Input Soft-Output (SISO) decoders with interleavers and de-interleavers, utilizing the Maximum a Posteriori (MAP) algorithm. The MAP-based approach reduces the number of decoding iterations, leading to improved decoding speed and lower computational complexity while maintaining high error correction performance. The proposed design is suitable for high-speed communication applications such as wireless networks and data transmission systems.

Index Terms**—**Turbo Codes, Error Correction, Recursive Systematic Convolutional (RSC) Encoder, Interleaver, Soft-Input Soft-Output (SISO) Decoder, Maximum a Posteriori (MAP) Algorithm, Iterative Decoding, Noisy Channel, Wireless Communication, Data Transmission Systems.

I. INTRODUCTION

The rapid evolution of modern communication systems has significantly increased the demand for efficient and reliable data transmission techniques. Internet services, satellite communications, and emerging applications such as the Internet of Things (IoT) involve the continuous transmission of massive amounts of data across various channels. During transmission, signals are subjected to several impairments including thermal noise, interference, signal attenuation, shadowing, and multipath propagation. These factors introduce errors in the received signal, which can degrade system performance, reduce data integrity, and affect the overall quality of communication.

Maintaining reliable communication under such adverse channel conditions is a fundamental challenge in Digital Communication. To overcome these challenges, error control coding techniques are employed to detect and correct errors introduced during transmission. Among these, Forward Error Correction (FEC) has gained significant importance as it allows error correction at the receiver without the need for retransmission. Conventional error correction techniques such as linear block codes and convolutional codes have been widely used, but they provide limited performance in low SNR conditions and are unable to achieve performance close to the Shannon Limit.

Turbo codes, introduced by Berrou et al., marked a revolutionary breakthrough in coding theory by demonstrating performance close to the Shannon Limit. The fundamental concept of turbo coding is based on parallel concatenation of two or more RSC encoders separated by an interleaver. The interleaver plays a crucial role by rearranging the input data sequence in a pseudo-random manner, thereby reducing the correlation between bits and improving the effectiveness of the decoding process. At the receiver, turbo decoding is performed using iterative techniques with algorithms such as MAP, Log-MAP, and Max-Log-MAP, where soft information is exchanged between SISO decoders over multiple iterations.

II. METHODOLOGY

The proposed turbo coding system is designed to improve the reliability of data transmission over noisy communication channels. It consists of three main components: turbo encoder, communication channel, and turbo decoder.

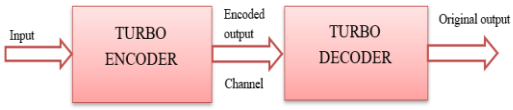

Fig. 1: Proposed Block Diagram

2.1 Turbo Encoder

The turbo encoder consists of two RSC encoders connected in parallel, with an interleaver placed

between them. The input binary sequence is directly applied to the first encoder, which produces systematic bits identical to the input and parity bits based on convolutional encoding. The same input sequence is passed through an interleaver before being fed into the second encoder, which generates another set of parity bits. The final encoded output is formed by combining the systematic bits and both sets of parity bits.

2.2 Interleaver

The interleaver rearranges the order of input bits without changing their actual values. By spreading consecutive bits across different positions, the interleaver reduces the effect of burst errors and minimizes correlation between adjacent bits. At the receiver side, a de-interleaver restores the original order of the bits, enabling proper decoding.

2.3 Communication Channel

The encoded data is transmitted through a communication channel modeled as an Additive White Gaussian Noise (AWGN) channel: r = s + n, where r is the received signal, s is the transmitted signal, and n is the noise component.

2.4 Turbo Decoder

The turbo decoder consists of two SISO decoders along with an interleaver and a de-interleaver. The decoder operates iteratively, where each decoder exchanges probabilistic information with the other. The decoding process is based on the Log-MAP algorithm. The Maximum A Posteriori (MAP) criterion $P(d_i = j \mid y)$ represents the probability of the transmitted bit given the received sequence y. The Log-Likelihood Ratio (LLR) = $\log[P(u_k = 1) / P(u_k = 0)]$: if LLR > 0 → bit = 1; if LLR < 0 → bit = 0.

III. IMPLEMENTED DESIGN

The proposed turbo coding system is implemented using Verilog Hardware Description Language (HDL) and simulated using Xilinx Vivado Design Suite.

3.1 Turbo Encoder Implementation

The turbo encoder is designed using two RSC encoders connected in parallel. The RSC encoders are implemented using shift registers and XOR logic gates. The generator polynomials are: $G_0(n) = x(n) + x(n-1) + x(n-3) + x(n-4)$ and $G_1(n) = x(n) + x(n-2) + x(n-3) + x(n-4)$. The final encoded output consists of the systematic bits and two parity streams.

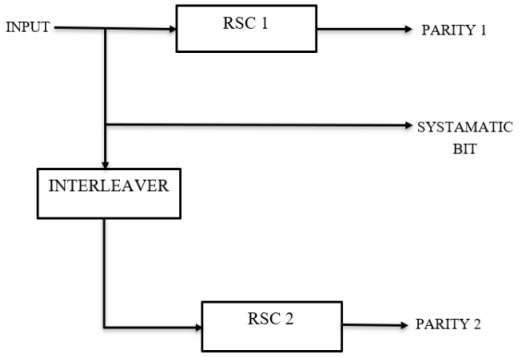

Fig. 2: Turbo Encoder Operation

3.2 Interleaver Implementation

The interleaver is implemented as a sequential logic module that rearranges the order of input bits without changing their values. A simple delay-based interleaver is used, where the input bit is stored in a register and output after one clock cycle. Both interleaver and de-interleaver operate synchronously with the clock signal to maintain proper data alignment.

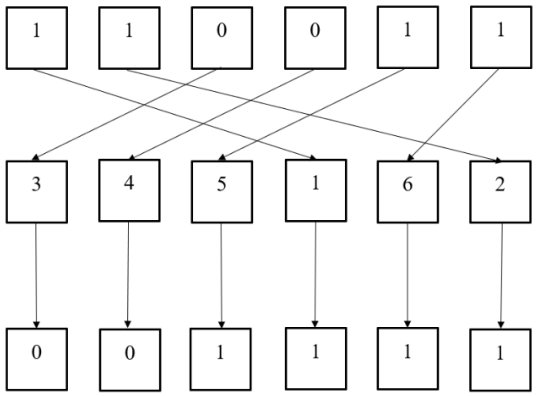

Fig. 3: Interleaver Operation

3.3 Turbo Decoder Implementation

The turbo decoder is implemented using two SISO decoders connected in an iterative structure. The first decoder processes the systematic bits and the first parity stream to generate extrinsic information. This information is interleaved and passed to the second decoder. The decoding process is iterative, meaning that the output of one decoder is fed back to the other to improve accuracy. The final decoded output is obtained after a sufficient number of iterations.

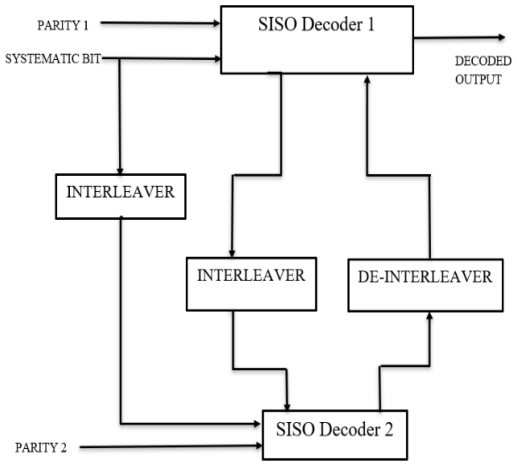

Fig. 4: Turbo Decoder Operation

IV. RESULTS & DISCUSSION

4.1 Simulation Results

The simulation is carried out using a Verilog testbench, where input binary sequences are applied to the turbo encoder. The waveform results show that the systematic output exactly follows the input sequence, confirming correct encoder operation. The parity bits generated by the two encoders are different, indicating proper functioning of the interleaver. At the decoder output, the reconstructed data closely matches the original input after a few clock cycles, demonstrating successful error correction.

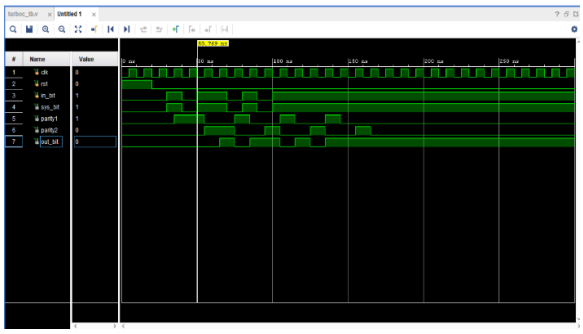

Fig. 5: Simulation Waveforms of Turbo Encoder and Decoder

4.2 RTL Analysis

The Register Transfer Level (RTL) schematic verifies the structural implementation of the turbo encoder and decoder. The encoder consists of two parallel RSC encoders and an interleaver, while the decoder includes two SISO decoders with iterative feedback. The RTL design confirms that all modules are properly connected and synchronized using clock and reset signals.

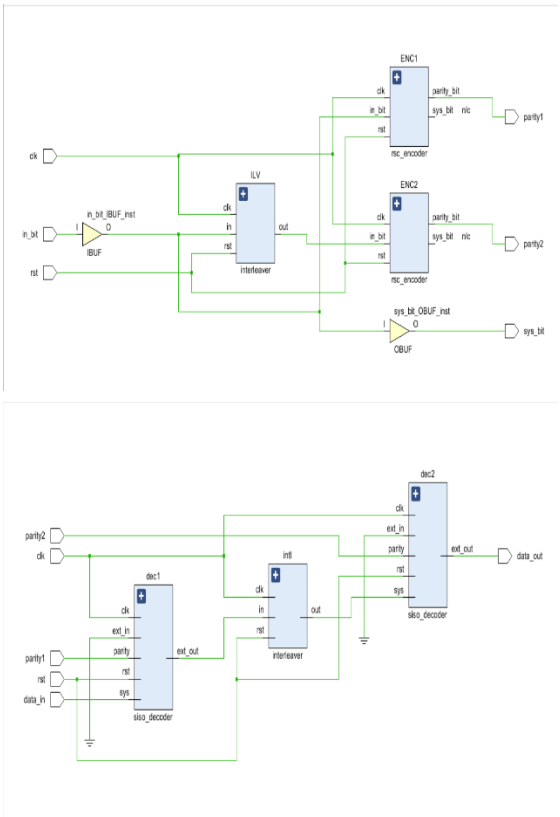

Fig. 6: RTL Schematic of Turbo Encoder and Decoder

4.3 Power Analysis

The power analysis report shows that the total on-chip power consumption of the system is approximately 0.06 W, which is very low for an FPGA-based implementation. The dynamic power consumption is minimal, indicating efficient switching activity within the design. Most of the power consumption is due to static (leakage) power, which is common in modern FPGA devices. The low power consumption makes the design suitable for energy-efficient applications such as wireless and portable systems.

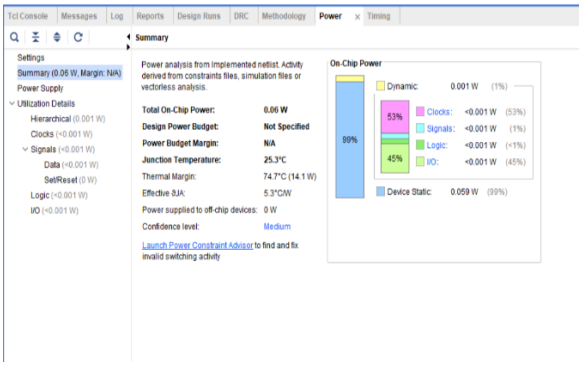

Fig. 7: Power Analysis Report

V. CONCLUSION

This paper presented the design and simulation of an efficient turbo encoder and decoder for error correction in communication systems. The proposed system uses parallel concatenated convolutional encoders along with an interleaver to improve error correction capability. At the receiver, an iterative decoding approach is employed, which significantly enhances the accuracy of recovered data. The Verilog-based implementation and simulation results confirm that the system performs correct encoding and decoding operations. The Bit Error Rate (BER) is considerably reduced due to iterative processing, and the design demonstrates low power consumption and efficient resource utilization. The system achieves performance close to the Shannon Limit, ensuring reliable data transmission.

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