Design and Simulation of CMOS Low Dropout Regulator for Low Power Applications Using Cadence

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***Abstract*—Portable biomedical instruments, IoT nodes, and mixed-signal subsystems need a supply that is both quiet and dependable, even when the available headroom is small. That requirement keeps low-dropout regulators relevant in spite of the efficiency advantage of switching converters. This work presents the design and simulation of a CMOS LDO regulator implemented in Cadence Virtuoso using the 90 nm process environment described in the source report. The regulator uses a PMOS pass device, a telescopic cascode error amplifier, a resistive feedback network, and a compensated closed loop intended for low-power operation. The circuit is evaluated through DC, AC, and transient simulations. The reported operating-point result gives an output voltage of 1.499 V, while the quiescent current is 68 μA. The measured line and load regulation are about 1.499 mV/V and 1.489 mV/mA, respectively. During load transients, the output shows roughly 18 mV undershoot and 22 mV overshoot. The summarized results also report a dropout voltage of about 300 mV, which indicates that regulation is maintained with modest headroom, although the dropout target remains the main area for improvement. The design is well suited to low-noise, low-power integrated supplies.**

***Index Terms*—CMOS LDO, low-dropout regulator, Cadence Virtuoso, low-power design, line regulation, load regulation, transient response**

I. INTRODUCTION

Power regulation is rarely the most visible block in an electronic system, but it is one of the blocks most likely to expose a weak design. Small voltage drift can corrupt sensor readings, disturb mixed-signal interfaces, and shorten battery run time. That is especially true in biomedical and IoT hardware, where the load is modest, the supply is often battery driven, and the power rail must remain clean under changing operating conditions.

Low-dropout (LDO) regulators are still a practical answer in this space because they combine circuit simplicity, low output noise, and easy integration in CMOS processes [1]– [4], [11], [12]. Unlike a conventional linear regulator, an LDO can regulate when the input voltage sits only slightly above the required output. When the voltage headroom is small, the efficiency of a linear solution improves, and the usual penalty of dissipating excess voltage becomes less severe. The report used for this manuscript focuses on exactly that operating region: a low-power integrated regulator intended for applications where noise and stability matter as much as raw efficiency.

The application context in the source report is fairly con- crete. Biomedical front ends such as ECG monitors and glu- cose sensors can lose accuracy when supply ripple is allowed to leak into the signal chain. IoT nodes face a different version of the same problem: battery energy is limited, but the rail still has to remain stable while sensors, controllers, and wireless blocks share the same supply. In both cases, the regulator is expected to be quiet, predictable, and compact rather than spectacularly efficient under all conditions.

Designing an LDO is not a one-dimensional sizing exercise. A larger pass device helps reduce dropout, but the associated gate capacitance makes loop compensation harder. Raising am- plifier gain improves DC accuracy, although it can also move the loop closer to instability. Lowering the internal bias current preserves battery energy, yet the transient response becomes slower. Those trade-offs appear repeatedly in practical LDO work [4], [10], [16], [17].

The report treats the design as a schematic-level study

rather than a full product-ready implementation. Layout and post- layout effects are left for future work, so the value of the exercise lies in the way the individual building blocks are assembled and verified in Cadence. That scope is appropriate for an academic design paper because it keeps the emphasis on circuit reasoning and measured simulation behavior.

The design reported here adopts a PMOS-pass architecture in 90 nm CMOS and implements the circuit at schematic level in Cadence Virtuoso [8]. The main contributions can be summarized as follows:

- a closed-loop CMOS LDO architecture built around a PMOS pass transistor, resistive feedback, and a telescopic cascode error amplifier;
- transistor-level design choices aimed at low quiescent current, usable phase margin, and small output variation under line and load changes; and
- simulation-based verification through DC, AC, and tran- sient analyses, including regulation metrics and dynamic response.

II. LITERATURE REVIEW

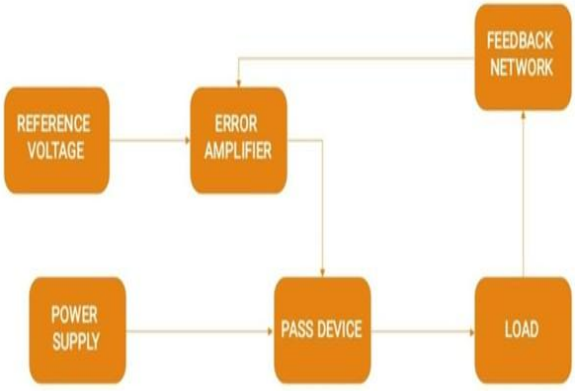
The starting point is the usual division between linear and switching regulators. Switching converters can exceed 90% efficiency, but they pay for that with switching ripple, greater implementation complexity, and the need for larger passive components. Linear regulators are easier to integrate and are generally quieter. LDOs sit in the useful middle ground for low-power systems: they retain the low-noise behavior of linear regulation while relaxing the headroom requirement [4], [9], [12], [13].

Among LDO topologies, the PMOS-pass structure remains the most common option for low-power integrated designs. Its main attraction is straightforward low-dropout operation, be- cause the pass-device gate can be driven toward the supply rail without requiring a boosted control voltage. The drawback is that PMOS devices offer lower mobility than NMOS devices, so current capability per unit area is not as strong [4], [14]. NMOS-pass LDOs improve on-resistance and area efficiency, but they usually need a charge pump or another gate-boosting method to sustain low-dropout operation, which adds noise and overhead [3], [15].

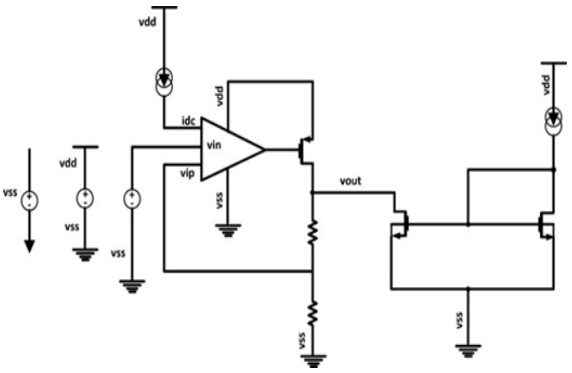
The report also discusses flipped-voltage-follower (FVF) and capacitor-free LDOs. FVF-based structures are attractive when very low quiescent current is the priority. Capacitor- free regulators, on the other hand, address the integration problem created by large off-chip output capacitors. Their weakness is that internal compensation becomes more delicate, and stability depends heavily on pole-zero placement [5], [6], [18], [19].

The report also frames the literature in terms of the main performance parameters. Dropout voltage determines how much battery energy can still be used before regulation is lost. Line and load regulation show whether the feedback loop has enough DC authority to hold the output steady as the environment changes. Transient response and phase margin expose the quality of the compensation strategy, while quiescent current tells us how much energy is consumed simply to keep the regulator alive. In other words, a good LDO is not just a low-dropout circuit. It is a circuit that balances accuracy, speed, stability, and internal power overhead.

The prior-art summary in the report places the present work alongside established CMOS LDO designs. Rincon- Mora reported a 1.2 V regulator in 0.5 μm CMOS with 23 μA quiescent current and 200 mV dropout, while Leung and Mok presented a capacitor-free LDO in 0.35 μm CMOS with 1.5 V output, 35 μA quiescent current, and 250 mV dropout [4], [5], [16]. Ho and Leung emphasized low-voltage and low- quiescent-current operation, and Hazucha *et al.* demonstrated strong PSRR in a 90 nm design [6], [7], [20]. These references set a clear direction: low dropout, small quiescent current, and stable loop behavior remain the core metrics, but each



(a) Block-level architecture of the proposed LDO.



(b) Cadence schematic of the proposed regulator.

Fig. 1. Architecture views of the proposed CMOS LDO regulator.

III. METHODOLOGY AND PROPOSED DESIGN

A. Architecture

The regulator follows the standard four-block LDO struc- ture: a voltage reference, an error amplifier, a PMOS pass transistor, and a feedback divider. The divider senses the output voltage and returns a scaled version of it to the amplifier. The amplifier then adjusts the PMOS gate voltage so that the feedback node tracks the reference. If the output drops under increased load demand, the gate is pulled lower and the PMOS device conducts more strongly. If the output rises, the gate is pushed upward and the pass current is reduced.

This operating sequence is simple, but it explains most of the observed behavior in simulation. Under a line disturbance, the error amplifier senses the feedback shift and corrects the PMOS gate before the output can move too far. Under a load transient, the output capacitor provides the first line of support and the amplifier restores the steady state afterward. The relative speed of those two actions largely determines the size of the overshoot, undershoot, and settling period.

Using generic divider notation, the regulated output is set by

$$V_{OUT} = V_{REF} \left(1 + \frac{R_T}{R_B}\right), \qquad (1)$$

where R_T and R_B are the top and bottom feedback resistors, respectively. The source report assigns high-value resistors of 300 kΩ and 1.2 MΩ so that divider loss stays in the mi- croampere range. The block-level architecture and the Cadence schematic used for simulation are shown in Fig. 1.

B. Error Amplifier and Feedback Network

The error amplifier is implemented as a telescopic cascode OTA. That choice is reasonable for an LDO intended for low-power operation because it offers high gain and useful bandwidth without excessive bias current. The design targets reported for the amplifier include a 10 V/μs slew rate and a 10 MHz gain-bandwidth product, which are appropriate for a low-power regulator that still needs a reasonably fast control loop.

The schematic also shows an NMOS active-load current mirror at the output side. In this design, the two NMOS transistors M_1 and M_2 use the same dimensions, each with W/L = 1.05 μm/1 μm. Because the two devices are matched, the branch behaves as a current mirror and is naturally described as an active load. The associated bias current in the shown schematic is 10 mA, which sets the operating current for that mirror branch during simulation.

The report later lists preliminary OTA sizing ratios around W/L = 26 for the input pair, 13 for the cascode devices, and 20 for the mirror devices. In the final schematic, the PMOS pass device is much larger than the NMOS mirror pair, which is consistent with the intended split between current delivery and small-signal control.

C. Pass Device Choice and Dropout Considerations

The PMOS pass transistor is the dominant power device in the regulator. Near dropout, its channel behaves like a control- lable resistance, so the dropout voltage can be approximated by

$$V_{DO} \approx I_{LOAD,\max} R_{ON}, \qquad (2)$$

with

$$R_{ON} \approx \frac{1}{\mu_p C_{ox}(W/L)(V_{SG} - |V_{TP}|)}. \qquad (3)$$

The report uses a PMOS pass device of 1.05 μm/280 nm. A wider device lowers R_{ON} and helps the dropout target, but the larger gate capacitance also introduces a low-frequency pole at the gate node. That trade-off is central to LDO design: reducing dropout too aggressively can make the control loop sluggish or unstable if the amplifier is not compensated properly.

D. Stability Strategy

The output capacitor of 1 μF is the main stabilizing element in the reported design. The stability discussion in the source text identifies the dominant pole at the output node and a non- dominant pole at the pass-transistor gate. Using the values reported for the compensated design,

$$f_{p1} = \frac{1}{2\pi r_{ds,p} C_{OUT}} \approx 320 \text{ Hz}, \quad (4)$$

and

$$f_{p2} = \frac{1}{2\pi R_{oa} C_{gs,p}} \approx 400 \text{ kHz}. \quad (5)$$

The report notes that an uncompensated loop would leave too little phase margin at unity-gain crossing, so Miller compensation is introduced to move the pole locations apart and

TABLE I DESIGN SPECIFICATIONS USED FOR THE REPORTED LDO

Parameter	Reported value
Technology	90 nm CMOS
Input voltage range	1.8–3.3 V
Target output voltage	1.5 V
Dropout target	< 300 mV
Load current range	1–100 mA sweep; 10 mA nominal DC point
Quiescent current target	< 100 μA
Load regulation target	< 1.5 mV/mA
Line regulation target	< 1.5 mV/V
Phase margin target	> 60°
Error amplifier target	10 MHz GBW, 10 V/μs slew rate
Pass device size	1.05 μm/280 nm PMOS
NMOS current-mirror size	1.05 μm/1 μm ($M_1 = M_2$)
Current-mirror bias current	10 mA

recover a phase margin above 60°. From a design standpoint, that is the right decision. The regulator is meant for stable low- power operation, not for pushing the bandwidth to its absolute limit.

E. Design Trade-Offs

One of the more useful aspects of the source report is that the design choices are tied to clear engineering compromises rather than presented as isolated facts. The PMOS pass device is selected to simplify low-dropout operation, the telescopic cascode amplifier is selected to keep gain high with modest bias, and the external output capacitor is retained to keep loop stabilization manageable. Even the use of large feedback resistors reflects the same style of thinking: divider loss is reduced, but the feedback node becomes more sensitive to parasitic effects.

IV. DESIGN SPECIFICATIONS

Table I consolidates the design targets and implementation details repeated through the source report. The values are suf- ficient for a low-power CMOS LDO intended for biomedical, IoT, and mixed-signal support rails.

V. SIMULATION SETUP

The circuit is implemented at schematic level in Cadence Virtuoso and simulated with the Cadence environment de- scribed in the report [8]. No layout extraction is included, so the study remains a pre-layout verification exercise. That keeps the focus on architecture, device sizing, and loop behavior.

The testbench uses an input source swept across the reported operating range of 1.8–3.3 V. The output node is connected to a 1 μF capacitor, and the load is represented by a current source so that the regulator response can be checked under changing load demand. The report describes a load sweep from 1 mA to 100 mA, while the nominal DC operating-point result is taken at 10 mA and $V_{IN} = 2.5$ V. That is a reasonable way to separate static bias verification from broader performance sweeps.

The simulation flow follows a bottom-up verification style. The error amplifier is checked first through AC analysis so that gain, gain-bandwidth, and phase margin can be confirmed

before the full regulator is closed around the pass device. After that, the complete LDO is evaluated with DC sweeps to confirm operating regions and regulation behavior. Only then is transient analysis used to stress the loop with sudden load changes. That order matters, because it keeps a local amplifier issue from being mistaken for a system-level compensation problem.

Three analyses are used.

- DC analysis: verifies the operating point, nominal output voltage, and behavior across the input range.
- AC analysis: evaluates the standalone error amplifier frequency response and checks whether the compensated loop can maintain a usable phase margin.
- Transient analysis: applies load changes and records overshoot, undershoot, and settling behavior.

This sequence is practical. It avoids treating the LDO as a black box and instead checks the amplifier first, then the closed-loop regulator.

Another useful detail in the report is the separation between specification-driven targets and measured behavior. The design stage aims for low dropout, low quiescent current, and a phase margin above 60°. The simulation stage then shows which of those targets are met directly and which ones remain slightly off. That makes the discussion more honest and more useful than simply listing ideal specifications.

VI. RESULTS AND DISCUSSION

A. Error Amplifier Performance

The reported AC simulation of the error amplifier shows DC gain greater than 60 dB, gain-bandwidth around 30 MHz, and phase margin above 60°. Those numbers are more than adequate for a low-power LDO in which the dominant pole is intentionally placed at the output node. The result suggests that the amplifier is not the limiting block in regulation accuracy; rather, the full-loop behavior depends on how the pass device and output capacitor shape the poles. The simulated AC response is shown in Fig. 2.

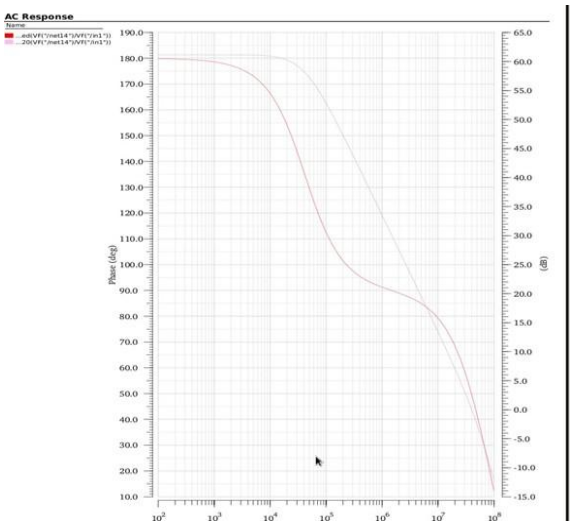


Fig. 2. AC response of the designed error amplifier used in the LDO loop.

B. DC Regulation and Static Behavior

At the nominal operating point, the source report gives an output voltage of 1.499 V and confirms that the pass transistor remains in saturation. The quiescent current is 68 μA, which stays below the stated 100 μA target. From a low-power standpoint, that is a good result. It means the internal control circuitry does not consume a disproportionate share of the available current.

The line and load regulation figures are both close to 1.5 in their respective units, which indicates that the closed loop is doing its job. Output deviation under input sweep is small outside the dropout region, and the regulator holds the target voltage with little static error. For the intended applications, that is more important than achieving an especially aggressive bandwidth number.

The DC result also says something about the chosen PMOS device. Because the pass transistor remains in saturation at the nominal point, the loop still has gain available for regulation. If the device were already drifting too far toward triode operation in nominal conditions, the regulator would become much more sensitive to further load increase and input reduction. The operating-point result therefore supports the basic device- sizing decision even though the final dropout number is not yet ideal.

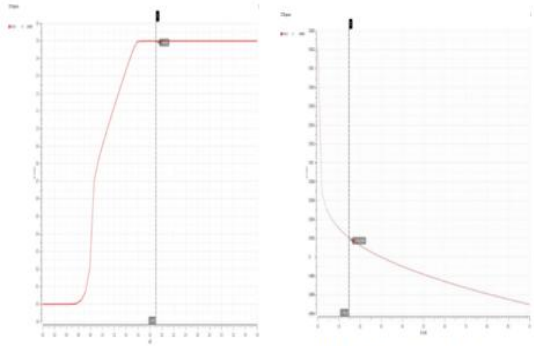
C. Dropout, Line Regulation, and Load Regulation

The source report is strongest when it compares related metrics instead of treating them separately. The measured line regulation of about 1.499 mV/V suggests that changes at the input are only weakly transferred to the output. The measured load regulation of about 1.489 mV/mA shows a similar level of control over load-induced disturbances. Together, these numbers indicate that the error amplifier provides adequate loop gain over the low-frequency range that matters most for DC regulation.

Dropout is a more demanding metric because it depends not only on loop accuracy but also on pass-device headroom. The summarized result of about 300 mV is acceptable for proof-of- concept operation, yet it falls short of the tighter design goal stated earlier in the report. In practical terms, that mismatch is not surprising. Once low quiescent current, wide load range, and comfortable phase margin are all imposed at the same time, the pass device often ends up being the block that sets the last real limit. Representative static-response plots are shown in Fig. 3.

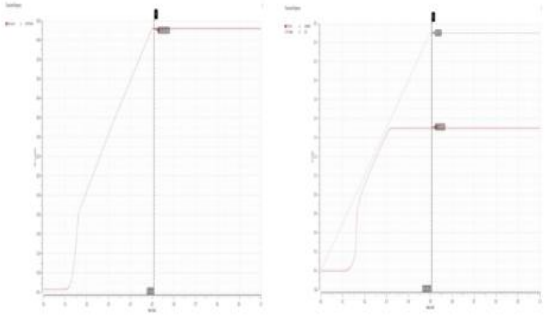
D. Transient Response

Transient simulation reports an undershoot of about 18 mV and an overshoot of about 22 mV during load changes. Those excursions are modest for a low-power LDO using an external output capacitor, and they suggest that the amplifier and pass device recover quickly after a step in demand. The report does not provide a numeric settling-time value, but it explicitly describes the settling as fast. Given the small excursion levels, that assessment is reasonable.



(a) Line Regulation. (b) Load-regulation curve.

Fig. 3. Static response of the proposed LDO from Cadence simulation.



(a) Power Consumption. (b) Transient Response.

Fig. 4. Dynamic response of the proposed LDO from transient simulation.

From a control perspective, the transient result is consis- tent with the compensation discussion. The output capacitor absorbs the immediate current mismatch, while the amplifier brings the gate of the PMOS device to a new operating point. If the loop were under-compensated, one would expect ringing or repeated overshoot cycles. If it were excessively slow, the first voltage dip would be much larger. The reported waveform behavior sits between those extremes, which is usually where a practical LDO should operate. Figure 4 summarizes two transient views captured during simulation.

E. Power Implication

The report's summary table lists a power figure of 35 μW. Even without a detailed breakdown, that number supports the broader conclusion that the control circuitry overhead is kept small. At the same time, the report correctly notes that total LDO dissipation increases with both load current and voltage drop across the pass device. This is the familiar limitation of linear regulation: the circuit can be very clean electrically, but it never escapes the physics of burning excess voltage as heat.

F. Suitability for Target Applications

The reported performance lines up well with the applica- tions emphasized in the source document. A regulator intended for biomedical sensing or low-power IoT support rails does not need to deliver the highest possible efficiency at large voltage conversion ratios. It needs to keep the output quiet,

TABLE II SUMMARY OF REPORTED SIMULATION RESULTS

Metric	Reported result	Comment
Error amplifier DC gain	> 60 dB	Sufficient for regulation
Error amplifier GBW	≈ 30 MHz	Comfortable small-signal bandwidth
Error amplifier phase margin	> 60°	Stable amplifier operation
Output voltage	1.499 V	Very close to 1.5 V target
Quiescent current	68 μA	Below target limit
Dropout voltage	≈ 300 mV	Highest remaining weakness
Load regulation	≈ 1.49 mV/mA	Near target
Line regulation	≈ 1.499 mV/V	Near target
Transient undershoot	≈ 18 mV	Small deviation
Transient overshoot	≈ 22 mV	Small deviation
Reported power	35 μW	From summary table in report

tolerate moderate disturbances, and consume little current internally. The low quiescent current, small static output error, and restrained transient excursions reported here all point in that direction. The only caution is the dropout value, which becomes more important as the supply approaches the regulated output. For systems with a little extra headroom, the design is already practical. For

systems running very near the edge of battery discharge, one more optimization pass would be worthwhile.

G. Summary of Reported Metrics

H. Discussion

The most convincing part of the design is not a single number but the overall balance of the results. The regulator reaches the intended 1.5 V output, keeps the quiescent current low, and shows controlled transient behavior. These are the qualities expected from a PMOS-based LDO intended for sensitive low-power loads.

At the same time, the dropout result deserves a more careful reading. The early design target is stated as less than 200 mV, but the final summary table reports about 300 mV. That does not invalidate the design; it simply shows where the next iteration should focus. In practical terms, the pass device sizing, gate-drive swing, or compensation strategy would need another round of optimization if tighter headroom is required. The line and load regulation figures are close to the stated targets, which implies that the feedback loop has enough DC authority. The transient response also points in the same direction: the regulator is stable and responsive without being over-tuned. For an educational yet technically meaningful schematic-level design, that is a solid outcome.

VII. CONCLUSION

The reported work demonstrates a CMOS LDO regulator designed and simulated in Cadence for low-power applications that need a quiet and stable supply. The chosen architecture combines a PMOS pass element, a telescopic cascode error amplifier, resistive feedback, and an external output capacitor. Based on the simulation data provided in the source report, the regulator delivers 1.499 V output, draws 68 μA quiescent current, and maintains line and load regulation near 1.5 mV/V and 1.489 mV/mA. The transient response remains controlled, with limited undershoot and overshoot during load changes.

The design matters because it shows a workable balance between regulation quality, power overhead, and circuit sim- plicity in a CMOS implementation. The reported dropout value of about 300 mV leaves some room for improvement, but the overall behavior is already suitable for low-power mixed-signal, biomedical, and IoT-oriented supply rails.

VIII. FUTURE WORK

The next practical step is layout implementation followed by post-layout simulation, since parasitic capacitances and routing resistance will affect both regulation and stability. A second useful extension is corner analysis across process and temperature, which would show how robust the present design remains outside nominal conditions. The report also points to capacitor-free operation as a natural future direction for better integration. Beyond that, reducing quiescent current further and combining the LDO with other on-chip power- management blocks would make the design more relevant to complete SoC power delivery.

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