Design and Systematic Comparative Analysis of Different Op-Amp Topologies (Using Gpdk180nm)

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***Abstract*—The current work performs a comparative study of four CMOS operational amplifier structures: single-stage, telescopic cascode, folded cascode, and Miller compensated by employing Cadence Virtuoso simulation software while maintaining identical biasing in order to provide a fair comparison of each structure. Parameters like DC gain, unity gain bandwidth (UGB), phase margin, slew rate, power dissipation, common mode rejection ratio (CMRR), and power supply rejection ratio (PSRR) are analyzed. It reveals the strengths and weaknesses of each structure with respect to gain, bandwidth, stability, and power consumption.**

***Index Terms*—Single stage, Telescopic cascode, Folded cascode, Miller compensated, DC gain, UGB, Slew rate, PSRR, GPDK 180nm technology.**

I. INTRODUCTION

Operational amplifiers are fundamental building blocks in analog and mixed-signal circuit design, widely used in applications such as signal conditioning, data converters, and communication systems, The performance of an operational amplifier is strongly influenced by its topology, which determines key parameters such as gain, bandwidth, power consumption, and stability.

With the scaling of CMOS technologies, there is an increasing demand for low-power and high-performance analog circuits. Different op-amp architectures, including single-stage, telescopic cascode, folded cascode, and two-stage amplifiers, offer unique trade-offs between these performance metrics.

This paper presents a comparative analysis of these four op-amp topologies implemented using gpdk180nm CMOS technology in Cadence virtuoso. All circuits are designed under identical biasing conditions to ensure a fair comparison. The objective is to evaluate and analyze the trade-offs in gain, bandwidth , stability, and power consumption, and to identify topologies for specific analog design requirements.

II. LITERATURE SERVEY

Designing operational amplifiers has attracted many researchers' attention in the area of analog circuits, particularly with regard to improving gain, bandwidth, and power performances with technology scaling. Traditional one-stage amplifiers have gained popularity for their simplicity in design and lower power consumption, although they possess challenges with regards to obtaining high gains and output drive capacity.

The architecture of Cascode has been thoroughly investigated due to its potential to realize a high-gain amplifier circuit by increasing the value of output resistance. Telescopic circuits are fast and low-power consumption structures; however, they have lower output swing and very stringent voltage headroom considerations. On the other hand, Folded Cascode circuits offer better input common mode range and output swing capabilities.

Two-stage operational amplifiers are normally employed where there is a need for higher gains and larger swings on the output signal. In this regard, a second gain stage is incorporated in such cases, although this may lead to instability issues and hence Miller Compensation..

Recent research focuses on the compromise among gain, bandwidth, stability, and power dissipation, pointing out that none of the topologies can be considered best for all situations. It necessitates a comparative study to be conducted in similar conditions.

III. METHODOLOGY

This paper discusses four CMOS operational amplifier designs: single stage, telescopic cascode, folded cascode, and two-stage Miller-compensated amplifiers. The designs were simulated in the Cadence Virtuoso platform using 180 nm CMOS technology.

In order to ensure a comparison that is accurate and valid for all the circuits involved, the biasing is carried out under the same operational conditions. The voltage supply is set at 1.8 V, while the capacitance loading is set at 1 pF. The tail current is set at 112 μA, with the branch currents being 56 μA each. The tail current transistor has an aspect ratio (W/L) of 12 μm/360 nm, while the differential transistors have a ratio of 3 μm/180 nm.

0.8 volts of input voltage is provided to the differential pair, while a 0.6 volt bias voltage is applied to the tail NMOS transistor for obtaining a constant current under any circumstances and keeping all the transistors in the saturation region.

For each topology we have made the Circuit by making the body effect zero by just connecting the body and source of every transistor so that the Vbs is always 0.

Each topology is to extract key performance parameters, including DC gain, gain bandwidth product, phase margin, slew rate, power consumption, CMRR, PSRR, and output swing. The results are then compared to evaluate the performance trade-offs among different architectures.

A. Technology and tools

All designs are implemented using gpdk180nm CMOS technology in the Cadence virtuoso environment

B. Common Design Parameters

To ensure a fair comparison, the following paraments are kept constant:

- Supply Voltage (Vdc): 1.8V
- Load Capacitance (CL): 1pF
- Tail Current (Ibiase): 112uA
- Branch Current (Ib1,Ib2): 56uA
- Tail Transistor (W/L): 12um/360nm
- Differential Pair (W/L): 3um/180nm
- Input Common Mode Voltage (V-,V+) :800mV
- Biase Voltage for tail current (Vbiase):600mV

C. Implemented Topologies

1. Single-Stage Op-Amp

Simple structure with low power consumption but limited gain.

2. Telescopic Cascode Op-Amp

High gain and bandwidth due to cascoding, but limited output swing.

3. Folded Cascode Op-Amp

Improved input range and output swing compared to telescopic design.

4. Two-Stage Miller Compensated Op-amp

High Gain and large output swing with compensation for stability.

The following parameters are evaluated:

DC Gain (Av)

The DC gain of an operational amplifier represents its ability to amplify low-frequency signals. A higher DC gain indicates better amplification.(Ac analysis then plotted in 20db scale and take the max valve)

Gain Bandwidth Product (GBW)

The Gain Bandwidth Product (GBW) defines the frequency at which the amplifier gain becomes unit. It indicates the speed of the amplifier and determines how well the op-amp can operate at high frequencies.(Find the 0db point in gain graph and it is equal to UGBW)

Phase Margin (PM)

Phase margin is a measure of the stability of the amplifier in feedback configurations. A higher phase margin ensure stable operation with minimal oscillations and overshoot.(Select the same graph and choose phase and now find the 0db frequency and see the phase valve then if the phase is negative then add 180 if positive keep as it is.)

Slew Rate (SR)
Slew rate is the maximum rate of change of the output voltage with respect to time.it determines the speed of the amplifier and it is critical for high-speed applications. (Go for transient analysis select the output then click on calculator and find slew rate and set valves and run it)

Power Consumption (PC)
Power consumption represents the total power drawn by the amplifier from the supply, it is an important metric for low-power and battery-operated applications. (multiply the vdc and current flowing through the biasing transistor)

Common Mode Rejection Ratio (CMRR)
CMRR measures the ability of the amplifier to reject common-mode signals present at both inputs. A higher CMRR indicates better noise immunity and improved differential signal amplification. (Find ACdb then use CMRR =Addb-Acdb formula)

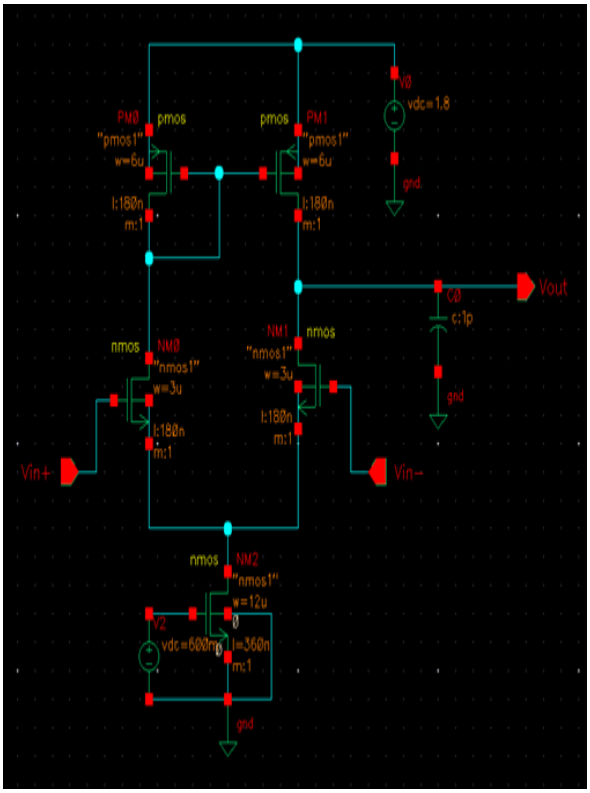
Power Supply Rejection Ration (PSRR)
PSRR indicates how well the amplifier rejects variations in the supply voltage. A higher PSRR ensures stable operation even in the presence of power supply noise. (Add a small ac signal in the vdc and find the gain same as 'A')

Output Swing (OS)
Output swing defines the maximum rage of the output voltage that the amplifier can achieve without distortion. It is limited by the supply voltage and transistor stacking in the circuit. (sweep the input from 0 to 1.8V and see the max and min output voltage and check the output voltage for half input 900mV)

IV. RESULTS

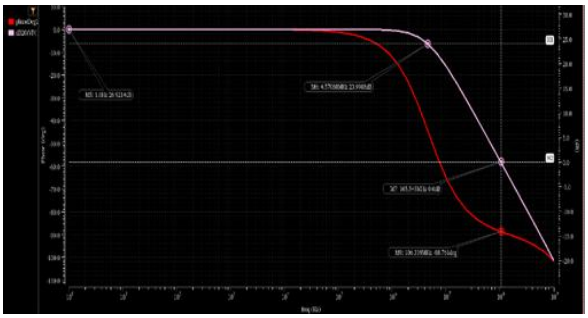
4.1 Single-Stage Op-Amp
It is the simplest form of CMOS amplifier topology, implemented using a differential pair with active load. Its primary advantage lies in its low-power applications. However, the achievable DC gain is limited due to the relatively low output resistance compared to cascode-based design. Despite these limitations, the single-stage amplifier offers better stability and does not require frequency compensation, resulting in a wider bandwidth compared to multi-stage architecture, therefore, it is well-suited for applications where moderate gain, high speed, and low power consumption are preferred over high precision.

In this Paper, the single-stage amplifier exhibits the lowest gain among all topologies while relatively low power consumption and higher bandwidth.



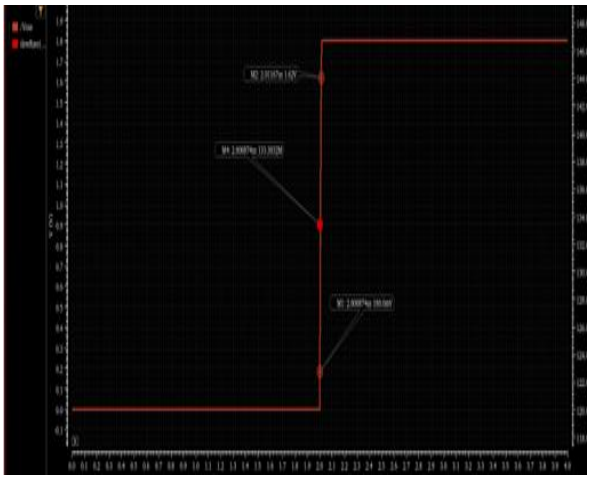
4.1.1 Circuit of Single-Stage Op-amp

Above is the Circuit of Single-Stage amplifier which is made with the help of two identical NMOS(NM0,NM1) where we provide the input and they convert voltage difference to current, then above we have 2 PMOS as Current mirror load PM0 is diode connected and sets the mirror then PM1 mirrors that current and creates high impedance at output, they convert differential current to single ended output voltage and then at the bottom, we have NM2 which sets the bias current forces the NM0 and NM1 to always flow constant current of (56uA in each branch total 112 uA flowing through its Drain to source to ground), And acts as constant current source,
At the load we have 1pf Capacitor C0.



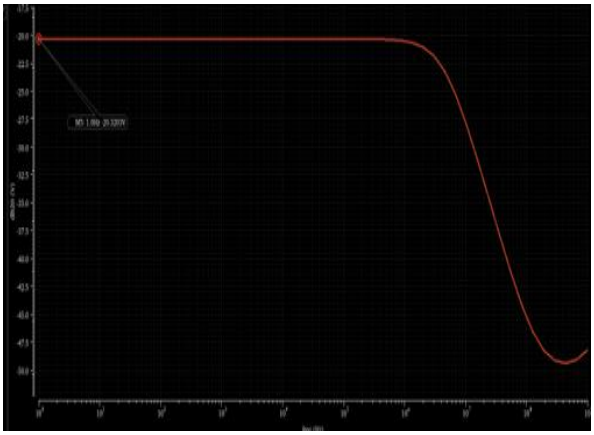
4.1.2 Gain and Phase Margin

Here we can see the Differential gain, Bandwidth, UGBW, Phase and we got Gain of 26.921db and BW of 4.65Mhz then UGBW is 105.545Mhz and for that we got -88.65deg margin and this value we got for 1v AC.



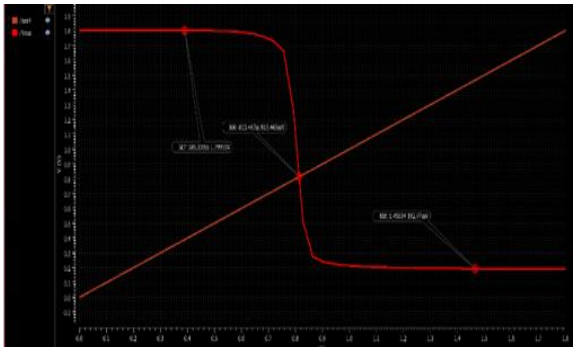
4.1.3 Slew Rate

We got a slew rate of 133.38V/uSec which means the amplifier can change 133.38V in a microsecond and we got this for a pulse input of period of 4uS, Pulse width of 2uS, trise=tfall=1nS.



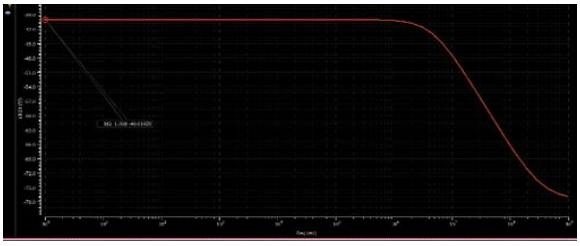
4.1.4 Common Mode Gain

Here we found -20.32db for the common gain mode which we got by giving the 1V Ac input to both the inputs



4.1.5 Output Swing

We got the Output swing of 1.6V (VH=1.79V, VL=192.97mV) taken by giving the input as variable then sweeping it from 0 to 1.8V

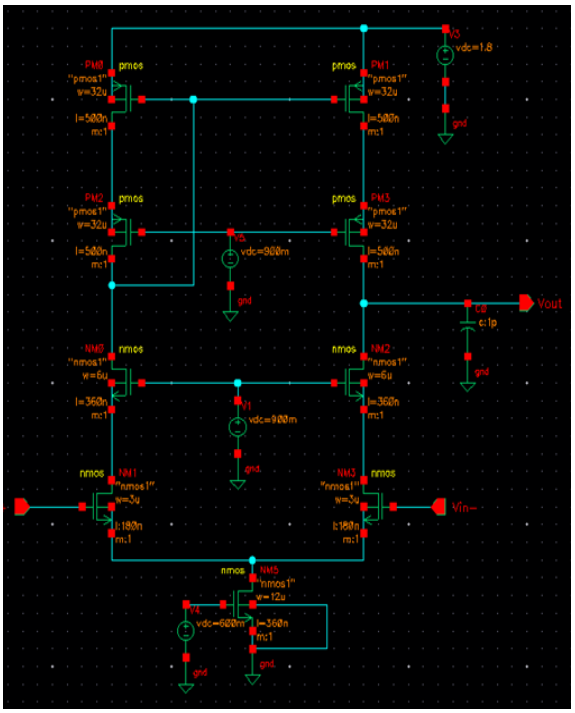


4.1.6 Power Supply Rejection Ratio

Above is the graph of PSRR and we got -40.01db for it, for this we gave normal dc voltage to the inputs, so they are in saturation region and then adding 10mV ac single of 1khz to the power supply.

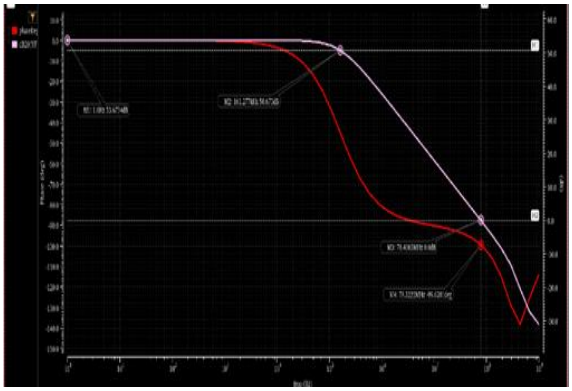
4.2 Telescopic Cascode Op-amp

The telescopic amplifier employs cascading techniques to significantly increase output resistance, thereby achieving higher DC gain. Additionally, it offers lower power consumption compared to multi-stage architecture, as it operates with a single current branch. However, the major limitation of the telescopic cascode amplifier with a single current branch. However, the major limitation of the telescopic cascode amplifier is its restricted output voltage swing, caused by the stacking of multiple transistors, which imposes strict application. Despite these constraints, the telescopic topology is highly efficient for high-speed and moderate-swing applications where high gain and bandwidth are critical In this we got, the telescopic cascode amplifier demonstrated higher gain.



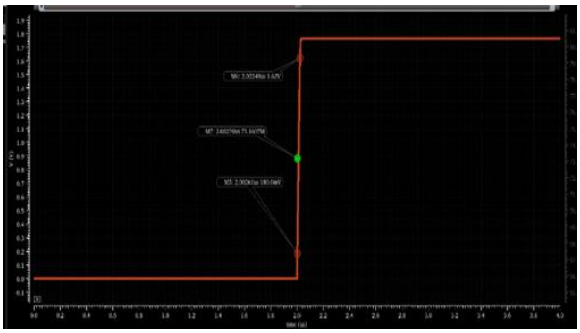
4.2.1 Circuit of Telescopic Cascode Op-amp

In Telescopic transistors are stacked to increase the impedance increasing the overall gain, Input pair and tail NMOS are same as Single Stage, the NMOS pair above differential pair is used to increase the output resistance by shielding the input transistor from voltage changes at the output known as gain boosters as is done by PMOS pair connected bellow PMOS load transistor, Top section PMOS work same as Single Stage PMOS do.



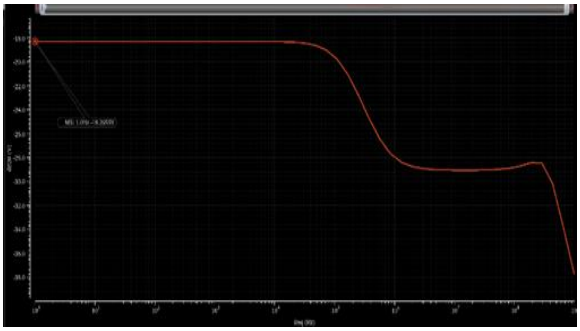
4.2.2 Gain and Phase Margin

We got Gain of 53.67db and BW of 161.277Khz then UGBW is 78.4Mhz and for that we got -99.62deg margin



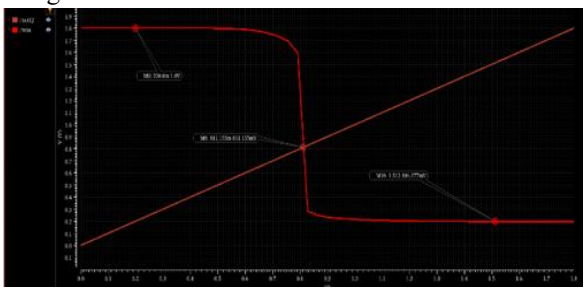
4.2.3 Slew Rate

We got a slew rate of 73.16V/uSec



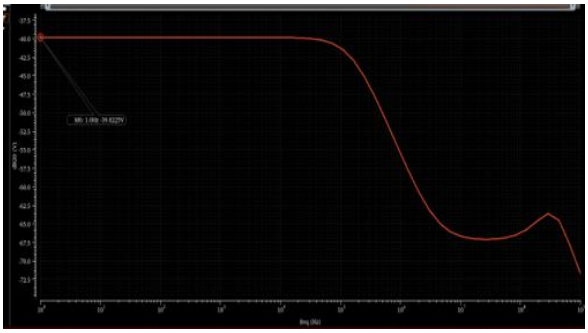
4.2.4 Common Mode Gain

We got -18.29db in the simulation



4.2.5 Output Swing

Above is the graph showing the Output swing of 1.61V (VH=1.8V, VL=196.377mV) same method used



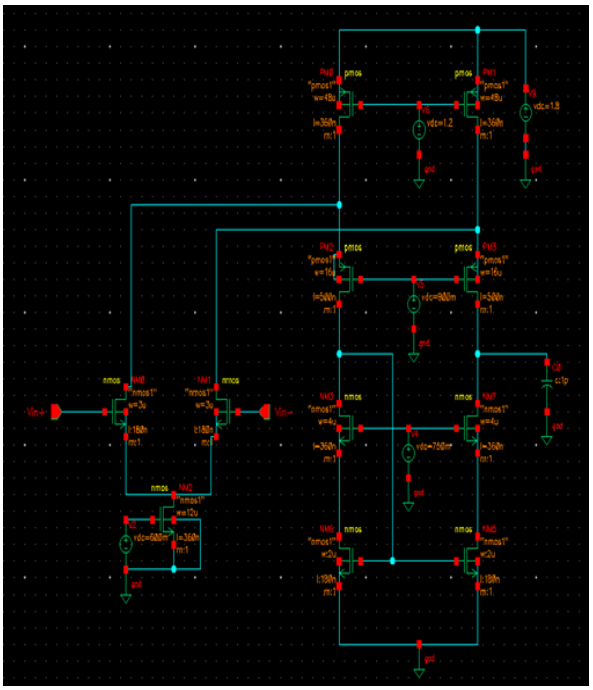
4.2.6 PSRR

From graph of PSRR we got -39.82db

4.3 Folded Cascode Op-Amp

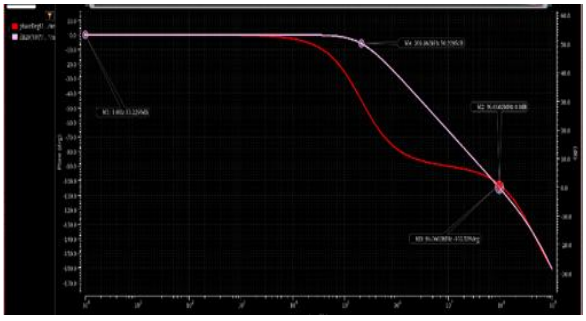
The folded cascode OPAMP is designed to overcome the voltage headroom limitations of the telescopic cascode topology while maintaining high gain. By Folding the signal path it allows the use of both NMOS and PMOS transistors, but by adding more current branch the power consumption increases to

Its same as Telescopic but the voltage swing is increased



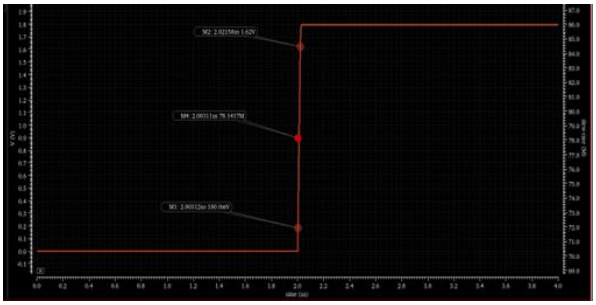
4.3.1 Circuit of Folded Cascode Op-amp

The folded part of the circuit is working same as the Telescopic Differential and tail current and top PMOS are working as active load and current source, the middle section PMOS and NMOS section are used to increase the output impedance, which is crucial for high gain bottom NMOS are used for constant current source



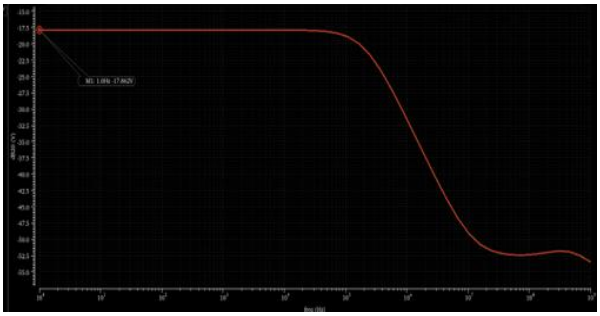
4.3.2 Gain and Phase Margin

We got Gain of 53.22db and BW of 209.96Khz then UGBW is 96.06Mhz and for that we got -102.5deg margin



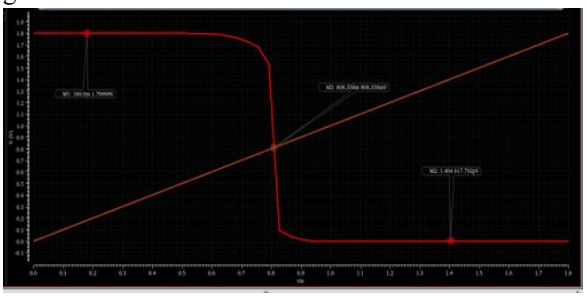
4.3.3 Slew Rate

We got a slew rate of 78.14V/uSec



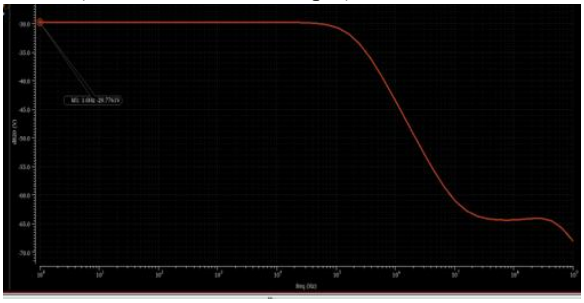
4.3.4 Common Mode Gain

We got -17.86db in the simulation for the common gain mode



4.3.5 Output Swing

Above is the graph showing the Output swing of 1.79V (VH1.79V, VL=617.7pV)



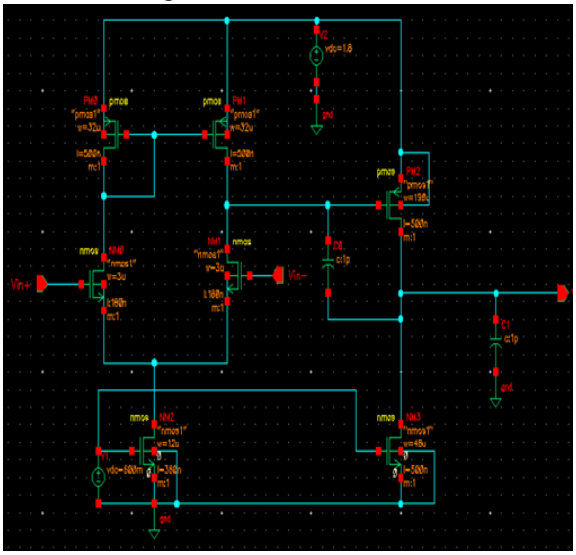
4.3.6 PSRR

From graph of PSRR we got -29.77db

4.4 Two-Stage Miller Compensated Op-amp

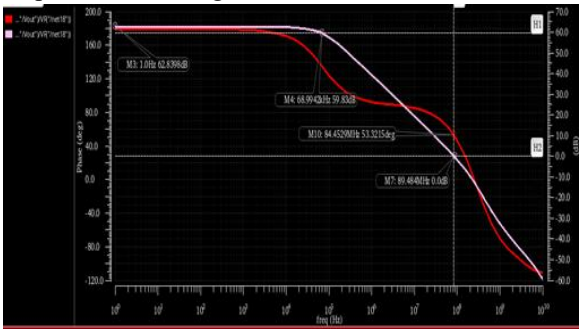
The Two-Stage operational amplifier uses cascaded gain stages to achieve high DC gain and large output swing. However, the presence of multiple stages introduces stability issues, which are addressed using miller compensation. This improves stability but reduces bandwidth, making the design suitable for high-gain applications where speed is not the primary concern.

The two-stage amplifier achieved the highest gain due to cascaded stages.



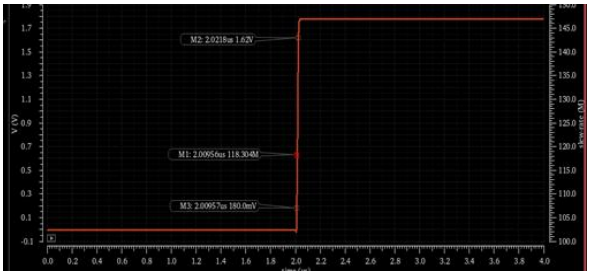
4.4.1Circuit of Two-stage Miller Compensated Op-amp

Here we have two stages 1 differential amplifier, 2 Common Source Amplifier 1 stage is working as 1 topology, in 2 stage we have is used for providing the extra gain and it increases the output swing to then capacitor used in between the stages is to prevent the amplifier from being unstable and start oscillation



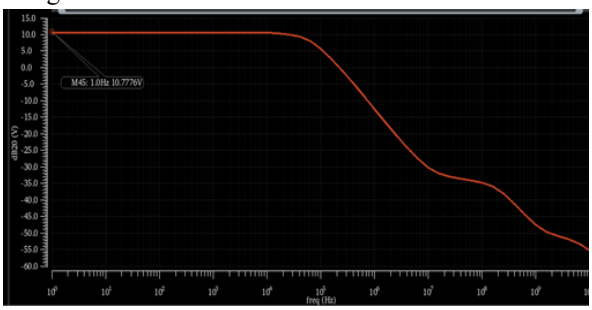
4.4.2 Gain and Phase Margin

The Gain of the circuit is 62.83db and BW of 68.99Khz then UGBW is 89.48Mhz and for that we got 53.32deg margin



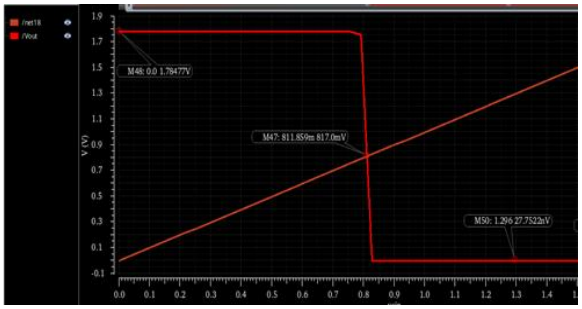
4.4.3 Slew Rate

We got a slew rate of 118.3V/uSec



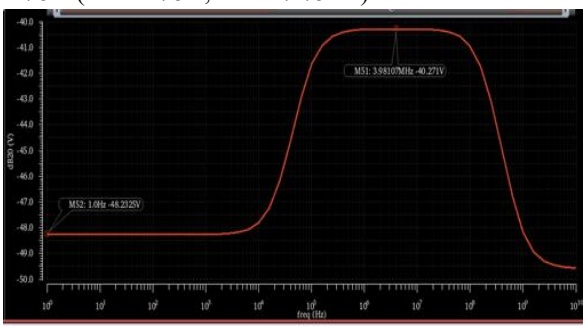
4.4.4 Common Mode Gain

We got 10.77db in the simulation for the common gain mode



4.4.5 Output Swing

Above is the graph showing the Output swing of 1.78V (VH=1.78V, VL=27.75nV)



4.4.6 PSRR

From graph of PSRR we got-48.23 At low frequency but at high frequency the PSRR increases to -40.27db

4.5 COMPARITION TABLE

SR.NO.	Parameters			
	Av.dif. (20db)	*Av.com. (20db)*	*B.W (Hz)*	*U.G.B.W (MHz)*
Differential Amplifer	26.92	-20.32	4.57M	105.54
Telescopic amplifer	53.67	-18.29	161.27 K	78.408
Folded Cascode	53.22	-17.86	209.96 K	96.06
Miller Compensated	62.83	10.77	68.99K	89.48

P.M (deg)	*S.R (V/uSec)*	*P.C (mW)*	*CMRR (20db)*	*PSRR (20db)*	*O.S (V)*
91.35	133.38	0.2	47.24	-40	1.6
80.38	73.16	0.2	71.96	-39.822	1.61
77.5	78.14	0.33	71.08	-29.77	1.79
53.32	377.31	0.84	52.06	-40.27	1.78

V. CONCLUSION

A comparative analysis of four CMOS operational amplifier topologies has been done under identical biasing conditions using 180 nm technology. And body biasing effect removed cause the source and body is connected for all the MOSFET and The results demonstrate that each topology exhibits distinct performance characteristics. Since we have kept some parameters as constant we are getting some results which are different from the theory

In terms of Bandwidth we got Differential amplifier best for our circuits cause it provides much higher bandwidth compared to other topology's and the power consumption is also very low

Telescopic and Folded Cascode is near around same in everything and since we are operating at 1.8v VDC we did not got much output swing difference to.

The Miller Compensated amplifier provides high gain but the Bandwidth is less than other topologies and the UGBW is also less, Even the differential gain is highest among others because of the common mode gain which we are getting positive, cause the secondary stage is amplifying the singles coming from the differential pair, the differential pair is attenuating the common mode signal but the CS amplifier is again amplifying the single which makes AC positive which reduces the CMRR and the bandwidth we got for this its less cause the capacitor used to Connect the differential pair and CS amplifier is less resulting the bandwidth reduced.

This paper shows the results of different analysis for different topologies and shows how the gain bandwidth and phase margin changes with the topology to topology

VI. FUTURE SCOPE

Future research could concentrate on optimizing these topologies at low supply voltages and more advanced technology nodes.

Further, we could consider maintaining the body biasing and designing the circuit accordingly and use Techniques like adaptive biasing and gain boosting techniques to improve performance characteristics. Also, a layout level study and simulation could be done for the analysis of parasitic effects. Further investigation into incorporating these circuits within larger analog and mixed signal circuits like data converters and sensors could also be undertaken.

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