# Design of a Two-Stage Operational Amplifier with Two Gain Stages and a Buffer Stage Using CMOS Process

Mrs. B. Swapna[1], M. Veera Chaithanya[2], M. Deepika[3], M. Prabhas[4], MD. Ammar[5]
[1]*Assistant Professor, Dept. of ECE, TKR College of Engineering and Technology*
[2,3,4,5]*Student, Dept. of ECE, TKR College of Engineering and Technology*

***Abstract*—Operational amplifiers remain basic building blocks in analog and mixed-signal integrated circuits, but a single- stage CMOS amplifier often cannot deliver the gain and output drive demanded by practical VLSI systems. This work presents the schematic-level design and analysis of a two-stage CMOS operational amplifier with an added buffer stage in 180 nm technology. The architecture combines an NMOS differential input pair, PMOS active loads, a second common-source gain stage, Miller compensation, and an output buffer intended to preserve drive capability under a 10 pF load. The design calcu- lations are organized around a 10 MHz gain-bandwidth target, a 10 V/$\mu$s slew-rate target, an approximately 60° phase margin, and an overdrive voltage of 200 mV. The reported AC simulation shows a gain of about 69.78 dB, while transient analysis indicates a stable output settling near 1.43 V with a settling time of roughly 305 $\mu$s. Power behavior becomes steady after the initial settling interval, which is consistent with the low-power intent of CMOS implementation. The resulting amplifier is suitable for analog signal processing, data-conversion interfaces, and related mixed-signal applications that require stable, moderate- bandwidth voltage amplification.**

***Index Terms*—CMOS operational amplifier, two-stage op-amp, Miller compensation, analog VLSI, 180 nm CMOS, Cadence Virtuoso, buffer stage**

## I. INTRODUCTION

Operational amplifiers are used throughout analog and mixed-signal electronics because they provide voltage ampli- fication, signal conditioning, filtering support, and interface capability for larger systems. In practical form, an op-amp accepts a differential input and produces a single-ended output, ideally with very high gain, very high input impedance, and very low output impedance. Modern realizations cannot reach the ideal case, but integrated implementations still try to approach it closely enough for sensor interfaces, active filters, analog-to-digital converters, voltage regulators, and communi- cation circuits. The move toward compact and battery-powered systems has made low-power op-amp design especially rele- vant, and CMOS technology has become the preferred plat- form because it combines low static power consumption, strong immunity to noise, and compatibility with large-scale integration.

The need for a two-stage CMOS topology appears when a single-stage amplifier can no longer satisfy the required gain and load-driving conditions. A single-stage circuit is attractive because it is simpler and usually lighter in power, yet its volt- age gain and output capability are often inadequate for weak-signal amplification or for operation with nontrivial loads. A two-stage arrangement offers a more practical balance. The first stage supplies differential amplification and high input impedance, the second stage contributes additional gain, and a buffer stage can be inserted to improve output drive and isolate the internal nodes from the external load.

That structure is particularly useful in CMOS analog design. Complementary NMOS and PMOS devices support low-power biasing, integration with digital circuitry, and straightforward current-mirror implementation. At the same time, multi-stage amplification introduces new design pressure. As gain is increased, bandwidth and stability become more difficult to manage, and compensation can no longer be treated as an afterthought. The project document addresses this design space by focusing on a two-stage CMOS op-amp with a buffer stage, designed for stable operation and low-power behavior in a 180 nm process.

The objective of the present work is to restate that

project in IEEE-style form while staying strictly within the information reported in the source document. The design target is a 180 nm CMOS operational amplifier with high voltage gain, low power consumption, high input impedance, low output impedance, and compensated frequency response. The reported evaluation is schematic-level and simulation-based, with emphasis on gain, transient response, and qualitative power behavior under the specified operating conditions.

## II. RELATED WORK

The reviewed literature shows that two-stage CMOS op- amp design remains a mature but still active topic because no single topology solves gain, bandwidth, power, and stability at once. Bharath Reddy and Gowda compare 180 nm and 45 nm realizations of a two-stage op-amp and show how scaling affects speed, power dissipation, and frequency re- sponse [1]. Their work is useful in showing the direction of technology-node trends, but it remains limited to simulation- based validation. As noted in the source project, the absence of hardware realization and parasitic-aware verification leaves
uncertainty between ideal schematic behavior and physical implementation.

Zaidi *et al.* study compensation methods for CMOS oper- ational amplifiers and compare conventional Miller compen- sation, indirect Miller compensation, and negative-feedback- based approaches [2]. That contribution is valuable because it isolates the stability problem rather than hiding it inside a larger design narrative. Even so, the work is mainly centered on phase margin and oscillation control. The project document points out that a narrow focus on stability does not fully address power efficiency, slew rate, or gain-bandwidth trade- offs, all of which matter in low-power analog systems.

Yuan and Fan present a two-stage CMOS operational am- plifier in 180 nm technology and report a design route aimed at high gain and improved output swing [3]. The strength of that work lies in its practical orientation and its accessible design explanation. Its limitation, according to the project review, is the lack of comparison across additional technology nodes. Since scaling affects leakage, speed, noise, and power, a single-node treatment does not fully expose the design trade- offs that a VLSI designer eventually faces.

Chanapromma and Mahattanakul introduce a current-buffer- based procedure for two-stage CMOS op-amps and emphasize improved gain as well as stronger load-driving ability [4]. The inclusion of a current buffer is directly relevant to buffer-assisted architectures because it reduces interstage loading and improves output handling. The source document, however, observes that the treatment is less detailed on compensation strategy and phase-margin improvement. Without those details, it is harder to judge the full stability envelope of the amplifier. Kumar *et al.* approach CMOS op-amp design from the Cadence implementation side and give a practical route for schematic entry, simulation, and basic evaluation [5]. Kuendi- ger *et al.* provide a related tutorial perspective for Cadence schematic design in a CMOS process environment [6]. Both references are useful for workflow and learning, but neither is presented as a deep performance-optimization study. The project review notes that advanced checks such as post-layout complexity. analysis and process-voltage-temperature (PVT) variation are not treated in sufficient detail, which limits robustness claims.

Classical compensation literature gives a deeper foundation for the stability side of this design problem. Ahuja showed that a current-buffer-oriented compensation path can widen capacitive-load tolerance and improve supply-rejection behav-ior in CMOS op-amps [7]. Eschauzier *et al.* then demonstrated multipath nested Miller compensation for simultaneously high gain and high speed [8], while You *et al.* and Leung and Mok analyzed multistage compensation strategies based on nested transconductance-capacitance and nested Miller con-cepts in a more systematic way [9], [10]. Lee and Mok later proposed active-feedback compensation for low-power multistage amplifiers [11], and Hurst *et al.* examined Miller compensation with current buffers in fully differential two- stage CMOS op-amps [12]. Together, these works make it clear that compensation choice cannot be separated from bandwidth, settling behavior, load drive, and implementation complexity.

A broader conclusion follows from the literature survey. Existing studies often emphasize one axis of

performance at a time, such as gain improvement, compensation, or design flow, while leaving other requirements only lightly examined. Noise, slew rate, parasitic sensitivity, and real-world variation are not always quantified with the same care as gain or stability. The project therefore positions its contribution as a compact, simulation-based design exercise that combines high gain, compensated stability, moderate bandwidth targets, and load-driving capability in a 180 nm CMOS implementation.

## III. THEORETICAL BACKGROUND

The theoretical basis of the amplifier follows standard CMOS analog design principles built around differential am- plification, current-mirror loading, multi-stage gain, and com- pensation [13]– [15], [16]– [19]. The central idea of the input stage is differential operation: the circuit responds to the volt- age difference between two input terminals while suppressing any common-mode component. This behavior is important because common-mode disturbances often appear as noise or interference. In a CMOS realization, the differential pair is typically formed with NMOS transistors so that higher electron mobility can be used to obtain stronger transconductance for a given bias condition.

Those broader analog-design references are also useful because they give the hand-analysis framework for transcon- ductance, output resistance, pole locations, output swing, and noise in multistage CMOS amplifiers. That perspective helps connect the project's transistor-level sizing equations with the larger design trade-offs that govern gain, stability, and power consumption in practical op-amp implementations [16]– [19]. MOSFET region of operation is equally important. For analog voltage amplification, the transistors are biased in saturation, where the drain current is controlled mainly by the gate overdrive rather than by the drain-source voltage. In the design calculations reported in the project document, the drain current relation is written as

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} V_{ov}^2, \qquad (1)$$

where $\mu_n C_{ox}$ is the process transconductance factor, $W/L$ is the device aspect ratio, and $V_{ov}$ is the overdrive voltage. This expression directly links device sizing, current level, and overdrive requirement. When the aspect ratio increases at fixed current and process parameters, transconductance can be improved, which in turn supports higher gain.

The first gain stage in a two-stage op-amp uses a differential pair with active loads. The active PMOS current-mirror load raises the effective output resistance of the stage and converts the differential signal into a single-ended voltage. The source document describes this stage as the point where high input impedance, initial voltage gain, and common-mode rejection are established. The second stage then takes the first-stage output and applies additional amplification through a common- source configuration. In practice, the overall gain is obtained

by cascading these two stages rather than forcing a single stage to provide all the required amplification.

Frequency response introduces the main difficulty. Internal capacitances and node resistances create multiple poles in the transfer function. As the input frequency increases, the gain rolls off and the phase shifts. If the loop phase approaches $180^\circ$ while the loop gain remains above unity, oscillation becomes possible. To control this behavior, the project uses Miller compensation, in which a capacitor is connected be- tween the output of the second stage and the intermediate node. This capacitor introduces a dominant pole at lower frequency and makes the gain fall earlier, thereby improving the phase margin and stabilizing the amplifier.

Two performance concepts are central to the reported design calculations: gain-bandwidth product (GBW) and slew rate. For the compensated two-stage amplifier, the project document expresses the relationship between input-stage transconduc- tance and GBW as

$$g_m = 2\pi\, GBW\, C_L, \qquad (2)$$

with $C_L$ denoting the load capacitance. Slew rate is treated as the maximum rate of output-voltage change and is governed by the current available to charge or discharge the effective load capacitor. The reported calculation uses

$$SR = \frac{I_O}{C_L}, \qquad (3)$$

which makes the current requirement explicit once $SR$ and $C_L$ are fixed.

The design document also gives the transconductance- current-size relation as

$$g_m = \sqrt{2 I_D \mu_n C_{ox} \frac{W}{L}} . \quad (4)$$

This expression is useful because it links the required $g_m$ back to bias current and geometry. In other words, bandwidth, gain, and power are not independent choices. A larger $g_m$ supports bandwidth, but it must come from either larger current or larger device size. The same compromise shows up in noise and power behavior. The project notes that CMOS op-amps exhibit thermal, flicker, and shot-noise components, and that sizing and biasing influence both signal integrity and energy consumption. For low-power analog blocks, the designer is constantly working across these trade-offs rather than optimizing a single parameter in isolation.

## IV. PROPOSED METHODOLOGY

The proposed amplifier is organized as a three-part signal path: a differential input stage, a second gain stage, and a buffer stage, with a Miller compensation capacitor tied around the first two stages. The document describes the architecture as a two-stage CMOS operational amplifier enhanced by an additional output buffer, all implemented in Cadence using a 180 nm process environment. A 1.8 V supply is identified in the schematic description, and the biasing network is

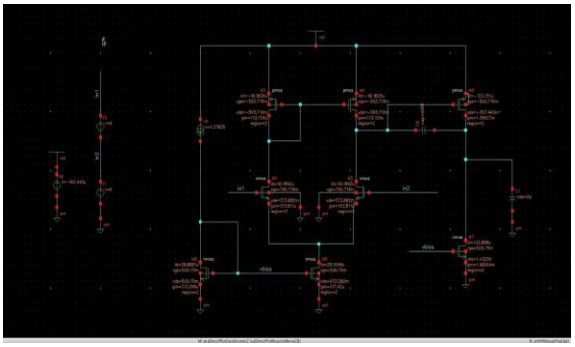

Fig. 1. Cadence schematic of the reported two-stage CMOS operational amplifier with Miller compensation and output loading.

arranged so that the transistors remain in saturation for linear amplification.

Figure 1 shows the Cadence-level implementation used for the reported simulations. The differential input pair, active- load devices, gain stage, compensation capacitor, and output- loading nodes are visible directly in the schematic, making the stage-wise operation discussed in this section easier to trace. The differential input stage forms the electrical front end of the design. Two matched NMOS transistors, labeled $M_1$ and $M_2$ in the project description, receive the input signals. Their sources are tied together and connected to a tail current source so that the total bias current remains controlled while the branch currents redistribute according to the input difference. PMOS devices, identified as $M_3$ and $M_4$, act as an active current-mirror load. This combination performs two jobs at once: it amplifies the differential signal and converts it intoa single-ended output that can be passed to the next stage.

Because the first stage sits directly at the input, its influence on input impedance, noise rejection, and offset sensitivity is especially strong.

The second stage is implemented as a common-source gain stage. Its purpose is not subtle; it provides most of the remaining voltage gain needed to approach the overall design target. The signal from the differential stage is applied to the gate of the second-stage device, and the amplified output is obtained at the drain node. The appeal of this stage is its ability to produce large gain with a relatively compact transistor arrangement. Its drawback is equally familiar: once the second high-gain stage is added, the amplifier acquires additional poles and the stability problem becomes unavoidable.

That is why the compensation network is not optional in the reported design. A capacitor $C_c$ is connected between the second-stage output and the first-stage output node. The project identifies this arrangement as Miller compensation. The capacitor shifts the dominant pole to lower frequency and im- proves phase margin so that the op-amp can tolerate negative feedback without oscillation. The compensation choice also interacts with bandwidth and slew rate. A larger capacitor tends to help stability but slows the dynamic response, while a smaller capacitor makes the circuit faster but can reduce phase margin. The document therefore treats compensation as part of

TABLE I REPORTED DESIGN SPECIFICATIONS

| Parameter | Value |
|---|---|
| Technology | 180 nm CMOS |
| Gain-bandwidth target | 10 MHz |
| Load capacitance, $C_L$ | 10 pF |
| Slew-rate target | 10 V/$\mu$s |
| Phase-margin target | 60° |
| Voltage-gain target | $\geq$ 70 dB |
| Overdrive voltage, $V_{OV}$ | 200 mV |

the core methodology rather than as a small correction added after the gain stages are sized.

Bias generation is handled through transistors and mirrors that establish reference currents and voltages for the internal stages. The source document mentions devices such as $M_7$ and $M_8$ in the biasing network and explains that current mirrors help maintain operating conditions across the amplifier. Stable biasing is important here because the intended behavior of the differential pair, the second gain stage, and the buffer all depends on remaining in saturation. If the bias point drifts too far, gain, linearity, and dynamic behavior will change together. The buffer stage is placed at the output to lower output impedance and improve current-driving capability. In the project text it is described as a source-follower-like output stage that isolates the internal gain nodes from the load. This is useful for two reasons. First, it allows the output signal to be delivered to the load with less degradation. Second, it reduces the sensitivity of the earlier stages to load variation. The design therefore treats the buffer not as an accessory but as an enabling block for reliable signal transfer under capacitive loading.

The signal flow is direct. A differential input is first con- verted into a single-ended amplified signal. That signal is then boosted by the second gain stage. The compensation path shapes the frequency response so that the cascade remains stable, and the final buffer delivers the output to the external load. Within the limits of the source document, this methodol- ogy is intended to balance gain, stability, and power efficiency rather than pushing only one metric to an extreme value.

## V. DESIGN AND IMPLEMENTATION

The reported implementation uses a 180 nm CMOS process. The project document justifies this choice on practical grounds. Compared with smaller technology nodes, 180 nm remains easier to study, less sensitive to short-channel effects and leak- age, and still capable of supporting useful analog and mixed-signal building blocks. It also provides a familiar environment for educational VLSI work and for initial prototyping before more aggressive scaling is attempted.

The main design specifications extracted from the source document are listed in Table I. These values define the operating target for the sizing exercise and for the subsequent simulation study.

TABLE II REPORTED TRANSISTOR ASPECT RATIOS

| Transistor group | Reported $W/L$ |
|---|---|
| $M_1$, $M_2$ | 26 |
| $M_3$, $M_4$ | 13 |
| $M_5$, $M_6$, $M_7$, $M_8$ | 20 |
| Tail transistor ($M_9$) | 26 |

The first sizing step is based on the slew-rate requirement. Using the specification $SR = 10$ V/$\mu$s and the load capacitance $C_L = 10$ pF, the document computes the bias current requirement as

$$I_0 = SR \times C_L = 100\,\mu\text{A}. \qquad (5)$$

This value sets the current scale for the op-amp design. It is a key number because it ties dynamic response directly to power consumption; increasing current would improve charging speed but also raise energy use.

The next step is to estimate the differential-pair aspect ratio. Using $I_D = 100\ \mu$A, $V_{ov} = 0.2$ V, and the process factor implied by the source calculation, the reported drain-current

sizing gives

$$\left(\frac{W}{L}\right)_{1,2} \approx 26. \qquad (6)$$

A separate calculation based on the transconductance require- ment begins with the GBW expression. For a 10 MHz design target and a 10 pF load, the project computes

$$g_m \approx 2\pi \times 10^7 \times 10 \times 10^{-12} \approx 628\,\mu\text{S}. \quad (7)$$

Substituting this result into the reported $g_m$ relation produces another estimate for the input-pair aspect ratio, approximately

21. The final sizing summary in the project document never- theless retains an aspect ratio of 26 for $M_1$ and

$M_2$, so that value is treated here as the implemented design choice.

The source document reports the aspect-ratio summary shown in Table II. It also notes a channel length of $L = 1\ \mu$m for the calculation summary, so the width can be obtained from $W = (W/L)L$. For example, $W/L = 26$ corresponds to $W = 26\ \mu$m when $L = 1\ \mu$m. The use of a 1 $\mu$m channel length within a 180 nm process is not contradictory; it simply means the devices are not forced to minimum length in this design exercise.

Implementation is carried out in Cadence Virtuoso using the available 180 nm device library. The workflow described in the source document begins with schematic capture, where the designer selects transistors and circuit elements from the process library and connects them into the complete op-amp. After schematic entry, simulation is performed to evaluate how the circuit is expected to behave if fabricated. The generated reports are then examined to identify gain, transient behavior, and power trends under the stated operating conditions. In the present project, the work is limited to schematic-level simulation and result evaluation in Cadence [5], [6].

The flow shown in Fig. 2 summarizes the simulation path followed in this work. It starts from schematic capture, pro- ceeds through simulator setup and response analysis, and ends with inspection of the generated waveforms and numerical results. This presentation is consistent with the scope of the paper, which is restricted to schematic-level design and simulation rather than layout realization.

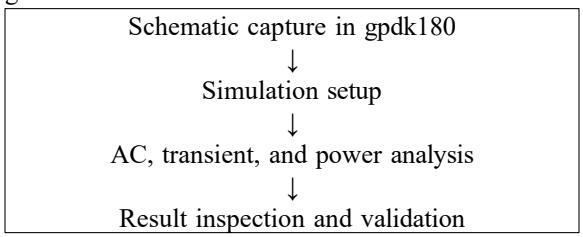


Fig. 2. Cadence Virtuoso flow summarized in the source document.

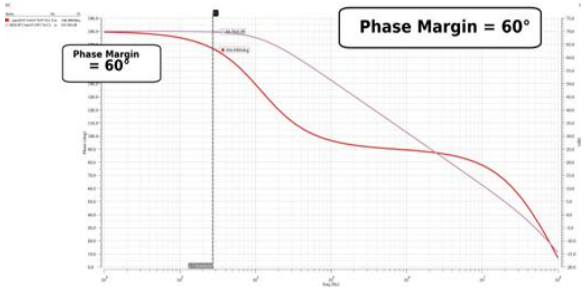


Fig. 3. Simulated AC response showing the reported gain of about 69.78 dB and a phase margin of approximately 60°.

From a design standpoint, the implementation strategy is conventional but sound. The differential stage establishes input sensitivity and common-mode rejection, the second stage provides the majority of the remaining gain, the Miller capacitor manages the multi-pole response, and the buffer protects the internal nodes from the load. The design therefore follows a sequence that is quite typical for analog CMOS op- amps, while the chosen numerical targets fix the circuit to a moderate-bandwidth, low-power operating region.

## VI. RESULTS AND DISCUSSION

The project document reports simulation results in terms of AC response, transient behavior, and power trends. The most explicit numerical result is the AC gain, which is stated as approximately 69.78 dB. This value is close to the design target of at least 70 dB from Table I. The difference is only about 0.22 dB, so from a practical schematic-level viewpoint the design can be regarded as nearly meeting the intended gain objective.

The AC analysis is presented for a 0.8 V input case, with an additional AC response figure also shown for a 1.6 V input condition. The accompanying discussion states that the phase response indicates stable operation over the frequency range. Although the project document does not tabulate a numer- ical phase-margin result, the qualitative observation matters because the circuit is explicitly multi-stage and therefore sen- sitive to pole placement. The presence of stable phase behavior is consistent with the intended role of Miller compensation in the proposed architecture.

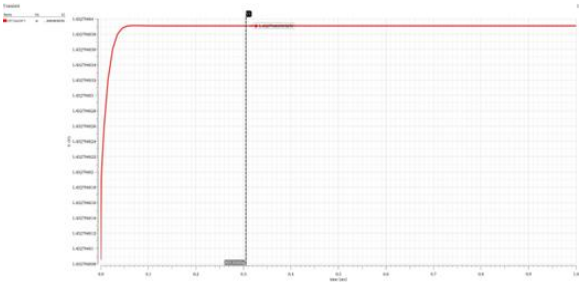

Fig. 4. Transient output response indicating settling near 1.43 V with a settling time of about 305 $\mu$s.

Transient analysis provides another important check because it exposes how the amplifier behaves in time rather than only in small-signal frequency response. The source document reports that the output settles to approximately 1.43 V and that the settling time is around 305 $\mu$s. Just as importantly, the waveform is described as smooth and stable. This is a useful observation in a two-stage design with compensation, because time-domain ringing or repeated overshoot would immediately suggest that the pole-zero arrangement is not well controlled. Within the limitations of the source data, the transient response therefore supports the claim that the compensation network and output stage are functioning as intended.

The power result is described qualitatively rather than numerically. According to the reported transient power plot, power initially varies during the settling interval and then approaches a constant steady-state value. No absolute power number is provided in the project text. It would be inap- propriate to infer one from the figure labels alone, so the present paper limits itself to the stated conclusion: the op- amp exhibits steady behavior after the initial transient and is considered suitable for low-power applications in the context of the reported simulation.

The practical relevance of the reported behavior is also worth noting. The source document repeatedly associates this kind of two-stage CMOS op-amp with sensor interfaces, analog signal-processing chains, communication systems, and data-conversion blocks. That connection is reasonable within the reported evidence. High input impedance reduces loading at the front end, differential operation improves noise rejection, and the output buffer helps the circuit tolerate load interaction more gracefully than a simpler unbuffered stage chain.

A concise comparison between design targets and reported observations is given in Table III. The table makes one point clear. Some quantities, such as gain and transient settling, are explicitly stated in the source. Other quantities, such as GBW, slew rate, and phase margin, are treated as design targets or as qualitative checks rather than as fully tabulated simulated results. That distinction is important if the work is to remain factually accurate.

From an analog design perspective, the results reflect a sensible compromise. The gain is high enough to support pre- cision amplification in moderate-bandwidth applications, and

TABLE III COMPARISON OF DESIGN TARGETS AND REPORTED RESULTS

| Parameter | Target or setup | Reported result / observa- tion |
|---|---|---|
| Voltage gain | $\geq 70$ dB | 69.78 dB from AC analysis |
| GBW | 10 MHz | Used as a design specifica- tion; no separate simulated numerical value tabulated |
| Slew rate | 10 V/$\mu$s | Used in design calcula- tions; no separate simu- lated numerical value tab- ulated |
| Load capacitance | 10 pF | Applied as the stated load condition |
| Phase margin | 60° target | Stable phase behavior stated qualitatively; no explicit numerical phase margin listed |
| Transient output | Not separately tar- geted | Output settles near 1.43 V |
| Settling time | Not separately tar- geted | Approximately 305 $\mu$s |
| Power behavior | Low-power intent | Initial variation followed by steady-state stabiliza- tion; absolute power not re- ported |

that settles near 1.43 V in roughly 305 $\mu$s. Power behavior stabilizes after the initial transient interval, supporting the low- power intent of the CMOS implementation. Taken together, these results indicate that the design reaches a useful com- promise between amplification, stability, and efficiency at the schematic level.

the compensated response suggests that the two-stage structure is under control rather than marginally stable. The presence of the buffer stage is also meaningful in interpretation, even though its effect is expressed qualitatively. The document repeatedly associates the buffer with lower output impedance, reduced loading between stages, and stronger drive capability, which helps explain why the amplifier is presented as suitable for sensor interfaces, data converters, and communication- oriented analog blocks.

There are also limits to what can be concluded. Since the project document does not provide explicit simulated values for GBW, phase margin, or absolute power dissipation, the evaluation of these quantities remains indirect. The design calculations indicate what the circuit was intended to meet, and the qualitative simulation descriptions suggest that the circuit behaves consistently with those goals. Still, schematic-level confirmation of gain and transient settling is stronger than the evidence currently available for the remaining metrics. That does not invalidate the reported design, but it does define the boundary of the present analysis.

## VII. CONCLUSION

A two-stage CMOS operational amplifier with a buffer stage has been presented in 180 nm technology using the information reported in the project document. The design combines a differential NMOS input pair, active PMOS loads, a common- source second gain stage, Miller compensation, and a buffer-oriented output stage to balance gain, stability, and load- driving capability. The sizing procedure is organized around a 10 MHz GBW target, a 10 V/$\mu$s slew-rate target, a 10 pF load, and a 60$^{\circ}$ phase-margin target.

The reported simulations show that the amplifier achieves a gain of about 69.78 dB and exhibits a stable transient response

## VIII. FUTURE WORK

The most immediate extension of this work is post-layout verification. The literature review in the project document makes it clear that parasitic capacitances and resistances can alter the behavior of a multi-stage amplifier, so extracted post- layout simulation is needed before stronger implementation claims are made. A second priority is full PVT analysis so that gain, stability, and transient response can be checked under supply, process, and temperature variation.

Technology scaling is another natural direction. Since the reviewed literature already compares 180 nm with smaller nodes, the same architecture could be revisited in 90 nm or 45 nm environments to study speed, power, and sizing trade-offs more closely. Finally, the low-power aspect can be developed further through improved biasing and current optimization. Those steps would strengthen the design and make its performance more convincing for practical mixed- signal integration.

## REFERENCES

[1] R. Bharath Reddy and S. K. Gowda, “Design and Analysis of CMOS Two Stage OP-AMP in 180nm and 45nm Technology,” *International Journal of Engineering Research & Technology (IJERT)*, vol. 4, no. 5, pp. 1100–1103, May 2015.

[2] M. Zaidi, I. Grout, and A. K. A’Ain, “Evaluation of Compensation Techniques for CMOS Operational Amplifier Design,” in *Proc. Int. Conf. on IC Design and Technology (ICICDT)*, pp. 5–8, Jun. 2018.

[3] T. Yuan and Q. Fan, “Design Of Two Stage CMOS Operational Amplifier in 180nm Technology,” *arXiv preprint* arXiv:2012.15737, Dec. 2020.

[4] C. Chanapromma and J. Mahattanakul, “Improved Design Procedure for Two-Stage CMOS Op Amp Employing Current Buffer,” in *2020 17th Int. Conf. on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)*, Phuket, Thailand, pp. 384–387, 2020.

[5] S. Kumar, A. Sharma, P. Jangra, P. Rathee, and R. Yadav, “Design of CMOS Operational Amplifier in 180nm Technology,” *International Journal of Innovative Research in Computer and Communication Engi- neering*, vol. 5, no. 4, pp. 8779–8784, Apr. 2017.

[6] T. Kuendiger, J. Schrey, I. Taha, Y. Lin, T. Dai, L. Liang, S.-T. Huang, and Y. Huang, “Cadence Op-Amp Schematic Design Tutorial for TSMC

CMOSP35," technical tutorial, Dec. 7, 2001.

[7] B. K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 18, no. 6, pp. 629–633, Dec. 1983.

[8] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100- MHz 100-dB Operational Amplifier With Multipath Nested Miller Compensation Structure," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 12, pp. 1709–1717, Dec. 1992.

[9] F. You, S. H. K. Embabi, and E. Sa´nchez-Sinencio, "Multistage Am- plifier Topologies With Nested Gm-C Compensation," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 2000–2011, Dec. 1997.

[10] K. N. Leung and P. K. T. Mok, "Analysis of Multistage Amplifier- Frequency Compensation," *IEEE Transactions on Circuits and Sys- tems I: Fundamental Theory and Applications*, vol. 48, no. 9, pp. 1041– 1056, Sep. 2001.

[11] H. Lee and P. K. T. Mok, "Active-Feedback Frequency-Compensation Technique for Low-Power Multistage Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 511–520, Mar. 2003.

[12] P. J. Hurst, S. H. Lewis, J. P. Keane, F. Aram, and K. C. Dyer, "Miller Compensation Using Current Buffers in Fully Differential CMOS Two- Stage Operational Amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 2, pp. 275–285, Feb. 2004.

[13] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 3rd ed. Oxford, U.K.: Oxford University Press, 2012.

[14] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001.

[15] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd ed. Hoboken, NJ, USA: Wiley-IEEE Press, 2010.

[16] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed. Hoboken, NJ, USA: Wiley, 2009.

[17] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. New York, NY, USA: Wiley, 1997.

[18] W. M. C. Sansen, *Analog Design Essentials*. New York, NY, USA: Springer, 2006.

[19] J. H. Huijsing, *Operational Amplifiers: Theory and Design*, 2nd ed. Dordrecht, The Netherlands: Springer, 2011.