

Comparative Performance Analysis of Three LDO Architectures In 180 Nm CMOS

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Abstract—Three LDO circuit topologies fabricated in a commercial 180 nm CMOS technology and simulated in Cadence Spectre have been compared in this paper. The first one is a Normal LDO circuit with no compensation. It can reach a DC loop gain of ≈ 80 dB, while oscillating at any load current values, from phase margins -6.2° (0 mA) to -83.9° (30 mA). The second one introduces the Miller compensation with $C_c = 27$ pF and $R_z = 820 \Omega$, resulting in loop stabilisation, with phase margins varying from 46.5° (7.5 mA) to 39° (30 mA). At the same time, PSRR reaches -73 dB at 1 Hz frequency. Still, transient spikes can be observed due to constant biasing at $120 \mu\text{A}$. The third circuit topology features a folded cascode error amplifier and Class-AB push-pull output stage with external compensation of $4.7 \mu\text{F}$, having a 90.6° phase margin, along with -62.3 dB high-frequency PSRR at 1 MHz. Nonetheless, during load step test from 1 mA to 50 mA, its output fails catastrophically and can produce only 11.2 mA out of 50 mA requested. Differential to single-ended signal contentions have been identified as the reason behind

Large size transistor will have a considerable gate capacitance, C_{gg} . Slew rate of the error amplifier depends on its tail current,

$$SR = \frac{I_{\text{tail}}}{C_{gg}} \quad (1)$$

For a transistor of width $W = 1000 \mu\text{m}$, $C_{gg} \approx 1.5$ pF. To achieve a slewing of $SR = 1 \text{ V}/\mu\text{s}$, the tail current will be $I_{\text{tail}} = 1.5$ mA. This value of I_{tail} is not feasible for battery-driven electronics that should consume less than $100 \mu\text{A}$ in quiescent mode.

Adaptive biasing and Class AB buffering have been suggested to address this problem [5], [6]. Nevertheless, the successful realization depends on proper signaling between the error amplifier and the buffer stage.

In this work, three LDOs fully simulated in Cadence 180 nm CMOS technology are compared:

- Normal LDO: three-stage LDO without compensation, providing maximum DC gain, however being unstable by nature;
- Miller LDO: same structure as above, however with compensation according to Miller principle ($C_c = 27$ pF, $R_z = 820 \Omega$), which makes it stable, although with limited slew-rate;
- Adaptive LDO: folded cascode error amplifier with a push-pull current buffer, which guarantees high slew-rate and low dropout, however failure under transients.

The same testbench is used for the simulations performed for all the aforementioned designs, making comparison of different trade-offs possible for parameters such as gain, stability, bandwidth, PSRR, and transients.

The structure of the paper is as follows. First, prior art concerning the design of LDO compensation and

I. INTRODUCTION

The Low-Dropout regulator (LDO) has become a key component for the power management system in contemporary electronic devices especially when supplying current to the analog, RF, and digital circuits which are noise-sensitive. Contrary to the switching converter, the LDO has negligible output ripple, very good PSRR and simplicity of design. Nonetheless, there exist two main challenges while designing high-output current LDOs and these include stability and transient response.

The pass transistor of the LDO should have a very large size to ensure low dropout voltage, such as 200 mV at 50 mA. In this case, the $R_{ds,on}$ should equal $\approx 4 \Omega$, and to meet this objective, the transistor will need a size of a few hundreds of microns in the 180 nm process.

adaptive biasing is given in Section II. Next, in Section III the design of the circuits discussed is described. Simulations results are given in Section IV, including DC, AC analysis, PSRR, and transient performance. Conclusions and guidelines for circuit design are made in Section V.

II. LITERATURE SURVEY

A. Compensation Techniques

The stability of operation is the first priority in multi-stage LDO regulators. The most simple and reliable approach for obtaining stable operation is dominant-pole compensation through adding a large external capacitor C_L on the output side [2]:

$$\omega_{p,dom} \approx \frac{1}{R_{out}C_L} \quad (2)$$

This ensures that the dominant pole is placed at an extremely low frequency where the loop gain begins to decrease before the phase degradation caused by internal poles occurs. But in the present case, an additional capacitor needs to be employed and the bandwidth is constrained.

Speaking of the on-chip solution, it is important to resort to Miller compensation since it is still the most widely used form of compensation [1], [4]. The concept involves placing a capacitor C_c in parallel with the high-gain stage in order to obtain a dominant pole from the Miller effect:

$$\omega_{p1} \approx \frac{1}{g_{m2}R_{out1}R_{out2}C_c} \quad (3)$$

A nulling resistor R_z connected in series with C_c will create a zero that can be used for cancelling the non-dominant pole:

$$\omega_z = \frac{1}{C_c \left(\frac{1}{g_{m2}} - R_z \right)} \quad (4)$$

B. Adaptive Biasing and Slew-Rate Improvement

The application of adaptive biasing can help enhance the transient response without increasing the quiescent current. The work done by Hazucha et al. [5] utilized the push-pull output buffer design, delivering the high current upon the presence of loading. Impedance buffer attenuation method, suggested by Al-Shyoukh et al. [6], reduces the impedance of the buffer stage

output, moving the parasitic poles to higher frequencies. Flip voltage follower (FVF) architecture [8] ensures low impedance as well as fast settling time.

New inventions continuously help push the boundaries. The sub-1V capacitor-less LDO for IoT applications by Chong and Mok [11] provides excellent slew rate performance and decent PSR. Another notable invention in the field of LDOs comes from Ho and Leung [12]. They presented their LDO with the push-pull buffer design, featuring the adaptive biasing technique, with the figure-of-merit of 0.6 ps. Kim et al. [13] developed their transient enhanced LDO featuring nested Miller compensation in the automobile domain. The last example by Zhang et al. [14] shows a novel LDO with 0.5 ps FOM made in 180 nm CMOS technology. Adaptive biasing technique and push-pull buffer were used in their design.

C. Gaps in the Literature

There are quite a few successes presented in the literature concerning LDOs. However, one could wonder whether there were any unsuccessful attempts regarding the topic. What happens when the error amplifier (folded cascode), with differential outputs, drives the Class-AB push-pull buffer stage? Which test methods can reveal the problem and which can conceal it?

Here, we explore these topics, demonstrating a real-life case study in which both the normal and Miller-based LDO designs succeed whereas the adaptive LDO, made up of proven modules, performs unexpectedly.

III. METHODOLOGY

All circuits were designed and simulated in a 180 nm CMOS technology using BSIM3v3 models. DC, AC analysis (loop gain through. stb), PSRR, and transient simulations were performed using Cadence Spectre. Testbenches included similar load steps, corner cases, and sweep analyses to ensure a fair comparison.

All three designs aim at driving 30 mA from 3.3 V supply voltage (Normal and Miller LDOs) and 50 mA from 1.8 V supply voltage (Adaptive LDO). Block diagrams are illustrated in Figs. 1, 2, and 3.

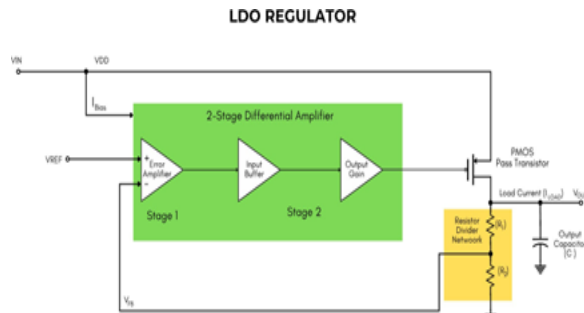


Fig. 1: Block diagram of the Normal LDO (uncompensated three-stage)

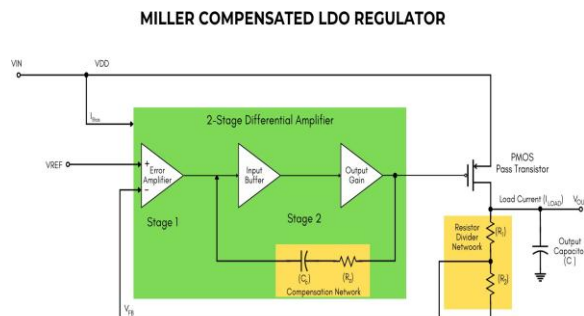


Fig. 2: Block diagram of the Miller-compensated LDO.

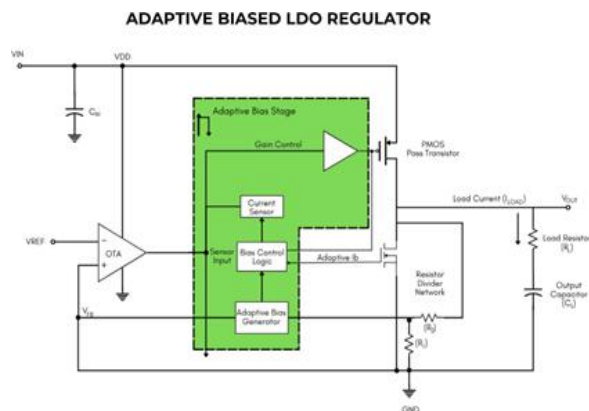


Fig. 3: Block diagram of the Adaptive LDO (folded cascode + Class-AB buffer)

A. Normal LDO (Uncompensated Three-Stage)

The three-stage cascade for the Normal LDO consists of a first-stage NMOS differential pair, a second-stage PMOS common source amplifier, and a third-stage PMOS pass transistor. Resistors $R_1 = 67 \text{ k}\Omega$ and $R_2 = 100 \text{ k}\Omega$ provide $V_{OUT} \approx 1.503 \text{ V}$ based on $V_{REF} = 0.9 \text{ V}$. Compensation has not been implemented explicitly; there is only the load capacitance $C_L = 200$

TABLE I: Normal LDO transistor dimensions (W/L in $\mu\text{m}/\mu\text{m}$)

Device	W (μm)	L (μm)
NM0, NM1 (diff pair)	50	0.18
NM2–NM4 (current mirrors)	9	0.18
PM1, PM2 (active loads)	10, 20	0.18
PM3 (second stage)	720	0.18
PM0 (pass PMOS)	360	0.18

The loop gain of the proposed LDO topology has a value of around 80 dB and arises due to multiplication of all three stage gains. But all three stages create poles at low frequencies. As a result, the total phase shift of the loop reaches almost 270° before the unity-gain frequency, and oscillation will definitely occur.

B. LDO Miller Compensation

Miller compensation LDO is constructed using normal LDO by adding an extra compensating circuit made up of $C_c = 27 \text{ pF}$ and $R_z = 820 \Omega$, which connects the drain terminal of PM3 to the output of LDO. In this case, the poles would be separated into two groups, where one pole exists in very low frequencies and other poles exist in high frequencies. Using a nulling resistor, it would be possible to design a pole in the left half plane, which would counteract the second non-dominant pole. Other parameters will remain constant and would correspond to those of normal LDO. Width of pass transistor would still remain the same as $360 \mu\text{m}$.

C. Adaptive LDO (Folded Cascode + Class-AB Buffer)

Adaptive LDO has been developed to operate on a lower voltage of 1.8 V and deliver more load current (50 mA).

It contains three stages:

1) Folded cascode error amplifier (Stage 1):

PMOS-input differential pair with folded cascode loads, tail current $20 \mu\text{A}$. This topology provides high DC gain ($> 60 \text{ dB}$) and wide input common-mode range.

2) Class-AB inverting buffer (Stage 2):

PMOS pull-up (PM8, $W = 50 \mu\text{m}$, $10 \mu\text{A}$ static) and NMOS pull-down (NM6, $W = 100 \mu\text{m}$, capable of $500 \mu\text{A}$ dynamic). This buffer is intended to drive the large gate capacitance of the pass transistor with high slew rate.

3) Pass PMOS (Stage 3):

Width 1000 μm with multiplier $M = 20$, effective width 20,000 μm . This device is sized to achieve $R_{ds,on} \approx 2\ \Omega$ at $V_{GS} = 0.6\ \text{V}$, supporting 50 mA with a dropout of 100 mV.

The feedback network uses $R_{top} = R_{bot} = 500\ \text{k}\Omega$ to set $V_{OUT} = 1.2\ \text{V}$ from $V_{REF} = 0.6\ \text{V}$. Frequency compensation is provided solely by an external $C_L = 4.7\ \mu\text{F}$ capacitor at the output – a deliberate choice to guarantee stability at the cost of bandwidth. Key transistor dimensions are listed in Table II.

TABLE II: Adaptive LDO key transistor dimensions (W/L in $\mu\text{m}/\mu\text{m}$)

Device	W (μm)	L (μm)
PM0 (tail)	20	0.5
PM1, PM2 (input pair)	10	0.5
PM3–PM5 (cascode)	5,5,30	0.5
NM1, NM2 (input pair)	10	0.5
NM3, NM4 (cascode)	5	0.5
NM5 (bias)	20	0.5
PM8 (buffer pull-up)	50	0.5
NM6 (buffer pull-down)	100	0.5
Pass PMOS	1000 (M=20)	0.18

IV. RESULTS AND DISCUSSION

A. Normal LDO Results

1) DC and Regulation:

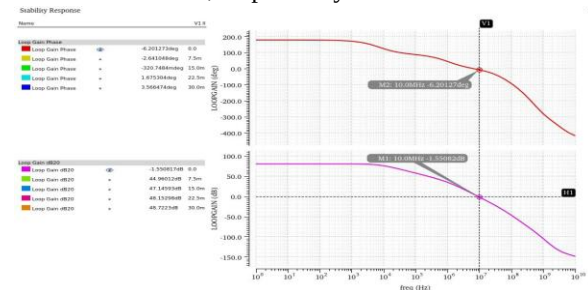
In DC simulation, $V_{OUT} = 1.549\ \text{V}$ was obtained at 10.24 mA of nominal load current. The small deviation (46 mV) from the expected output voltage of 1.503 V is caused by the imbalance between PM1 and PM2 (due to their unequal widths). The DC loop gain is around 80 dB, leading to an outstanding level of static regulation. The load regulation is only 0.046 mV/mA for a wide range of currents (from 0 mA to 30 mA). The line regulation is not observable, since the output swings uncontrollably; a sure sign that DC performance is insufficient.

2) PSRR:

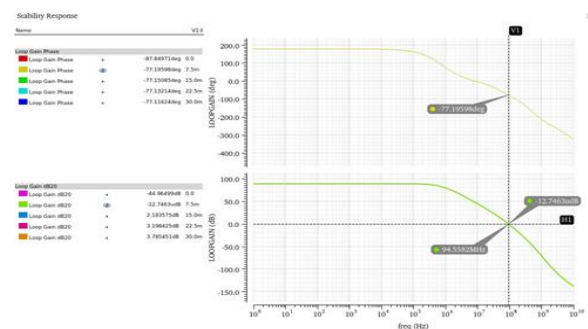
For a frequency range close to zero, the PSRR equals $-73.04\ \text{dB}$, agreeing with the large DC gain. In contrast, due to no compensation, the PSRR shows significant peaking behavior (the highest gain being $-3.43\ \text{dB}$ at 63 MHz).

3) AC Stability

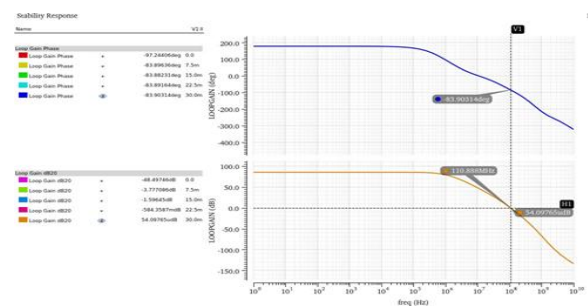
Oscillation at All Loads: The Bode diagrams for the loop gain at three values of load currents, 0 mA, 7.5 mA, and 30 mA, are shown in Fig. 4. For a load current of 0 mA, the UGBW is found to be 10 MHz while the phase margin turns out to be negative, that is, -6.2° . In this case, the loop gain and the unity gain frequency increase as the load current increases since the transconductance of the pass transistor increases. Thus, the value of the unity gain frequency becomes 94.55 MHz and 110.8 MHz at load currents of 7.5 mA and 30 mA, respectively. However, the phase margin continues to become more and more negative; it is -77.2° and -83.9° , respectively.



(a) 0 mA: PM = -6.2° , UGBW = 10 MHz



(b) 7.5 mA: PM = -77.2° , UGBW = 94.55 MHz



(c) 30 mA: PM = -83.9° , UGBW = 110.8 MHz

Fig. 4: Normal LDO loop gain Bode plots at three load currents. The phase margin is negative across the entire load range, confirming sustained oscillation.

B. Miller-Compensated LDO Results

1) DC and Regulation:

For the Miller LDO, $V_{OUT} = 1.548$ V and $I_{OUT} = 10.24$ mA, same results as for the normal LDO. Line regulation is 0.84 mV/V between $V_{DD} = 1.75$ to 3.3 V, while load regulation is 16.8 μ V/mA from 0 to 30 mA. Both are very good numbers and satisfy power management requirements.

2) AC Stability - Phase Margin Load Dependent:

From Fig. 5, at an output current of 7.5 mA, the phase margin obtained from the Bode plot is 46.48° while $UGBW = 22.43$ MHz. The stability is well maintained for the circuit with great damping. For 30 mA, there is a reduction in phase margin to 44.85°, although $UGBW$ increases to 32.01 MHz; the result is acceptable.

But for the case of zero output current, there is further reduction in phase margin to 6.08° and $UGBW = 1.02$ MHz. As observed previously, the reason behind this behavior is that of the load dependency of the Miller compensated LDO; at zero load, the output resistance of the pass transistor

3) PSRR – The Miller Hump:

Low-frequency PSRR is -73 dB, which is possible due to high DC gain. But the presence of feedforward through C_c , in Miller compensation, deteriorates PSRR at medium frequencies.

As seen from Fig. 6, there is a hump at 25.12 MHz with a very low PSRR of just -13.2 dB. Beyond that point, the load capacitor, C_L , becomes dominant, resulting in a PSRR of -43.7 dB at 1 GHz.

This hump is inherent to Miller compensation and may lead to problems for systems that require good PSRR in 10-100 MHz.

4) Transient Response – Slew-Rate Limitation:

A step change in the load current from 5 mA to 30 mA (Fig. 7) results in significant fluctuations in the output voltage: undershoot up to ≈ 0 V and overshoot up to ≈ 2.4 V.

The constant tail current of 120 μ A can neither charge nor discharge the 27 pF Miller capacitor in sufficient time. From the slew rate formula $SR = I_{tail}/C_c = 120 \mu A/2$

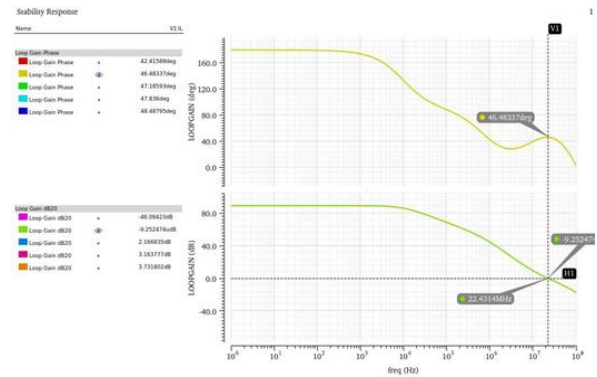


Fig. 5: Miller LDO loop gain at 7.5 mA load (phase margin 46.48°).

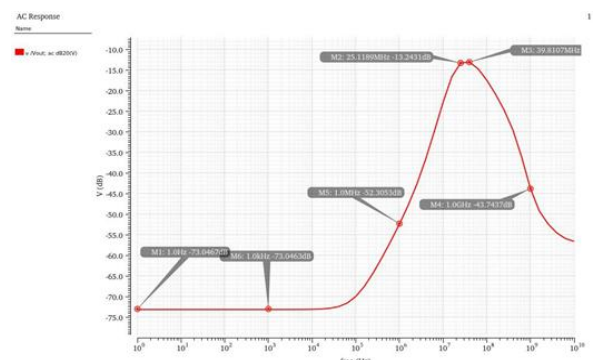


Fig. 6: Miller LDO PSRR vs. frequency. Note the hump at 25 MHz (-13.2 dB).

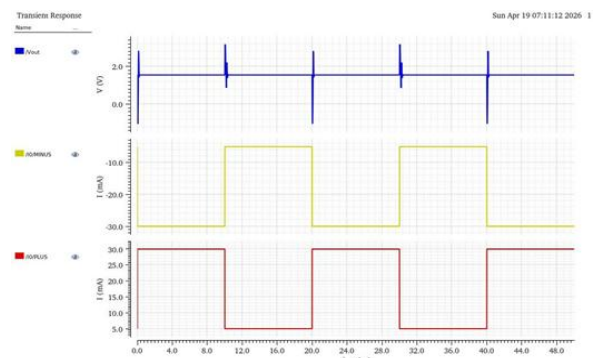


Fig. 7: Miller LDO transient response to a 5–30 mA load step. Output swings from 0 V to 2.4 V.

C. Adaptive LDO Results

1)DC Performance – Excellent:

The adaptive LDO provides $V_{OUT} = 1.208$ V (0.67% error from 1.2 V), line regulation 1.3 mV/V, load regulation 0.042 mV/mA, and dropout voltage 150 mV for the target 50 mA. Such specifications make the proposed design comparable to state-of-the-art LDOs due to high DC gain (> 60 dB) of the folded cascode circuit and low on-resistance of the pass transistor.

2)AC Stability - Unconditionally Stable with External Capacitor Connection:

When using an external capacitor of $4.7 \mu\text{F}$, the main pole of the amplifier shifts down to the value of 100 Hz. The Bode diagram (Fig. 8) indicates that the gain has a DC value of 48 dB, the frequency with unity gain is 4.09 kHz, and a phase margin of 90.6° . Phase stays at the level of 90° till 1 MHz. It means that all the parasitic poles of internal cascode and buffer stages have their values above 100 MHz when the loop gain is below -80 dB . So, our circuit is unconditionally stable, but the bandwidth is very low (5000 times lower than the Miller LDO).

3)PSRR – Low-Frequency Performance Weakness, High-Frequency Performance Strength:

As seen in Fig. 9, two distinct frequency ranges are apparent here. However, above 1 MHz, the large $4.7 \mu\text{F}$ capacitor provides passive filtering, improving PSRR to -62.32 dB at 1 MHz (marker M2) and beyond -100 dB at higher frequencies. This profile makes the adaptive LDO suitable for powering high-frequency digital loads (e.g., FPGAs) where low-frequency noise is not a concern.

4)Large-Signal Transient Failure – Catastrophic Collapse:

A load step from 1 mA to 50 mA (Fig. 10) causes a linear collapse of the output voltage from 1.21 V to 0.88 V over $40 \mu\text{s}$. Applying the capacitor discharge equation:

$$I_{\text{cap}} = C_L \frac{\Delta V}{\Delta t} = 4.7 \mu\text{F} \cdot \frac{0.33 \text{ V}}{40 \mu\text{s}} = 38.78 \text{ mA} \quad (5)$$

the LDO itself supplies only $50 - 38.78 = 11.22 \text{ mA}$ – just 22% of the target. The pass-transistor gate voltage never falls below 1.15 V (initial 1.35 V), confirming that the buffer cannot drive the gate sufficiently low.

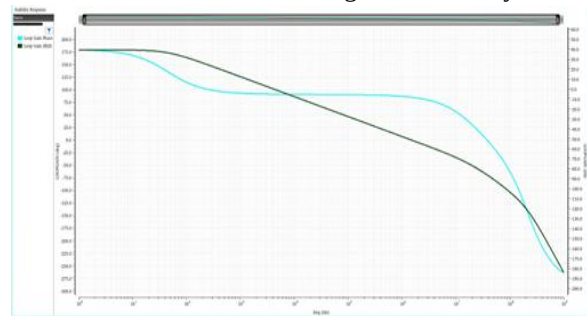


Fig. 8: Adaptive LDO Bode plot with $C_L = 4.7 \mu\text{F}$ (PM 90.6° at 4.09 kHz).

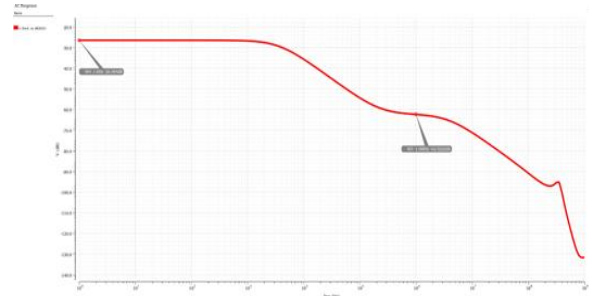


Fig. 9: Adaptive LDO PSRR vs. frequency. M1: -26.38 dB , M2: -62.32 dB at 1 MHz.

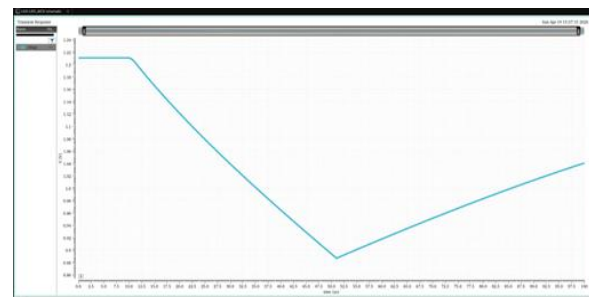


Fig. 10: Adaptive LDO transient response to a 1–50 mA load step. Output collapses linearly.

5)Fault Detection – Differential Contention:

In such an error amplifier design, there are two outputs that define how the pull-up PM8 and pull-down NM6 transistors operate in the Class AB circuit. If the output voltage is less than a certain threshold voltage, then the current flowing in the NM6 transistor increases, while the current flowing through the PM8 decreases. In PMOS transistor, decreasing the bias current means that the value of V_{GS} becomes more negative for some constant drain-source voltage, hence the transistor conducts heavily. So, both NM6 and PM8 transistors become active, hence keep their gates at some mid-value (1.15 V). Thus, no further current flows from the pass transistor, and the output drops.

This fault may be detected by a large signal simulation since AC model simulation does not consider the non-linear parts of the feedback system, and uses the small-signal model with proper differential-to-single-ended conversion. The proper conversion with the correct current-mirror load should get rid of contending states.

D. Design Trade-offs and Lessons Learned

Table III consolidates all key metrics. From this study, we extract the following design guidelines:

1. Buffer stages must have single-ended OTA outputs. A fold cascode amplifier should be loaded by a current mirror stage before being used in the Class AB operation.
2. Use of non-inverting buffers (source follower circuits) simplifies the design. It helps us not encounter the issue of inversion due to the use of an inverted signal for Miller compensation.
3. Transient analysis is inevitable. All parameters, including DC gain, phase margin, and power supply rejection ratio, may seem perfect; yet they may completely collapse with a load change.
4. External compensation leads to a stable circuit but with narrow bandwidth. The UGBW of 4.09 kHz of an adaptive LDO can be acceptable for very slow loading currents. Any high-speed LDO will require an internally compensated approach.
5. LDO circuits with Miller compensation need a minimum load. The value of the phase margin at no load of 6.08° in Design 2 is too poor even with the presence of a bleeder resistor.

TABLE III: Comparative performance summary (Cadence Spectre results)

Parameter	Normal LDO	Miller LDO	Adaptive LDO
Process / V_{DD}	180nm / 3.3V	180nm / 3.3V	180nm / 1.8V
Target load	30 mA	30 mA	50 mA
Actual max load	30 mA (unstable)	30 mA (met)	11.2 mA (failure)
Phase margin	-6.2° to -83.9°	46.5° – 39°	90.6° (4.7 μ F)
Unity-gain freq.	10–110.8 MHz	22.43 MHz	4.09 kHz
PSRR @ 1 kHz	–73.04 dB	–73 dB	–26.38 dB
PSRR hump	Severe peaking	–13.2 dB@25 MHz	None
High-freq PSRR	–3.43 dB@63 MHz	–43.7 dB@1 GHz	–62.32 dB@1 MHz
Transient response	Unstable	Spikes (0–2.4V)	Collapse
Dropout voltage	≈ 50 mV	1.75 V	150 mV

V. CONCLUSION

There were proposed three variants of LDO circuit design. Normal LDO design possesses the highest value of DC gain (≈ 80 dB), but cannot be used as a voltage regulator because of oscillations for any output current. Application of Miller compensation ($C_c = 27$ pF, $R_z = 820 \Omega$) allows getting stability again, but results in obtaining a working 30 mA voltage regulator with decent properties of line/load regulation and low-frequency PSRR.

The price for that is the limited range of transient response spikes (0–2.4 V) and extremely poor value of phase margin of 6.08° at no-load condition. Adaptive LDO design features a high phase margin (90.6°) and excellent high-frequency PSRR (-62.3 dB) at 1 MHz, but fails completely when load changes from 1 to 50 mA, providing 11.2 mA current as result.

The reasons for failure found based on the capacitor discharge equation, are related to differential-to-single-ended signal conversion conflict problem – effect which is impossible to be considered by means of traditional small signal AC model.

VI. FUTURE SCOPE

The adaptive LDO can be corrected by the following modifications:

1. Replace the folded cascode with a two-stage op-amp having a current-mirror active load. This provides a single-ended output that can properly drive the Class-AB buffer without contention.
2. Use a non-inverting buffer such as a source follower or a super source follower. This would make the overall feedback loop inverting, re-enabling Miller compensation.
3. Add transient detection circuitry – a comparator-based slew booster that injects extra current during large load steps [6].
4. Optimise pass-transistor sizing – a slightly smaller device ($W = 600 \mu\text{m}$) might reduce C_{gg} enough to allow internal compensation while still meeting dropout.

A revised schematic incorporating these changes is planned for future simulation and, if successful, for tape out in the same 180 nm process.

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