Design And Analysis of Conventional Vs Junctionless Finfets for Low-Power Applications

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***Abstract*—Conventional FinFETs face difficulties with short- channel effects and variability as device scaling approaches 14nm technology. With a uniformly doped channel, junction less FinFETs provide an alternative method that provides better electrostatic control. In this work, TCAD simulations are used to compare junction-based and junction less FinFETs. Transfer Characteristics are used to assess electrical properties such as I_{on} ($2.228e^{-5}$), I_{off} ($6.445e^{-12}$), I_{on}/I_{off} ($3.46e^{6}$), subthreshold slope (80.808) and threshold voltage (0.418) for junction-based finfet as well as for junction less finfet the I_{on} ($1.748e^{-8}$), I_{off} ($1.540e^{-8}$) , I_{on}/I_{off} (1.13), subthreshold slope (14030.6) and threshold voltage (0.527) and also electrostatic analyses such as electric field, potential distribution and mobility provide support. Performance metrics are extracted, including I_{on}/I_{off} ratio, subthreshold slope, and threshold voltage. The analysis show that while junction-based devices provide higher drive current, junction less FinFETs have smoother potential profiles and fewer short-channel effects. These results show that while conventional FinFETs provide higher drive current, junction less devices exhibit better electrostatic integrity and lower short- channel effects, making them more suitable for leakage-sensitive and ultra- low-power nanoscale applications.**

I. INTRODUCTION

The basic building blocks of modern integrated circuits have been Metal–Oxide-Semiconductor Field-Effect Transistors (MOSFETs) because of their simple design, scalability, and effective switching characteristics. The traditional planar MOSFETs have made it possible to continuously decrease the size of the device as per the Moore law, thus providing better performance and integration density. Nevertheless, planar MOSFETs are afflicted with atrocious short-channel effects, leakage currents, and loss of gate control over the channel, as the scale of the device dimensions approaches the deep nanometer. These constraints have a major effect on the reliability of devices and power consumption, especially in low-power devices, and require the design of superior transistor architectures beyond conventional planar designs [13], [14].

FinFET (Fin Field-Effect Transistor) technology's improved electrostatic control and scalability have made it a viable option for sophisticated nanoscale devices [10], [6]. FinFETs offer improved gate control by eliminating short-channel effects and enhancing switching characteristics through the use of a three-dimensional fin-shaped channel structure.

However, issues such as leakage current, variability, and short-channel effects become important as device dimensions get closer to the 14 nm technology and even lower [5], [11]. These difficulties are crucial in low-power applications, where energy efficient operations depend on reducing leakage and enhancing electrostatic control. However, the need for abrupt source-drain connections limits these benefits in conventional junction-based FinFETs. Exact doping methods are required, which add unpredictability and complicate production. Furthermore, leakage behavior and short-channel effects are caused by large electric field peaks due to steep doping gradients. Hence, Junctionless FinFET as a new alternative architecture to minimize these limitations [17], [18]. Using a uniformly doped channel removes the need for abrupt junction formation saving in fabrication and random dopant fluctuations. It therefore leads to smoother potential profiles and improved electrostatic integrity that are favorable for suppressing short-channel effects. But this paid off more voltage drop (drive current) with the risk of remains mobility degradation. This paper employs Technology Computer-Aided Design (TCAD) simulations to explore the design trade-offs between junction-based and junctionless FinFETs at the 14 nm technology node, and with low-

power applications in mind [6], [16]. Electrical and electrostatic (parameters) characterizations are considered to know the workings of a device. The threshold voltage, subthreshold slope, drain-induced barrier lowering, and I_{on}/I_{off} ratio are the key performance measures that are extracted to evaluate switching and leakage properties [9], [12]. This research offers information on how to choose the appropriate FinFET design to design nanoscale transistors that are energy efficient.

II. DEVICE STRUCTURE

A. Conventional FinFET

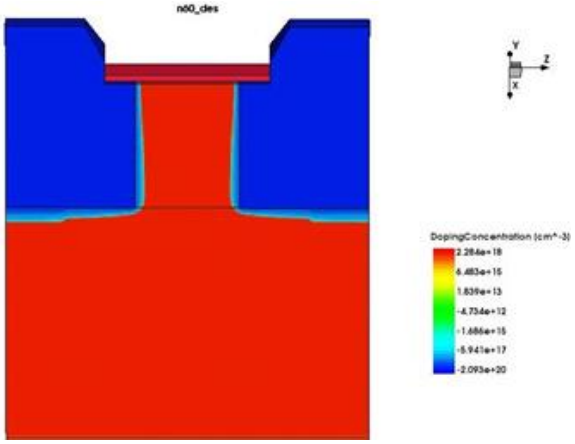

Fig. 1. 3D Structure of NMOS junction-based FinFET

Fig. 1 illustrates a standard junction-based FinFET, a tri- gate device in which the silicon channel is fin-shaped (channel length = 25 nm, fin height = 35 nm, fin width = 15 nm) and surrounded on three sides by the gate, providing strong electrostatic control [13], [10]. The channel is heavily doped (2×10^{20} cm^{-3}), while the source and drain regions are heavily doped (1×10^{20} cm^{-3}) using SiGe and SiC respectively, forming abruption junctions at the interfaces [5], [11]. A high-*k* dielectric such as HfO_2 (thickness = 1.2 nm) is used as the gate oxide to enhance gate capacitance and reduce leakage current. A tungsten gate metal (thickness = 5 nm) is employed to ensure proper work function alignment. The silicon substrate is moderately doped (1×10^{16} cm^{-3}) with a thickness of 50 nm. When the applied gate voltage exceeds the threshold voltage, an inversion layer forms, enabling carrier transport between the source and drain. Abrupt junctions introduce fabrication complexity and high electric field gradients, though they are essential for device operation [2], [4].

In Fig.2 a junctionless FinFET shows the channel, source and drain share a uniform doping profile of the same type and concentration, thus eliminating pn junctions. The device retains the same structural dimensions (L = 25 nm, H = 35 nm, W = 15 nm) and material composition (silicon channel on silicon substrate with HfO_2 high-*k* dielectric of thickness ~1.7 nm). The uniformly doped channel operates in depletion mode, where at zero gate bias the channel is fully depleted, preventing current flow. As the gate voltage increases, the depletion region reduces and conduction begins. The tri-gate architecture and high-*k* dielectric remain consistent with conventional FinFETs; however, the absence of abrupt junctions simplifies fabrication, reduces variability, and results in a smoother electrostatic potential distribution within the device. Based on Fig. 1 and Fig. 2, the main difference between junction-based and junctionless FinFETs are in their doping profile and mode of operation. Junction-based devices are based on inversion and abruption junctions, which lead to

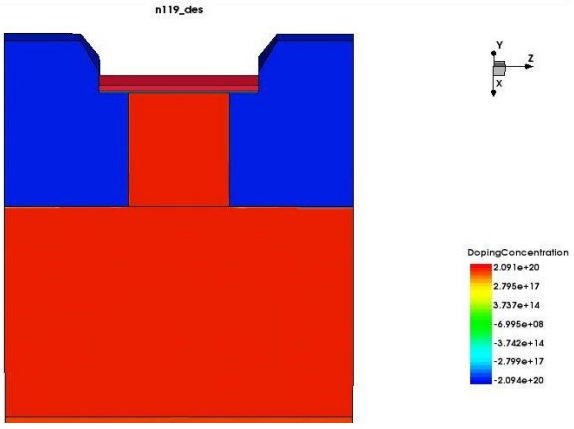

Fig. 2. 3D Structure of NMOS Junctionless FinFET

higher drive current, yet higher electric field peaks and variability. Junctionless devices, by contrast, are based on bulk conduction and do not have doping gradients, which results in smoother potential profiles and better electrostatic control. Such structural variations are very important in the leakage behavior and short channel effects and as such they play a significant role in determining the suitability of a device in low-power applications.

B. Device Parameters

TABLE I Device Parameters

Parameter	Doping (cm−3)	Material	Length/Thickness (nm)
Channel Length	2 × 1020	Silicon	25
Fin Height	–	Silicon	35
Fin Width	–	Silicon	15
Source	1 × 1020	SiGe	20
Drain	1 × 1020	SiC	20
Gate Oxide	–	HfO2	1.2
Gate Metal	–	Tungsten	5
Substrate	1 × 1016	Silicon	50

Table I shows the most significant device parameters that were utilized in the sentarous TCAD simulation, such as doping concentrations, the choice of the material, as well as the structural dimensions (such as channel length, fin width, and oxide thickness). The parameters are selected to depict realistic conditions of 14 nm technology nodes. The content of the doping and the material make a direct impact on the carrier transport, electrostatic control, and leakage behavior. Therefore, the parameter set as identified in Table I is crucial in shaping the overall performance and low-power of the FinFET devices.

III. DEVICE PERFORMANCE METRICS

A. Drain Current (I_d)

Drain current represents the current flow from drain to source and determines device drive capability.

$$I_d = 2\mu C_{ox} \frac{W_{eff}}{L} (V_{th})^2 \Delta Q_i \quad (1)$$

B. Leakage Current (I_{off})

Leakage current is the current flowing when the device is OFF ($V_g < V_{th}$).

$$I_{OFF} = I_0 e^{\frac{V_g - V_{th}}{nV_T}} \quad (2)$$

C. I_{on}/I_{off} Ratio

$$\frac{I_{on}}{I_{off}} \quad (3)$$

Switching efficiency is determined with this ratio.

D. Subthreshold Slope (SS)

$$SS = \left(\frac{\partial \log I_d}{\partial V_g} \right)^{-1} = \frac{\partial V_g}{\partial \log I_d} \quad (4)$$

Sharpness of the device switching from OFF to ON is indicated by SS.

E. Transconductance (g_m)

$$g_m = \left. \frac{\partial I_d}{\partial V_g} \right|_{V_d} = \text{constant} \quad (5)$$

Gate control over channel current is reflected by transconductance.

IV. RESULTS AND DISCUSSION

Electrical characteristics and electrostatic behavior obtained from TCAD simulations are used to analyze the performance of junction-based and junctionless FinFETs. The results are discussed with a focus on understanding device operation and evaluating their suitability for low-power applications [5], [11].

A. $I_d - V_g$ Characteristics

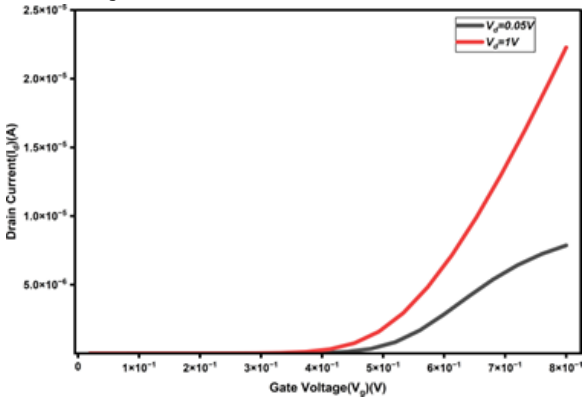

Fig. 3. Linear scale $I_d - V_g$ characteristics of Junction-based FinFET

In Fig. 3, the $I_d - V_g$ curve of the junction-based nMOS FinFET depicts a distinct threshold behavior, with the current flowing in the drain being low at lower gate voltages and rising exponentially above the threshold point. The difference between V_d = 0.05V and V_d = 1 V shows that there is ob- servable drain-induced barrier lowering (DIBL) and the sharp increase in current indicates good gate control of the channel and high inversion. The junction-based

device logarithmic

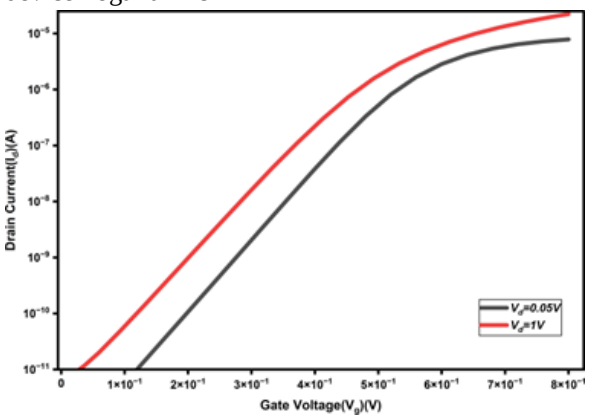

Fig. 4. Log scale $I_d - V_g$ characteristics of Junction-based FinFET

$I_d - V_g$ plot in Fig. 4 better indicates the subthreshold area with exponential growth in the drain current as the gate voltage changes. The gradient of the slope in this area is used to determine the subthreshold swing and the transition between curves at varying drain biases further establishes the short- channel effects. Fig. 5 shows that the $I_d - V_g$ characteristics of

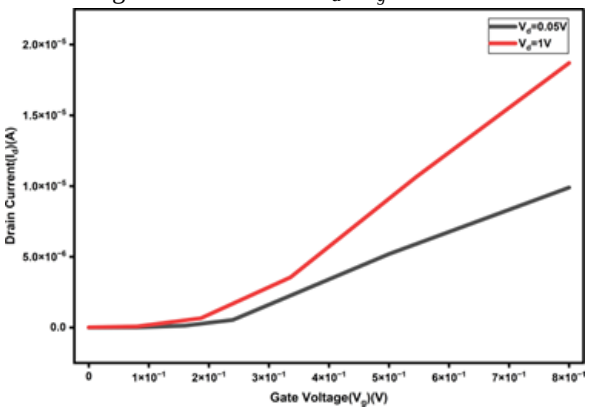

Fig. 5. Linear scale $I_d - V_g$ characteristics of Junctionless FinFET

the junctionless nMOS FinFET have a more gradual transition between the OFF to ON state, and the current at the lower gate voltages is relatively higher, owing to the lack of a junction barrier. This behavior implies better carrier movement and less scattering resulting in better current drive than the junction-based counterpart. Fig. 6 shows that the logarithmic plot of I_d vs. V_g of the junctionless device has a smoother subthreshold slope [17], [18] and a relatively larger leakage current. The lower steepness implies a compromise between the electrostatic control and ON-current, and the smaller change in the drain biases implies that the DIBL is relatively less, which emphasizes the benefits of junctionless architecture in scaled devices.

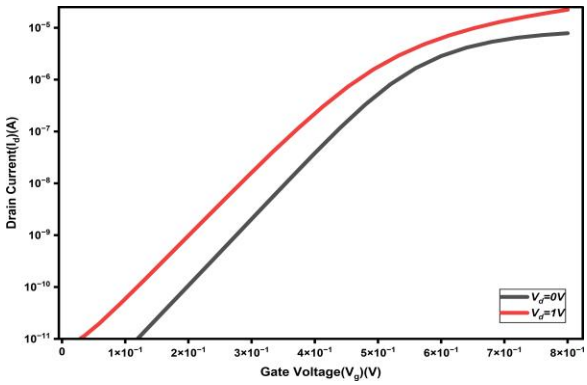

Fig. 6. Log scale $I_d - V_g$ characteristics of Junctionless FinFET

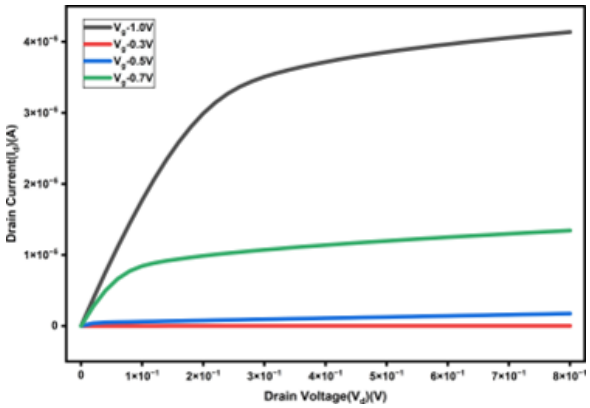

Fig. 7. $I_d - V_d$ characteristics of Junction-based FinFET

B. $I_d - V_d$ Characteristics

In Fig. 7, the output characteristic of the junction-based nMOS FinFET exhibits a typical tendency with the drain current increasing [7] with the drain voltage and ultimately leveling off with more V_d at the higher gate biases. It has distinct linear and saturation curves, where the larger gate voltages (V_g = 1.0 V) result in much larger drain currents be- cause of increased channel inversion. The saturation behavior is a good measure of pinch-off around drain, and the distance between curves is a good measure of gate control of channel conduction.

According to Fig. 8 the junctionless nMOS FinFET exhibits a very different $I_d - V_d$ characteristic, with bulk channel depletion controlling current conduction, but not junction formation. The drain current rises more quickly at lower V_d, and saturates sooner, especially

at higher gate voltages [6], which implies lower channel resistance and improved carrier transport. Also, the fact that noticeable current can be found at lower or negative gate biases implies a normally-on behavior, which is typical of junctionless devices [17]. This action illuminates the enhanced electrostatic control and decreased series resistance, and therefore the junctionless structure is beneficial to high- drive and low-power requirements.

C. Electrostatic Analysis

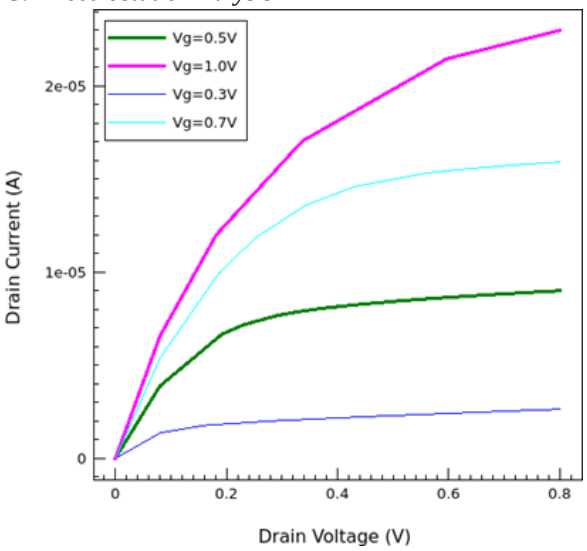

Fig. 8. $I_d - V_d$ characteristics of Junctionless FinFET

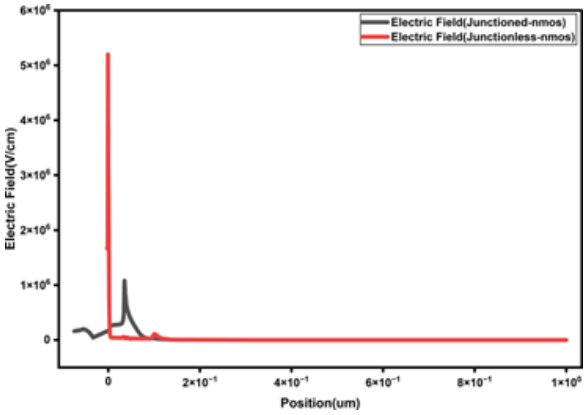

Fig. 9. Electric field in junction-based and junctionless Finfet

1) Electric Field Analysis:

Sharp electric field distribution of junction-based and junctionless nMOS devices is shown in Fig. 9. In the junctionless nMOS, a sharp peak in the electric field [5] is observed near the drain region, with a maximum value of approximately 5.2×10^6 V/cm, while the minimum value remains close to 0 V/cm along most parts of the channel. On the other hand, the junction-based nMOS has a relatively lower peak electric field of approximately, $\times 10^6$ V/cm with the lowest value also approaching zero. The much greater peak in the junctionless device would signify an enhanced focus of the electric field, whilst the junction- based device would reveal a more diffused and balanced field profile throughout the channel. This variability highlights that the junctionless design possesses more localized electric fields, which may increase carrier injection, but also may be reliably problematic such as the hot carrier effects [11]. In the meantime, the less jagged field distribution in the junction- based device is indicative of more controlled electrostatics, but with a lower carrier acceleration, highlighting the tradeoff between performance and reliability [2], [4].

2) Electron Mobility Analysis:

In Fig. 10 The electron mobility distribution indicates that in the case of the junction-based nMOS, the mobility lies between a minimum of around 0 $cm^2/V{\cdot}s$ and a maximum of about 1.35×10^3 $cm^2/V{\cdot}s$, whereas in the case of junctionless nMOS, the mobility lies between a minimum of 0 $cm^2/V{\cdot}s$ and a maximum of about1.32×10^3 $cm^2/V{\cdot}s$. The electron mobility distribution in the channel of junction-based and junctionless nMOS FinFETs increase sharply along the source-to-channel transition [8] and then remains nearly constant across the channel. The junction-based structure has a rather high peak mobility than the junctionless structure, which implies a relatively low impurity scattering [12] in the region of inversion. The junctionless de- vice, although exhibiting slightly lower mobility, has a more uniform profile along the channel, because of its uniformly doped structure. This implies that even though junctionless FinFETs can have higher impurity scattering, they have stable carrier transport [6], which helps to maintain stable current conduction and enhanced scalability of devices.

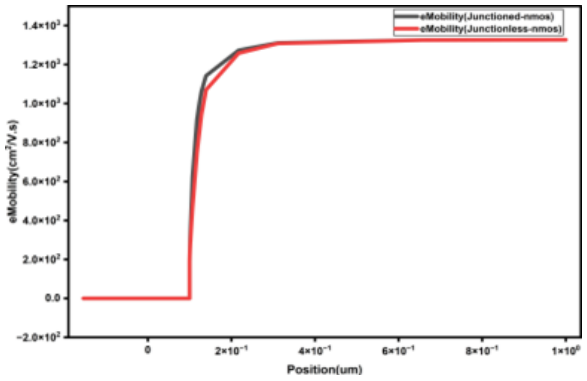

Fig. 10. Electric mobility in junction-based and junctionless Finfet

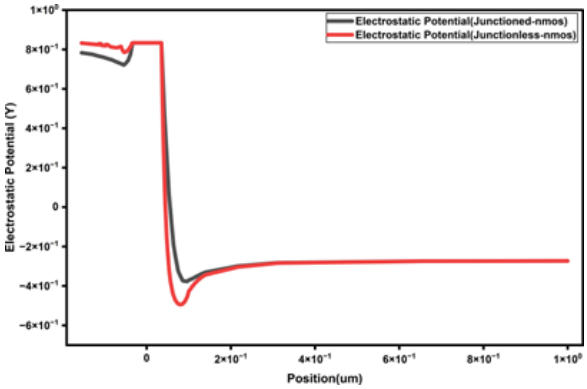

Fig. 11. Electrostatic Potential in junction-based and junctionless Finfet

3) Electrostatic Potential Analysis:

In Fig. 11, the dis- tribution of electrostatic potential shows that the field in the junction-based nMOS is between a minimum of about -4×10^{-1}V/cm and a maximum of about 7.9×10^{-1} V/cm, and in the junctionless nMOS is between a minimum of about -5.5×10^{-1}V/cm and a maximum of about 8.2×10^{-1} V/cm. The channels of both junction-based and junctionless nMOS FinFETs indicate a steep drop in the potential at the source channel junction, then a smooth change towards the drain. The junction-based device has a comparatively less rugged potential transition, reflecting a controlled formation of barriers [6] as a consequence of having source/drain junctions. Conversely, the junctionless device exhibits a steeper potential drop and a deeper minimum in the region around the channel which is a sign of greater gate control and complete depletion behaviour[17], [18]. This sharpening potential profile is better carrier transport, but implies increased coupling of the electric fields. All in all, the junctionless structure exhibits a better electrostatic control, which proves advantageous in scaling of the device and performance optimization.

TABLE II Device Performance Comparison

Parameter	Junction-based NMOS	Junctionless NMOS
(I_{on}) (A)	2.228e-5	1.748e-8
(I_{off}) (A)	6.445e-12	1.540e-8
(I_{on}/I_{off})	3.46e3	1.13
SS (mV/dec)	80.808	14030.6
(g_m) (S)	3.262e-5	1.347e-10
(V_{th}) (V)	0.418	0.527

A comparative analysis of the performance of junction- based and junctionless FinFETs of the nMOS and pMOS structure in terms of important parameters of the device is provided in Table 2. It can be seen in Table 2 that the ratios of junction- based devices show much higher values, largely because their leakage current (I_off) is much lower, which means that they are much more efficient in switching and they have a better OFF-state control. Junctionless devices, on the contrary, exhibit greater and therefore lower the ratio, a trade-off between complexity of structure and leakage. In addition, Table 2 notes that junction-based devices have reduced subthreshold swing (SS) and increased transconductance (g_m), which imply more precise switching properties and enhanced gating [10]. The values of threshold voltage (V_{th}), as well, are more favorable in junction-based devices whereas junctionless devices have relatively high and poorer SS because of uniform channel doping. Junction-based FinFETs exhibit superior electrical properties with respect to leakage, switching characteristics, and electrostatic control, though the junctionless FinFETs have structural benefits.

V. CONCLUSION

This paper provides a comparative study of 14nm junction based and junctionless FinFETs based on TCAD simulation in terms of their electrical and electrostatic characteristics.

The findings reveal that the junction-based nMOS has a much greater drive current, i.e., $I_{on} = 2.228 \times 10^{-5}$ A, than the junctionless device, which is almost three orders of magnitude larger. This is mostly enhanced

by the existence of abrupt source/drain junctions which can inject powerful carriers.

This again shows that the Ion/Ioff ratio of the junction-based device (3.46×106) is significantly greater than the junctionless one (1.13), and the junction-based device has better switching efficiency. This is also corroborated by the subthreshold slope, with the junction-based FinFET being able to reach to the subthreshold slope of 80.808 mV/dec in contrast to a much degraded 1403.06 mV/dec in the junctionless device, which demonstrates weaker gate control in the uniformly doped channel.When it comes to leakage characteristics the junctionless FinFET has a higher off-current $I_{off} = 1.540 \times 10^{-8}$ A than the junction-based device (6.445×10^{-12} A), and can be explained by the lack of junction barriers, which can still conduct (even in the OFF state). There is also a large variation in transconductance, with the junction-based device having a transconductance of 3.262×10^{-5} S versus 1.347×10^{-10} S in the junctionless device, which means better gate control and higher gain. Also, the increased threshold voltage of the junctionless device (0.527 V compared to 0.418 V) is an indication of the extra gate bias that is needed to completely deplete the channel that is highly doped before switching. Comprehensively, junction-based FinFETs are better in terms of drive strength, switching performance, and gain and junctionless FinFETs are simpler structurally and have unique electrostatic properties, demonstrating an inherent trade-off between performance and device structure.

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