Design And Implementation of a Power-Efficient Synchronous Dual-Port Memory Using Synthesis-Based Clock Gating and Pipelining

Mrs. R. N. S. Kalpana[1], K. Keerthan[2], P. Vamshi[3], Md. Mujtaba[4], M. Yoga Yashwanth[5]
[1]*Assistant Professor, Dept. of ECE, TKR College of Engineering and Technology*
[2,3,4,5]*Student, Dept. of ECE, TKR College of Engineering and Technology*

***Abstract*—This paper presents the design and implementation of a power-efficient synchronous dual-port memory using pipelined architecture and synthesis-based clock gating techniques. Conventional dual-port memory designs often result in high power consumption due to unnecessary switching activity and continuous clock operation. To overcome these limitations, the proposed design uses enable-controlled clock gating and optimized pipelined data transfer, thereby reducing dynamic power and improving efficiency. The architecture supports simultaneous read and write operations with effective conflict handling using priority-based access control. The memory is modeled using Verilog HDL and implemented using FPGA design tools such as Xilinx Vivado.**

***Index Terms*—Dual-Port RAM, Clock Gating, Pipelining, Verilog HDL, FPGA, Vivado, Low-Power Design.**

I. INTRODUCTION

Memory systems are central to digital design because they store and provide quick access to instructions and data during system operation. In modern VLSI and FPGA-based systems, the demand for fast and simultaneous memory access has increased due to applications such as digital signal processing, image processing, communication systems, and multi-core computing. Traditional single-port memories are simple and power-efficient, but they can perform only one read or write operation in a clock cycle, which limits throughput in parallel systems.

To overcome this limitation, dual-port memories are used because they allow two independent accesses to memory at the same time. However, many conventional dual-port memory architectures rely on asynchronous operation or separate clock domains, which can create timing uncertainty, higher switching activity, and greater power consumption. The present work proposes a synchronous dual-port RAM with a single clock domain, synthesis-based clock gating, and pipelined read operation to achieve better timing predictability and lower dynamic power dissipation.

The proposed design also includes conflict-resolution logic and a port-locking feature. When both ports attempt simultaneous writes to the same address, Port 1 is given priority to maintain deterministic operation and avoid memory corruption. When parallel access is not required, the design can operate in a single-port mode, improving flexibility and helping reduce unnecessary activity. This combination of synchronous operation, gated clocking, and structured RTL design makes the memory suitable for low-power and high-performance digital systems.

II. METHODOLOGY

The methodology of the proposed work begins with the analysis of an existing synchronous dual-port memory architecture to identify sources of power consumption, timing bottlenecks, and access conflicts. Based on this analysis, two major optimization methods are introduced: synthesis-based clock gating and pipelining. Clock gating is used to disable the clock signal when memory activity is not needed, thereby reducing dynamic power loss due to unnecessary switching.

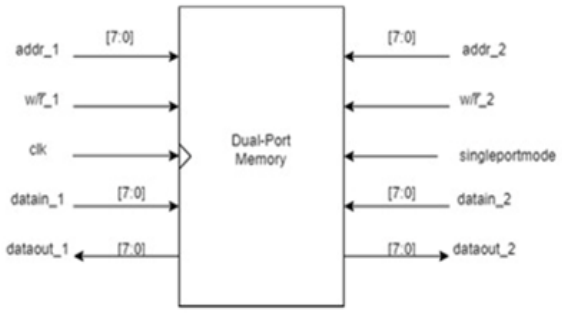

Fig. 1. Block Diagram of DP-memory

In the proposed design, a gated clock is generated from the global clock signal clk and an enable signal en. The synthesis-based clock gating method uses a negative latch and logic gating so that glitches are avoided and the generated clock remains synchronized with the original clock domain. This method ensures that memory operations occur only when required, which helps reduce power dissipation without affecting functional correctness

Table 1: OPERATIONS ON PORT 1 AND PORT 2

Port 1	Port 2	Condition	Operation
Write	Read	Address1=Address2 Or Address1≠Address2	Write data from Port 1 to Address 1 and read from Address 2 through port 2
Read	Write	Address1=Address2 Or Address1≠Address2	Write data from Port 2 to Address 2 and read from Address 1 through port 1
Read	Read	Address1=Address2Or Address1≠Address2	Read from Address 1 through Port 1 and read from Address 2 through Port 2
Write	Write	Address1≠Address2	Write data from Port 1 to Address 1 and write data from Port 2 to Address 2
Write	Write	Address1=Address2	Write data from Port 1 to Address 1 and drop data at Port 2

Table 1 presents the operating conditions and functional behavior of the proposed synchronous dual-port memory for different combinations of Port 1 and Port 2 access modes. The memory supports simultaneous read and write operations through two independent ports while ensuring reliable conflict management.

In the first case, Port 1 performs a write operation while Port 2 performs a read operation. Whether the addresses are same or different, data is written through Port 1 to Address 1, while Port 2 reads data from Address 2. This enables concurrent write-read functionality without interrupting either port.

In the second case, Port 1 is configured for reading and Port 2 for writing. Under both same-address and different-address conditions, Port 2 writes data to Address 2 while Port 1 reads from Address 1. This demonstrates bidirectional dual-port access capability.

The third case represents simultaneous read operations from both ports. When both ports are in read mode, each port independently reads data from its respective address. If both addresses are equal, the same memory location is accessed by both ports concurrently.

The fourth case illustrates simultaneous write operations to different addresses. Port 1 writes data to Address 1, while Port 2 writes data to Address 2 at the same clock cycle. Since the addresses are different, both write operations are completed successfully.

The fifth case considers simultaneous write attempts to the same address. In this condition, a memory access conflict occurs. According to the implemented priority-based arbitration scheme, Port 1 is given higher priority. Therefore, data from Port 1 is written successfully, while the write request from Port 2 is ignored.

III. IMPLEMENTED DESIGN

The implemented system consists of two major modules: a synthesis-based clock gating unit and a synchronous dual-port memory unit. The clock gating block receives the main clock and enable control, then produces a gated clock signal that activates the memory block only during valid operations. This reduces unnecessary toggling in idle periods and directly lowers dynamic power consumption.

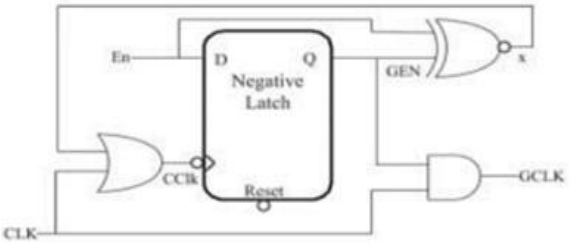

Fig.2 Synthesis based clock gating technique using negative latch

The memory block is developed as a 256 × 8-bit synchronous dual-port memory using Verilog HDL. It provides two independent ports, where each port has its own address bus, data input, data output, and write

enable control. This independent structure allows both ports to access memory simultaneously, making the design highly efficient for parallel data operations. The architecture is optimized for FPGA implementation so that available memory resources and logic elements are utilized effectively.

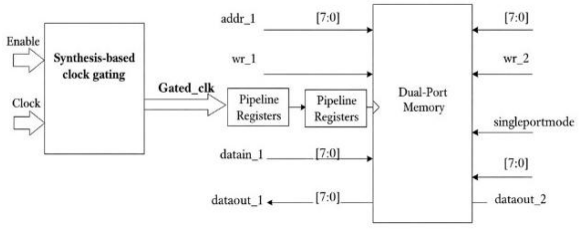

Fig.3. Block Diagram of Dual Port Memory with Gated clock

To ensure reliable operation during concurrent access conditions, controlled arbitration logic is incorporated into the design. When both ports attempt to write to the same memory address during the same clock cycle, Port 1 is assigned higher priority. This guarantees deterministic behavior and prevents data corruption. At the same time, the architecture fully supports simultaneous writes to different addresses as well as concurrent read operations from both ports.

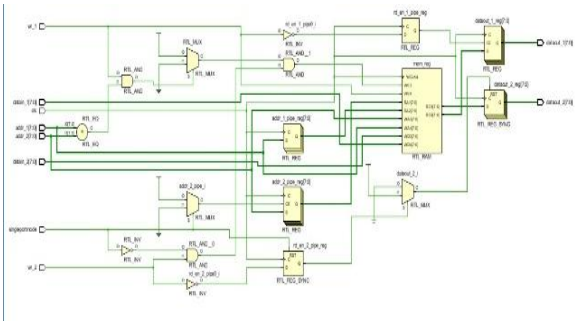

Fig.4 Schematic Diagram of Dual Port Memory with Gated Clock

A pipelined read mechanism is also introduced to improve timing performance. In this approach, addresses and control signals are first registered before the read data is delivered to the outputs. Although this adds a small latency of one clock cycle, it enables higher operating speed, improved timing closure, and more stable performance. Since the external interface of the memory remains unchanged, the proposed optimized architecture can directly replace conventional memory designs without requiring any changes to the surrounding system.

IV. RESULT AND DISCUSSION

The proposed memory was verified using behavioral and post-synthesis simulation in FPGA design environment. Multiple test cases were considered, including Port 1 write and Port 2 read, Port 2 write and Port 1 read, simultaneous reads, simultaneous writes to different addresses, simultaneous writes to the same address, and single-port mode operation. The simulation results confirmed correct functionality in all tested conditions.

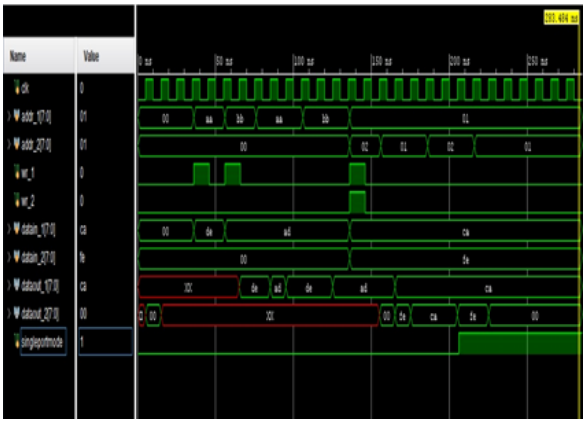

Fig. 5. Simulation Waveform of Dual Port Memory with Gated clock

The simulation waveform shows that the proposed synchronous dual-port memory system obtained during functional verification. The waveform presents the behavior of all major input and output signals, including the clock, address lines for both ports, write enable controls, input data buses, output data buses, and the single-port mode control signal. The results clearly demonstrate that the memory architecture performs reliable read and write operations under different operating condition

Table.2. Comparison table

Parameter	Dual Port Memory	Dual Port Memory With Synthesis Based Clock Gating
Area [LUT's]	14	15
Power [W]	16.789	0.458
Static Power[mW]	0.227	0.132
Delay[nS]	6.789	5.900
Net Delay	1.599	1.291
Logic Delay	5.189	4.609
Address Size	8	8
Data Size	8	8

Efficiency Scorecard

The results obtained from this project clearly show that the proposed memory design performs much

better than the conventional design. By introducing clock gating and architectural improvements, the system achieved lower power consumption, better speed, and only a very small increase in hardware resources.

Major Reduction in Power Consumption

The most noticeable improvement is the reduction in total power usage. This is nearly a 97% decrease in power consumption, which is a significant achievement. Lower power consumption means the circuit generates less heat and operates more efficiently. In real applications, this can improve battery life, reduce cooling requirements, and increase overall device reliability. This result confirms that the clock gating technique successfully reduced unnecessary switching activity when the memory was idle.

Faster Operation with Reduced Delay

In many cases, adding power-saving features can slow down a circuit. However, in this project, the opposite result was achieved. This shows that the optimized memory design became faster as well. Lower delay allows quicker data access and faster system response. It also means the memory can operate at a higher frequency, which is useful in high-speed digital systems. The reduction in both logic delay and net delay indicates that the internal data path was improved effectively.

Very Small Increase in Area

Every improvement in digital design usually comes with some hardware cost. In this case, the cost was minimal. Only one additional LUT was used. Using just one extra LUT to achieve such large power savings and improved speed is considered an excellent trade-off. The increase in area is very small compared to the benefits gained.

No Change in External Interface

Although internal changes were made to improve performance, the external memory interface remained the same. Since the interface did not change, the new memory can replace the previous design without modifying the rest of the system. This makes implementation easier and saves development time. The overall results prove that the proposed memory design is more efficient than the conventional design.

The project achieved a major reduction in power consumption by applying synthesis-based clock gating. The conventional dual-port memory consumed 16.789 W, while the optimized design consumed only 0.458 W, showing a significant improvement in energy efficiency. Lower power usage also reduces heat generation, improving system reliability and performance in compact high-speed applications.

In conventional circuits, the clock toggles continuously even when memory is idle, causing unnecessary dynamic power loss. To overcome this, the proposed design uses clock gating, where the clock becomes active only during valid memory operations. A negative latch is included in the gating logic to avoid glitches and maintain stable operation.

The optimized memory also demonstrated better timing performance. Logic delay was reduced from 5.189 ns to 4.609 ns through improved control logic and pipelined operation. This allows faster response and higher operating speed.

Area overhead remained minimal. The LUT count increased only from 14 to 15, which is negligible compared to the gains in power and speed. This provides a strong balance between power, timing, and area.

For simultaneous write conflicts, a priority-based mechanism was implemented where Port 1 is given higher priority than Port 2. Simulation confirmed reliable and predictable operation.

An additional security feature restricts Port 2 from writing to addresses 00h to 0Fh, protecting critical configuration and control data from accidental modification.

V CONCULSION

In conclusion, this project presents the design and implementation of an optimized dual-port memory using Verilog HDL. The objective was to develop a reliable memory system that supports simultaneous access through two ports while maintaining safe operation, predictable timing, and efficient hardware utilization. The architecture was implemented as a 256 × 8-bit memory using FPGA block RAM, which improves speed, reduces power consumption, and minimizes logic usage. The design combines synchronous memory concepts, pipelining, and arbitration to achieve high performance. Pipelined read operations introduce controlled latency while

enabling higher operating frequency and realistic synchronous memory behavior. Both ports can perform read and write operations simultaneously without data corruption. To prevent conflicts during simultaneous writes to the same address, a priority-based arbitration mechanism was implemented, where one port is given higher priority. This ensures deterministic and reliable operation. The inclusion of single-port mode further increases flexibility for specific applications. Verification was performed through multiple test cases including normal read/write operations, simultaneous dual-port access, write conflicts, and single-port operation. Simulation waveforms confirmed correct functionality and expected outputs. This project provided valuable practical experience in VLSI and FPGA design concepts such as synchronous design, memory inference, pipelining, arbitration, modular design, and verification techniques. Such experience is highly useful for applications in digital signal processing, communication systems, embedded systems, and System-on-Chip designs.

To conclude, the implemented dual port memory module can be considered a solid, scalable component of any high-speed digital electronic system. Apart from achieving the goals, this project also laid a solid ground for future improvements.

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