Concise Review of Low-Noise High Stability BJT Pierce Oscillators with SAW Resonators

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***Abstract*—Low-noise SAW (Surface Acoustic Wave) resonator-based oscillators are typically used in systems where high frequency stability, low phase noise, and good signal quality are required, along with compact size. They appear in a wide range of applications, including transmitters and receivers in wireless RF communication, local oscillators in superheterodyne receivers, frequency sources in mobile communication systems, and timing elements in satellite and GPS-based systems.**

This work focuses on the fundamental principles behind the design of such oscillators. It starts with the basic concept of oscillation and extends through established conditions such as the Barkhausen criterion and Kurokawa's negative-resistance approach. It also considers the nonlinear amplitude of stabilization and other practical aspects that influence oscillator behavior.

Particular attention is given to phase-noise reduction, since it remains one of the key limitations in high-performance designs. This is approached by examining how different parameters such as the active device and the power supply affect overall performance.

The paper also discusses the trade-offs that arise between efficiency, noise, and stability. These factors do not vary independently, so improving one often impacts the others. Based on this, the study outlines design approaches that aim to achieve better signal quality and improved selectivity, especially at higher operating frequencies.

***Index Terms*—Low-phase noise SAW Oscillators, RF Oscillator Design, BJT-based Pierce Oscillator, amplitude stabilization, frequency pushing**

I. INTRODUCTION

Surface Acoustic Wave (SAW) resonator-based oscillators have become an important part of modern communication and high-frequency electronic systems due to their ability to provide high frequency stability, compact size, low phase noise, and improved signal quality [4], [6], [7]. These oscillators are widely used in wireless communication systems, RF transmitters and receivers, satellite communication, radar systems, sensor networks, and precision timing applications where accurate frequency generation is required [4], [6]. Among various oscillator configurations, the Pierce oscillator topology is commonly preferred because of its simple circuit structure, reliable operation, and compatibility with high-Q resonators such as SAW devices [10]. However, despite their advantages, practical SAW oscillators are affected by several limitations including phase noise, frequency drift, resonator losses, impedance mismatches, and power-supply-induced disturbances [1], [3], [11]. Variations in the power supply can alter the operating characteristics of the active device and introduce unwanted fluctuations that degrade oscillator performance through frequency pushing and amplitude-to-phase conversion effects [3], [11], [12]. Therefore, maintaining a stable and low-noise power supply becomes an important requirement for improving overall system performance [3]. The proposed work focuses on the design and analysis of a 100 MHz SAW oscillator using a BJT-based Pierce oscillator topology with emphasis on improving frequency stability and output signal quality [10], [11]. A power-supply noise reduction approach is incorporated through the use of a low-pass filtering technique to suppress unwanted noise and ripple components. The proposed system aims to reduce supply-induced disturbances and improve spectral purity while maintaining stable oscillator operation [3], [4]. The expected outcome of the work is a low-noise and highly stable oscillator suitable for RF and wireless communication applications [4], [6].

II. OSCILLATOR

A. Introduction

An oscillator is a steady AC waveform generator using DC power and a feedback system. It does not use any external input; instead, it uses internal circuit noise, such as flicker noise, thermal noise, etc. [1]. The output is sustained due to internal loop

conditions [1]. Every oscillator satisfies 2 conditions for steady and sustained oscillations, which are called the necessary conditions of the Barkhausen criterion given by Heinrich Barkhausen [1], [2]. Barkhausen Criterion has the following 2 conditions –

1. The closed-loop gain, which is the product of the open-loop gain and the feedback factor of the amplifier used in the oscillator, should be unity for sustained oscillations [1], [2].

$$|A\beta| = 1 \qquad [1], [2]$$

2. The total phase shift caused by the amplifier stage and the feedback stage should be equal to 0º or a multiple of 360º (2π).

$$\angle A\beta = 0° \; or \; n2\pi \; , n \in Z \qquad [1], [2]$$

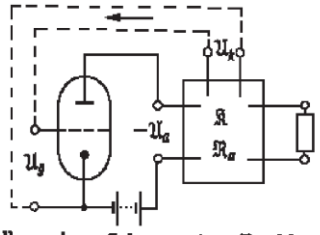


Bild 1. Allgemeines Schema einer Rückkopplung

(1) $\mathfrak{U}_a = -\mathfrak{B}\mathfrak{U}_e$; $\mathfrak{B} = -\frac{\mathfrak{U}_a}{\mathfrak{U}_e} =$ „*Verstärkungsfaktor*“

(2) $\mathfrak{k} = -\frac{\mathfrak{U}_k}{\mathfrak{U}_a} =$ „*Rückkopplungsfaktor*“

(3) $\mathfrak{k} = \frac{1}{\mathfrak{B}}$ oder $\mathfrak{k}\mathfrak{B} = 1$

(*Allgemeine Selbsterregungsformel.*)

Fig.1. Barkhausen’ s initial observations [2]

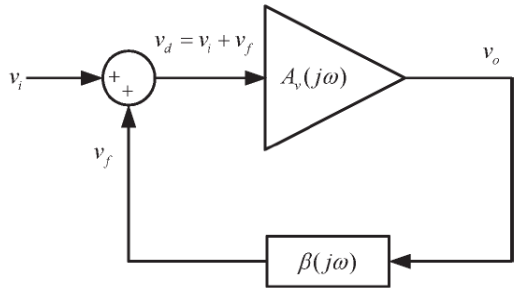


Fig.2. Basic feedback circuit [1]

B. SAW Resonator and Oscillator

Surface Acoustic Wave (SAW) resonator is a high-frequency passive device that uses mechanical resonance, that is, the resonance is achieved using the standing acoustic waves on the surface of a piezoelectric material [4]. This resonator is different from the others, like LC tank or crystal resonators, which use bulk vibrations [4]. The energy in SAW resonators is confined up to the depth of one wavelength of the substrate surface, as Rayleigh waves are the predominant mode of signal transmission [5]. Amplitude of Rayleigh waves decay exponentially as the wave moves into the bulk of the substrate, where the displacement components vary by an approximate formula, $e^{-2\pi y/\lambda}$ where y is the depth [5].

The working principle of the SAW resonator is the inverse piezoelectric effect, where the electric signals are converted back into mechanical vibrations [4], [6]. The physical structure of a SAW resonator is fabricated on a thin piezoelectric substrate using photolithography, using which the metal electrodes, usually of gold or aluminum, are patterned [4], [6]. There are 3 main components IDTs, reflectors, and aperture, the first one being Interdigital Transducers (IDTs) that are the comb-shaped electrodes (with ‘fingers’) which determine the frequency of the SAW resonator. The center-to-center distance, which is called the pitch, is equal to $\frac{\lambda}{2}$, thus, it determines the wavelength (λ) of the SAW resonator, and therefore, its frequency [6]. When RF voltage is applied to the IDTs, the periodic electric field causes the piezoelectric substrate to expand and contract [6]. This expansion and contraction cause Rayleigh waves [5], [6]. These waves travel along the surface until they hit the reflector gratings or Bragg mirrors [4], [6]. These reflectors are shorted or open-circuit metal strips that generally have a period of $\frac{\lambda}{2}$ to satisfy the Bragg condition [4], [6]. These reflect the signal back to the cavity [4], [6]. Standing waves are created only when these reflectors bounce the waves back and forth, and constructive interference occurs [4], [6]. The aperture here is the overlap length of IDT fingers [4], [6]. This influences the resonator’s impedance and coupling strength [4], [6].

Frequency Determination:

Here, the resonant frequency is governed by the physical properties of IDTs and the properties of the substrate material [7]:

$f_r = \frac{v}{\lambda}$ where, v is the phase velocity of the SAW in a specific material and λ is the wavelength defined by IDT finger spacing [7].

1 Port and 2 Port SAW resonator ECM

Most of the time, finding the correct SPICE model of a SAW resonator in a simulation environment is

tough. To ease this, Equivalent Circuit Models (ECM) are devised. There are two types of SAW resonators based on the number of ports. A 1 Port SAW is where a single IDT acts as input and output too, and is placed in between 2 reflector gratings [7], [8]. So, it excites the acoustic wave and senses the reflected wave simultaneously [7], [8]. Thus, it acts like a passive two-terminal impedance [7], [8].

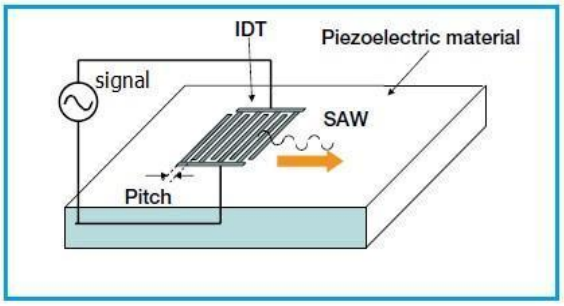


Fig.3. 1 Port SAW Resonator [8]

1 Port SAW ECM design considerations –

The electrical model for a 1-port SAW resonator is the Butterworth-Van Dyke (BVD) model, which has a static branch in parallel with the motional branch [7], [8]. The motional branch represents the mechanical resonance of the surface wave, where L (Motional Inductance) represents acoustic mass or inertia, C (Motional Capacitance) represents acoustic elasticity, and R (Motional Resistance) represents damping or acoustic and mechanical losses [7], [8]. The static branch represents parasitic or static capacitance C_o formed due to IDT electrodes [7], [8].

Resonant Frequency (f_r):

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{v}{\lambda} \quad [9]$$

Wavelength (λ):

$$\lambda = 2p \quad [9]$$

Static Capacitance (C_o):

$$C_o = N.W.C_{pair} \quad [9]$$

Where N is the number of finger pairs, W is the aperture and C_{pair} is the capacitance per finger pair unit.

Quality factor (Q_f): Is a dimensionless quantity which depicts the efficieny and sharpness of resonator as it's the ratio of peak energy stored to energy lost per cycle. A higher Q_f represents lower damping and narrower bandwidth (Δf) which is significant for oscillator stability and filter selectivity.

$$Q_f = \frac{2\pi f_r L}{R} = \frac{f_r}{\Delta f} \quad [9]$$

Motional Inductance (L):

$$L = \frac{Q_f R}{2\pi f_r} \quad [9]$$

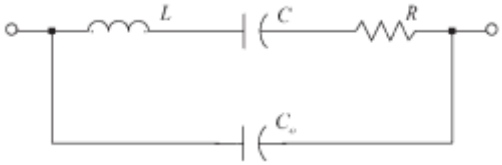


Fig.4. 1 Port SAW resonator ECM [1]

A 2 Port SAW uses two separate IDTs – one for input and the other one for output which are sandwiched between the two reflector gratings. The input IDT converts the electrical signal into mechanical wave, which resonates within the cavity formed by the gratings and is then picked up by the output IDT. Here the SAW resonator behaves like a transmission device or a very narrow band filter which is characterized by insertion loss and phase shift.

1 Port SAW is best suited for Colpitts oscillator and can be a bit nosy compared to 2 Port SAW [1]. Whereas, 2 Port SAW is best suited for Pierce oscillator and has better frequency stability and lower phase noise [1].

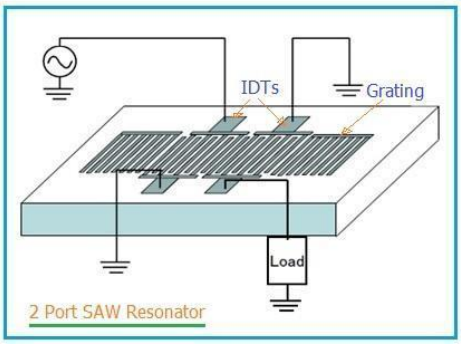


Fig.5. 2 Port SAW resonator [8]

2 Port SAW ECM design considerations –

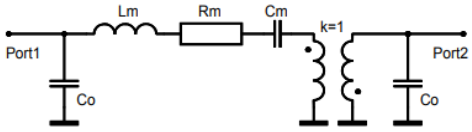


Fig.6. 2 Port SAW resonator ECM [10]

The concept is similar to 1-port SAW resonator but here there are two static capacitances and both will be

equal if both IDTs are equal [10]. Here, an additional ideal transformer is added to represent the electromechanical energy conversion and provide 180º phase shift [10].

Resonant Frequency (f_r):

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{v}{\lambda} \quad [10]$$

Wavelength (λ):

$$\lambda = 2p \quad [10]$$

Static Capacitance (C_o):

$$C_o = N.W.\epsilon_0\epsilon_r \quad [10]$$

Where ϵ_0, ϵ_r are the permittivity constants of vacuum and substrate.

Motional Capacitance (C):

$$C = C_o.\frac{8k^2}{\pi^2} \quad [10]$$

Where k is the electromechanical coupling coefficient of the material.

Motional Inductance (L):

$$L = \frac{1}{(2\pi f_r)^2 C} \quad [10]$$

Quality Factor (Q_f):

$$Q_f = \frac{2\pi f_r L}{R} = \frac{1}{2\pi f_r CR} \quad [10]$$

The main advantages of using a SAW resonator over an LC tank or a quartz crystal is its HF range of oscillation, starting from 30MHz to several GHz, has greater frequency stability over time and varying environmental conditions, has a very high-quality factor and thus lower phase noise, and is very compact and lightweight as acoustic waves are 100000 times shorter than electromagnetic waves at the same frequency [1].

C. SAW Resonator-based Oscillator using BJT

Research Gaps -

After reviewing numerous research papers, the following research gaps were identified: There is no specific 100 MHz SAW resonator-based oscillator with phase noise below -155 dBc/Hz at a 10kHz frequency offset. Most of the papers explain the impedance matching more than the actual circuit to be designed and made. Rarely have papers explained the power supply design for the oscillator with the oscillator design simultaneously.

Why BJT over MOSFET -

Here, the BJT is chosen over the MOSFET because it has superior phase noise performance due to lower flicker noise, which implies a much lower noise corner frequency and thus produces a cleaner signal with less jitter [11]. BJT has higher transconductance than comparable MOSFET for the same amount of bias current, thus this allows BJT to provide higher gain at higher frequencies, and also it is easier for the BJT to overcome insertion losses of the SAW resonator, ensuring reliable start-ups [11]. The parasitic capacitances of high-performance BJT are lower than those of a comparable MOSFET, which reduces the loading effect on the resonator and maintains a higher overall loaded Q factor [11].

Common Emitter (CE) configuration of BJT design

Basic formulae to design a CE amplifier at a specific frequency:

1. $V_{CEQ} = \frac{V_{CC}}{2}$ [12]
2. $I_C = \frac{V_{CC}}{10R_c}$ [12]
3. $P_Q = V_{CEQ}.I_C$ [12]
4. $I_E = I_B + I_C$ [12]
5. $I_C = \beta I_B$ [12]
6. $R_E = \frac{V_E}{I_E}$ [12]
7. $r_e = \frac{V_T}{I_E}$ [12]
8. $|A_V| = \frac{R_C || R_L}{r_e + R_{E1}}$ [12]
9. $V_{BE} = V_B - V_E$ [12]
10. $I_{div} = 10I_B$ [12]
11. $R_1 + R_2 = \frac{V_{CC}}{I_{div}}$ [12]
12. $V_B = V_{CC}.\frac{R_2}{R_1+R_2}$ [12]
13. $R_{in} = R_1||R_2||\beta(r_e + R_{E1})$ [12]
14. $C_{in} = \frac{1}{2\pi R_{in} f_L}$ [12]
15. $R_{out} = R_C||R_L$ [12]
16. $C_{out} = \frac{1}{2\pi R_{out} f_L}$ [12]
17. $R_E = R_{E1} + R_{E2}$ [12]
18. $C_E = \frac{1}{2\pi R_E f_L}$ [12]

III. POWER SUPPLY FILTERS

A. Introduction

Power-supply-induced noise is one of the significant factors affecting the performance of oscillator systems. Variations in supply voltage can introduce disturbances into the active device and resonator network, leading to frequency instability, increased phase noise, and degradation in output signal quality [3], [11]. Supply fluctuations may also produce frequency pushing and amplitude-to-phase conversion effects that adversely affect spectral purity [3]. Therefore, minimizing supply-induced disturbances becomes necessary for achieving stable and low-noise oscillator operation. To overcome these effects, a power supply filtering approach is incorporated into the proposed system.

B. Proposed Filter Design and Mathematical Analysis

To reduce unwanted ripple and noise components, a third-order π low-pass filter topology was selected due to its higher attenuation characteristics and improved suppression capability compared to lower-order filters. The proposed filter consists of two capacitors and one inductor arranged in a C-L-C configuration. The capacitors provide low impedance paths for AC noise components, while the inductor opposes rapid current variations and blocks unwanted disturbances.
The cutoff frequency of the filter is determined by:

$$fc=1/(2\pi\sqrt{LC})$$

For the proposed design:

Input Voltage = 15 V

Output Voltage = 5 V

Injected noise signal = 10 mV AC

Target cutoff frequency = 50–60 Hz
Selected component values:

C_1 = 100 µF

L = 100 mH

C_2 = 100 µF
The selected component values provide an approximate cutoff frequency of 55 Hz, allowing effective attenuation of unwanted supply disturbances while maintaining the required DC output.

C. Selection of Filter Topology

Different filter configurations provide different levels of attenuation and complexity [13]. First-order RC filters provide simple implementation but generally exhibit limited attenuation characteristics. LC filters improve selectivity and offer reduced power losses. However, higher-order π filters provide superior suppression performance because of their combined capacitive and inductive behavior [14].

The third-order π filter was selected for the proposed work because it provides improved attenuation of supply-induced disturbances while maintaining a relatively simple structure. The use of multiple reactive elements enhances filtering capability and improves voltage smoothening performance. This makes the π filter suitable for applications requiring stable and low-noise power supplies such as RF oscillator systems [13], [14].

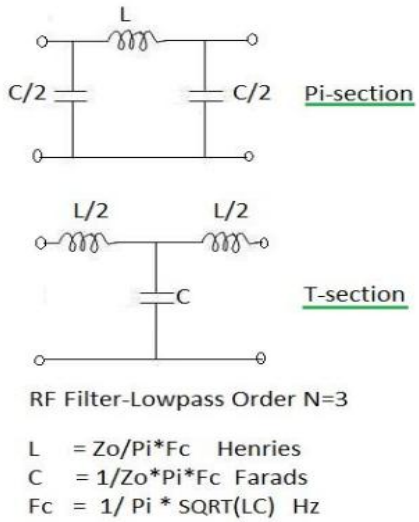


Fig.7. RF Low Pass Order of circuit is 3

This diagram illustrates commonly used passive low-pass filter configurations including π-section and T-section topologies. Among these configurations, the π filter structure was selected for the proposed work because it provides improved attenuation characteristics and better suppression of unwanted ripple components. The use of capacitive elements at both input and output stages along with an inductive element in the center improves filtering efficiency and enhances power-supply stability.

D. Circuit Implementation

The proposed power-supply noise reduction circuit is implemented using a third-order π low-pass filter configuration connected between the DC supply

source and the oscillator circuitry. The primary objective of the filtering stage is to minimize unwanted AC ripple components and external disturbances before they reach the active oscillator components. Since supply fluctuations directly affect the operating point of transistors and other active elements, proper filtering becomes important for maintaining stable oscillator behavior.

The input to the proposed system consists of a 15 V DC power source with an injected AC noise signal of approximately 10 mV. This noise signal represents practical disturbances that may arise from switching devices, regulator circuits, electromagnetic interference, and external electronic components. If these disturbances are allowed to propagate directly into the oscillator circuitry, they can introduce amplitude fluctuations and frequency instability.

The third-order π filter consists of two capacitors and one inductor connected in a C-L-C configuration. The first capacitor, C_1, performs initial filtering by providing a low-impedance path for AC noise signals and diverting them toward ground. This process reduces the amount of unwanted disturbance entering the remaining circuit stages. The inductor L acts as the main filtering element and opposes sudden variations in current flow according to the principle of electromagnetic induction. Since the inductor presents higher impedance to AC components and lower impedance to DC components, ripple propagation through the circuit is significantly reduced. The second capacitor, C_2, performs secondary filtering by suppressing remaining disturbances and smoothing the voltage waveform.

After the filtering stage, a voltage regulator is introduced to convert the filtered 15 V DC signal into a regulated 5 V DC output suitable for oscillator operation. The voltage regulator maintains a stable output level even under minor supply variations and load fluctuations. The combined action of the π filter and voltage regulator creates a cleaner and more stable power source for the oscillator circuitry.

The selected component values for the proposed design are:

$C_1 = 100\ \mu F$

$L = 100\ mH$

$C_2 = 100\ \mu F$

Input Voltage = 15 V

Output Voltage = 5 V

Injected Noise Signal = 10 mV AC

These component values are selected to achieve a cutoff frequency close to the desired operating range while providing efficient suppression of unwanted disturbances.

E. Expected Results and Performance Analysis

The performance of the proposed filtering technique is evaluated by analyzing the behavior of the supply signal before and after the implementation of the filtering stage. The primary objective is to determine the ability of the filter to suppress AC disturbances and improve the quality of the power delivered to the oscillator system.

At the input stage, the supply signal consists of a DC component combined with an unwanted AC ripple component. Due to the presence of this ripple signal, the waveform may contain fluctuations around the desired operating voltage. These fluctuations can alter the operating characteristics of the active device and contribute to phase-noise degradation and frequency instability within the oscillator system [16].

After passing through the third-order π filter, a significant reduction in the AC ripple component is expected. The output waveform is expected to become smoother with reduced voltage variations and lower noise content. Following the voltage regulation stage, the output should provide an approximately constant 5 V DC signal with negligible ripple components.

Several performance parameters may be considered during analysis, including:

- Input ripple voltage
- Output ripple voltage
- Ripple attenuation percentage
- Voltage regulation performance
- Frequency stability improvement
- Reduction in supply-pushing effects

• Improvement in signal purity

The implementation of the proposed filtering technique is expected to improve overall oscillator performance by reducing unwanted disturbances that affect the active device and resonator network [16]. Improved filtering can reduce frequency variations and minimize noise propagation into the oscillator circuit. Furthermore, better supply quality is expected to contribute toward enhanced spectral purity and lower phase-noise characteristics.

The higher-order π filter structure also provides better attenuation characteristics compared to simple RC and LC filter configurations because of the combined action of multiple reactive components [13], [14]. This allows improved suppression of supply-induced disturbances and provides more reliable operation for RF and wireless communication systems.

G. Simulation Waveforms

The performance of the proposed filtering system can be analyzed using simulation waveforms obtained before and after implementation of the filtering stage. The following waveforms are considered:

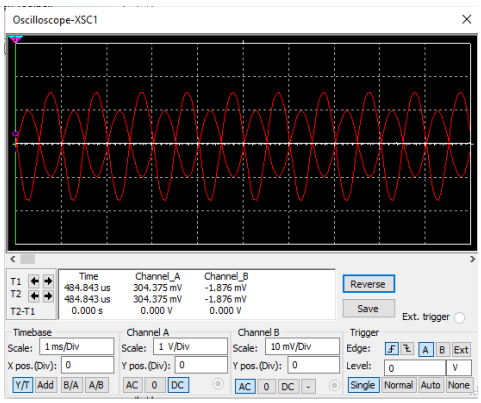
• Input voltage waveform with injected noise
• Filter output waveform
• Regulated output voltage waveform
• Ripple comparison before and after filtering
• Frequency response of the proposed filter

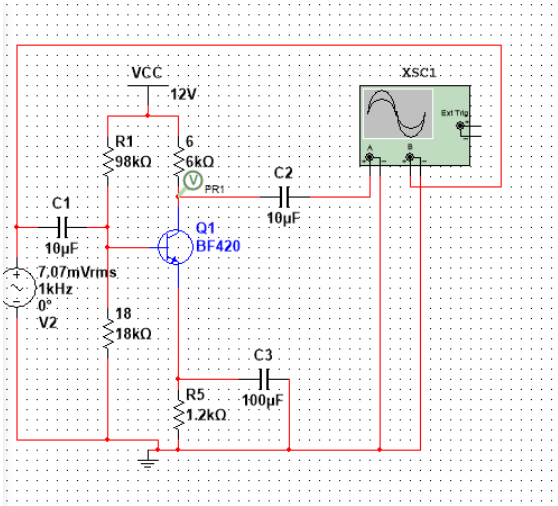
The comparison of these waveforms helps evaluate the effectiveness of the proposed filtering approach in reducing supply-induced disturbances.

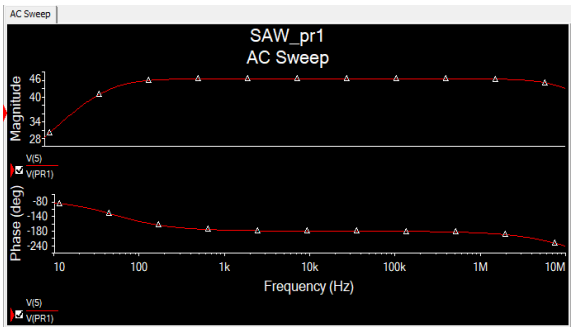
IV. SIMULATION RESULTS

A. Amplifier and Oscillator

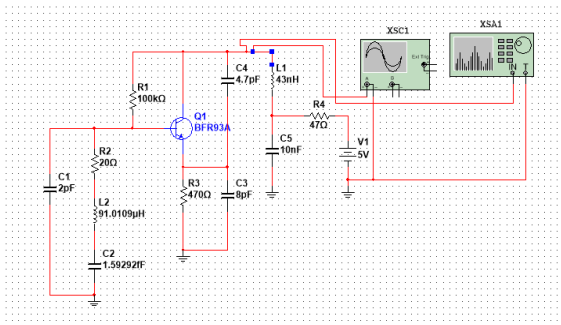
Amplifier circuit -



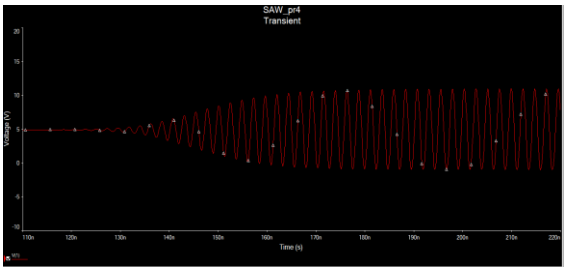




This is an example of a 1kHz CE BJT amplifier design. The selectivity can be changed by selecting the correct value for f_L.

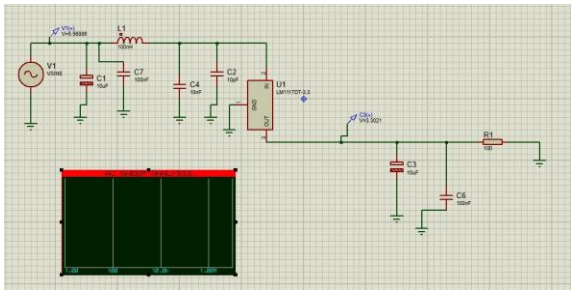


This is 1-Port SAW resonator circuit.

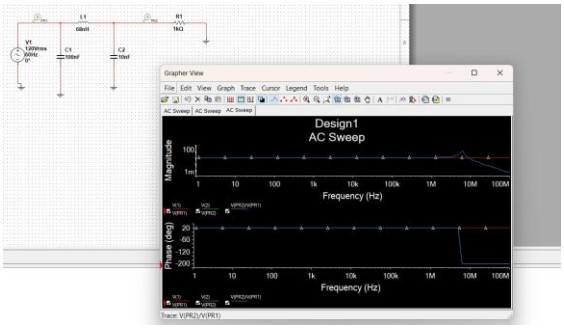


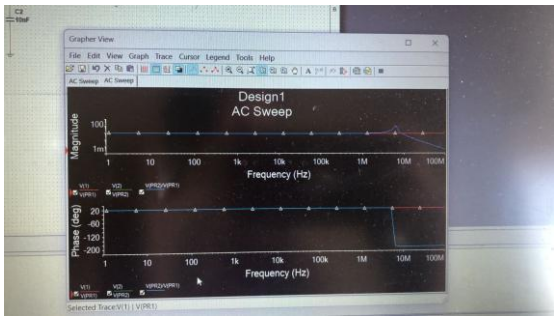
Transient response of the circuit.

B. *Filters*



The proposed power-supply noise reduction circuit was implemented and analyzed using simulation tools. The above circuit shows the designed π-filter integrated with a voltage regulation stage to suppress unwanted disturbances and improve supply stability.





This presents the AC sweep response of the filter, illustrating its attenuation characteristics over different frequencies. The results indicate effective suppression of unwanted noise components, resulting in improved power quality and more stable operation of the oscillator system.

V. POWER SUPPLY DESIGN

Phase noise and frequency stability in SAW oscillator-based RF systems are highly sensitive to power supply noise, ripple, and load transient response. A dedicated 5 V regulated supply, derived from a 15 V nominal input, powers the BJT amplifier and associated circuitry. This section presents the complete design methodology of a synchronous step-down (buck) DC-DC converter employing the Texas Instruments TPS561208DDC [13], covering topology selection, analytical design equations, component sizing, and WEBENCH/TINA-TI simulation-based performance verification

A. Converter Topology and IC Selection

A non-isolated synchronous buck topology is adopted for its superior efficiency, compact component count, and low output ripple at the required 3:1 voltage conversion ratio. The TPS561208DDC is a 1 A, 4.5–17 V input synchronous step-down converter in a 6-pin SOT-23 package [13]. It employs Texas Instruments' D-CAP2™ adaptive on-time PWM control, providing fast transient response and inherent stability with low-ESR ceramic capacitors without external frequency compensation [13]. Key parameters include: RDS(on),H = 140 mΩ, RDS(on),L = 84 mΩ, nominal switching frequency fsw = 580 kHz, internal soft-start = 1.0 ms, and VREF = 0.768 V. The device operates exclusively in CCM across its full load range, eliminating mode-transition-induced spectral interference on the supply rail [13].

B. Circuit Implementation

The converter is designed per the TPS561208 reference application circuit [13], with component values optimised using TI WEBENCH Power Designer. The TINA-TI SPICE simulation schematic is shown in Fig. 10, with all principal measurement nodes annotated. Both the WEBENCH and TINA-TI circuits share identical values: L1 = 4.7 µH (DCR = 80 mΩ), Cout = 47 µF (ESR = 2.143 mΩ), Cin = 2 × 10 µF (ESR = 5.463 mΩ each), Cbst = 100 nF, Rfbt = 56.2 kΩ, and Rfbb = 10 kΩ.

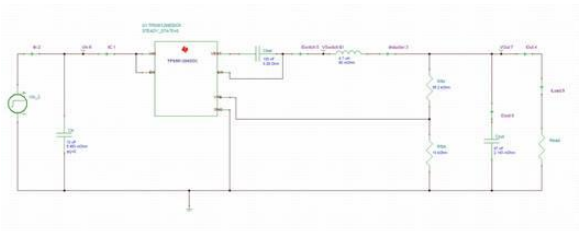


Fig. 10. TINA-TI transient simulation schematic of the TPS561208DDC buck converter. Configured for Vin = 15 V, Vout = 5 V, Iout = 1 A. All measurement nodes labelled [13].

C. Duty Cycle and Switching Frequency

In steady-state CCM, the voltage conversion ratio equals the duty cycle D:

$$D = V_{out} / V_{in} = 5.0 / 15.0 = 0.333 \ (33.3\%) \qquad (1)$$

D-CAP2 implements an adaptive on-time architecture maintaining quasi-fixed switching frequency across the input range [13]. WEBENCH computation at Vin = 15.6 V yields D = 33.22% and fsw = 538.95 kHz. Figure 11 shows the WEBENCH-simulated duty cycle versus output current across three input voltages. The monotonic positive slope reflects additional on-time needed to compensate resistive drops across RDS(on) and inductor DCR as load increases.

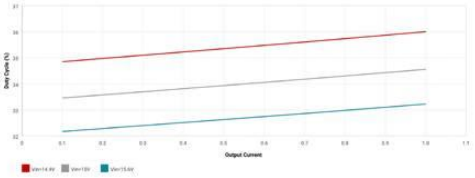


Fig. 11. WEBENCH-simulated duty cycle (%) vs. output current (A) for Vin = 14.4 V (red), 15 V (grey), and 15.6 V (teal). Duty cycle rises from ≈ 32% to ≈ 36% across the 0–1 A load range [13].

D. Output Voltage Setting

Output voltage is programmed via a resistor divider to the VFB pin (VREF = 0.768 V) [13]:

$$Vout = VREF \times (1 + Rfbt / Rfbb) \quad (2)$$

Substituting Rfbt = 56.2 kΩ and Rfbb = 10 kΩ gives Vout = 0.768 × 6.62 = 5.084 V — a 1.6% deviation from the 5.0 V target, within the 4.23% tolerance budget for 2% IC feedback and 1% resistor tolerances [13]. Both steady-state simulations confirm Vout,avg = 5.14 V.

E. Output Inductor Sizing

Peak-to-peak inductor ripple current in CCM [13]:

$$\Delta IL = (Vout / Vin,max) \times (Vin,max - Vout) / (L \times fsw) \quad (3)$$

With L = 4.7 µH, Vin,max = 15.6 V, Vout = 5 V, and fsw = 538.95 kHz: ΔIL = 1.36 A. Peak switch current IL,peak = 1.0 + 0.68 = 1.68 A, below the 2.0 A OCL limit [13]. RMS current IL,rms = $\sqrt{(1.0^2 + 1.36^2/12)}$ ≈ 1.07 A gives PL = 1.07^2 × 80 mΩ ≈ 91.5 mW (WEBENCH: 92.34 mW).

F. Output Capacitor and Ripple Analysis

Peak-to-peak output voltage ripple for a low-ESR ceramic capacitor:

$$\Delta Vout \approx \Delta IL \times (ESR + 1 / (8 \times Cout \times fsw)) \quad (4)$$

With Cout = 47 µF (ESR = 2.143 mΩ), ΔIL = 1.36 A: ΔVout ≈ 9.6 mV analytically; WEBENCH reports 19.06 mV. Steady-state TINA-TI simulation (Fig. 12) confirms ΔVout = 16.20 mV at Vout,avg = 5.14 V and fsw = 590.20 kHz — all within the 30 mV design limit. Output capacitor RMS current ICo,rms = 392.7 mA gives Pd,Cout = 330.48 µW [13].

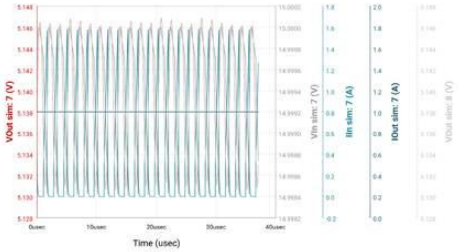


Fig. 12. TINA-TI steady-state simulation: Vout oscillates between 5.130 V and 5.148 V, yielding ΔVout = 16.20 mV peak-to-peak at Vout,avg = 5.14 V and fsw = 590.20 kHz [13].

G. Input Capacitor Selection

Two 10 µF / 25 V ceramic capacitors in parallel give Cin,eff = 20 µF. Input ripple current:

$$ICin,rms = Iout \times \sqrt{(D \times (1 - D))} = 1.0 \times \sqrt{(0.333 \times 0.667)} \approx 471 \text{ mA} \quad (5)$$

WEBENCH reports ICin,rms = 522.56 mA (including inductor ripple), well within each capacitor's 2.37 A rating, with Pd,Cin = 745.9 µW. A 100 nF bootstrap capacitor (Cbst) between VBST and SW is mandatory for high-side gate drive biasing [13].

H. Thermal Analysis and Power Budget

IC power dissipation is modelled as [13]:

$$PIC = Iout^2 \times (RDS(on),H \times D + RDS(on),L \times (1-D)) + Psw \quad (6)$$

WEBENCH reports PIC = 249.12 mW, PL = 92.34 mW, Pd,Cout = 330.48 µW, and Pd,Cin = 745.9 µW, giving Ptotal = 342.9 mW. Junction temperature:

$$Tj = Ta + PIC \times \theta JA,eff = 30 + 249.12 \times 10^{-3} \times 60 = 44.95°C \quad (7)$$

At 44.95°C — 80°C below the 125°C rated maximum and 115°C below the 160°C thermal shutdown threshold — the design supports continuous operation at ambient temperatures up to ≈ 80°C without derating [13].

I. Efficiency Analysis

Full-load conversion efficiency:

$$\eta = Pout / Pin = 5.0 / (5.0 + 0.343) = 93.58\% \quad (8)$$

Figure 13 presents the WEBENCH efficiency curves across Vin = 14.4 V, 15 V, and 15.6 V. Peak efficiency of ≈ 94–95% is achieved at 0.5–0.6 A partial load. The three curves overlap closely,

confirming less than 1 percentage point variation across the input voltage range — important for RF supplies subject to upstream transients.

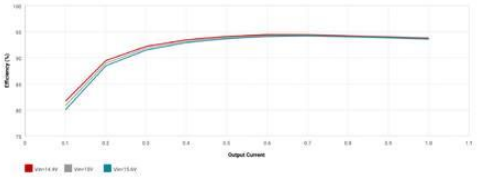


Fig. 13. WEBENCH efficiency (%) vs. output current (A) for Vin = 14.4 V (red), 15 V (grey), and 15.6 V (teal). Full-load efficiency is 93.58% at Vin = 15.6 V; peak ≈ 94–95% at partial load [13].

J. Soft-Start and Startup Behavior

The integrated 1.0 ms soft-start linearly ramps the internal reference on EN assertion, preventing inrush current and inductor saturation [13]. Figure 14 shows the TINA-TI startup simulation: Vout rises monotonically from 0 V and achieves 90% of its 5.14 V regulated value within 0.94 ms, with no overshoot or oscillation. Peak inductor current during startup is 1.72 A — below the 2.0 A OCL limit [13].

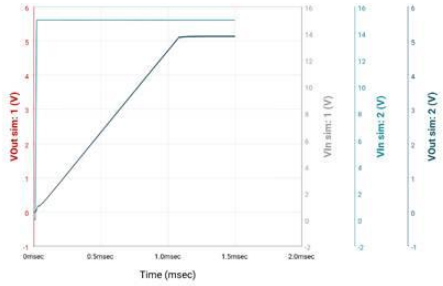


Fig. 14. TINA-TI startup simulation: Vout ramps from 0 V to steady-state ≈ 5.14 V. Output settles within 0.94 ms with no overshoot, confirming correct D-CAP2 soft-start operation [13].

K. Load Transient Response

Load transient performance (Fig. 15) for a 1.0 A ↔ 0.1 A step with 10 µs transition edges shows symmetrical overshoot/undershoot of 70 mV (1.36% of Vout) with a 20 µs recovery time. D-CAP2 re-asserts the on-pulse within one switching cycle of detecting a feedback error [13], comparing favourably with conventional voltage-mode PWM controllers that typically require several cycles. This is well within the ±5% (±250 mV) transient specification.

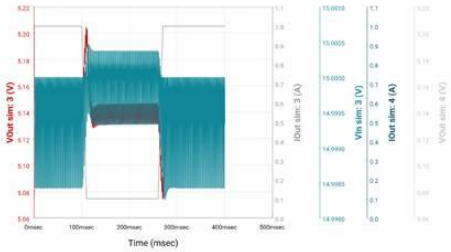


Fig. 15. TINA-TI load transient simulation: VOut exhibits 70 mV overshoot/undershoot for a 1.0 A ↔ 0.1 A step, recovering to regulation within 20 µs. Vout,avg = 5.14 V [13].

L. Input Transient Response

Figure 16 shows the output response to a Vin step between 14.4 V and 15.6 V under a fixed 1 A resistive load. Output voltage deviation is below 20 mV (0.39%) across the 1.2 V (8%) input step, with recovery within 50 µs — a line rejection ratio exceeding 26 dB. This level of power supply rejection is adequate for the BJT amplifier and oscillator stages, where supply-induced noise directly sets the phase noise floor.

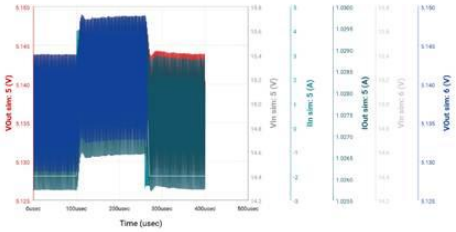


Fig. 16. TINA-TI input transient simulation: Vout deviation < 20 mV for a 1.2 V Vin step (14.4 V ↔ 15.6 V), recovering within 50 µs. Load current remains stable at 1.028 A [13]

TABLE I. POWER SUPPLY BILL OF MATERIALS – TPS561208DDC BUCK CONVERTER

Component	Part / Value	Specification	Qty
U1 – TPS561208 DDC	IC – Sync. Buck	Vin: 4.5–17 V, Vout: 0.76–7 V, 1 A, 580 kHz	1
L1 – Output Inductor	NIC NPI43C4R7M TRF	4.7 µH, DCR = 80 mΩ	1
Cout – Output Cap.	TDK C3216X5R1C 476M160AB	47 µF, ESR = 2.143 mΩ, 16 V, X5R	1
Cin – Input Cap.	Taiyo Yuden MSAST21GB	10 µF, ESR = 5.463 mΩ, 25 V, X5R	2

	B5106MTNA01		
Cbst – Bootstrap Cap.	AVX 08053C104KAT2A	100 nF, ESR = 280 mΩ, 25 V, X7R	1
Rfbt – Upper Feedback R	Yageo RC0201FR-0756K2L	56.2 kΩ, 1%, 50 mW	1
Rfbb – Lower Feedback R	Yageo RC0201FR-0710KL	10.0 kΩ, 1%, 50 mW	1

TABLE II. SIMULATED PERFORMANCE SUMMARY – 15 V TO 5 V SYNCHRONOUS BUCK CONVERTER

Parameter	Simulated Value	Design Target / Spec.
Input Voltage (Vin)	14.4 – 15.6 V	4.5 – 17 V
Output Voltage (Vout,avg)	5.14 V	5.0 V nominal
Switching Frequency	538.95 kHz (calc.) / 590.20 kHz (sim.)	580 kHz nominal
Duty Cycle	33.22%	Vout/Vin,nom ≈ 33.3%
Conduction Mode	CCM	CCM (full load)
Peak-to-Peak Vout Ripple	16.20 mV (sim.) / 19.06 mV (calc.)	< 30 mV
Peak-to-Peak ΔIL	1.24 A (sim.) / 1.36 A (calc.)	< 1.50 A
Peak Switch Current	1.68 A	< 2.0 A (OCL)
Load Transient Overshoot	70 mV (0.1 A ↔ 1.0 A step)	±250 mV (±5% Vout)
Transient Settle Time	0.02 ms (20 µs)	< 1.0 ms
Efficiency η (full load)	93.58%	> 90% at 1 A
Total Power Dissipation	342.9 mW	< 500 mW
IC Junction Temperature Tj	44.95°C	< 125°C (TJ,max)
Startup Time	0.94 ms	≈ 1.0 ms (internal SS)
Input Cap. RMS Current	522.56 mA	< 2.37 A per capacitor
Output Cap. RMS Current	392.7 mA	< rated IRMS

sim. = TINA-TI steady-state simulation. All values at Ta = 30°C, Vin = 15.6 V, Iout = 1.0 A unless stated.

All simulated parameters satisfy design targets with substantial margin. Output voltage ripple (16.20 mV) and transient deviation (70 mV) remain within the budgets established by the oscillator supply sensitivity analysis. The IC junction temperature of 44.95°C — 80°C below the rated maximum — confirms long-term thermal reliability under continuous full-load operation.

VI. CONCLUSION

This paper presented a concise review and design-oriented analysis of low-noise, high-stability SAW resonator-based Pierce oscillators using BJT technology for RF communication applications. The study discussed the fundamental operating principles of oscillators, Barkhausen stability conditions, SAW resonator characteristics, equivalent circuit modelling, and the advantages of using SAW devices for high-frequency and low-phase-noise applications. The comparison between 1-port and 2-port SAW resonators highlighted the suitability of the 2-port configuration for Pierce oscillator implementations due to its improved frequency stability and lower phase-noise performance.

A BJT-based common-emitter oscillator topology was selected because of its lower flicker noise, higher transconductance, and reduced parasitic capacitances compared to MOSFET-based designs, making it more suitable for stable RF oscillator operation. The paper also emphasized the importance of power-supply quality in oscillator systems, since supply-induced disturbances directly affect phase noise, frequency stability, and spectral purity. To address these issues, a third-order π low-pass filtering approach and a regulated synchronous buck converter power supply were incorporated into the proposed system.

Simulation and analytical results demonstrated that the proposed power-supply design achieved effective ripple suppression, stable voltage regulation, fast

transient recovery, and high conversion efficiency. The TPS561208DDC-based synchronous buck converter delivered a regulated 5 V output with a peak-to-peak ripple of 16.20 mV, transient deviation of 70 mV, and full-load efficiency of 93.58%, while maintaining safe thermal operation with a junction temperature of 44.95°C. These results confirm that the proposed supply architecture is capable of minimizing supply-induced noise and improving overall oscillator stability.

Overall, the proposed approach provides an effective foundation for the development of compact, low-noise, and frequency-stable RF oscillator systems suitable for wireless communication, sensing, and precision timing applications. Future work may include practical hardware implementation, phase-noise characterization, impedance matching optimization, PCB parasitic analysis, and experimental validation of the complete oscillator system under real operating conditions.

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