Design and Analysis of An Optimized 8t SRAM Cell

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Abstract **- Static Random Access Memory (SRAM) serves as a key component in modern electronic systems, especially within a processors operating at high frequencies, cache memory structures, and energy efficient embedded systems. With the continuous scaling of CMOS technology towards nanoscale dimensions, traditional SRAM structures face multiple design constraints [1], including higher leakage current effects, lower operating voltage levels, reduction in noise tolerance, and instability during read access. The commonly implemented 6T SRAM cell[4], while efficient, exhibits stability constraints because of shared access path used for both reading and writing processes, especially in deep sub-micron technologies.This paper describes the design and performance analysis of an 8-Transistor (8T) SRAM cell developed with 45 nm CMOS technology using the Cadence Virtuoso simulation platform[1]. The proposed 8T architecture introduces an imdependent read path that separates the internal storage nodes from the bit lines while reading data,which improves read stability and reducing read interference effects[6]. The circuit performance is evaluated through transient analysis, focusing on key parameters including power dissipation, signal delay, and stability during read operation[6].In addition, a comprehensive parametric analysis is conducted to examine the performance of the SRAM cell across different operating conditions. The simulation outcomes demonstrate that the proposed 8T SRAM cell achieves lower power usage, enhanced Static Noise Margin (SNM), and better operational reliability when compared to conventional 6T SRAM designs. These features make the 8T SRAM cell suitable for energy-efficient and high-performance VLSI systems, including portable devices, Internet of Things (IoT) systems, and advanced computing platforms.**

Keywords: **SRAM, 8T SRAM Cell, 45nm CMOS Technology, Low Power VLSI, Static Noise Margin (SNM), Read Stability, Leakage Power Reduction, Cadence Virtuoso, Transient Analysis, Parametric Analysis, CMOS Scaling, Memory Design, High-Speed Cache Memory, Embedded Systems**

I. INTRODUCTION

Static Random Access Memory (SRAM) is a core memory element widely used in present-day digital hardware. It plays a significant role in microprocessors, microcontrollers, and System-on-Chip (SoC) designs due to its fast access speed, low latency, and ability to retain data without requiring refresh operations. With the rapid advancement of Very Large-Scale Integration (VLSI) systems, there is a growing need for memory units that provide high performance while maintaining low power consumption and efficient area utilization. As a result, SRAM design has become an active research area, particularly with the adoption of nanoscale Complementary Metal-Oxide-Semiconductor (CMOS) technology.Technology scaling has enabled the integration of a large number of transistors onto a single chip, thereby enhancing computational capability. However, when CMOS technology approaches deep submicron levels (such as 45 nm and below), several issues begin to affect the performance and reliability of SRAM cells. These challenges include increased leakage current, reduced operating voltage, process variations, and decreased noise margins. Among these, leakage power and stability are the most critical concerns in SRAM design.Traditionally, the 6-Transistor (6T) SRAM cell has been the standard choice due to its compact structure and efficient functionality. This cell consists of two cross-coupled inverters forming a bistable storage element, along with access transistors that connect the cell to the bit lines for read and write operations. Despite its widespread use, the 6T SRAM cell faces several limitations, particularly in scaled technologies. One major issue is the read disturbance problem, which occurs when the read operation unintentionally alters the stored data. This happens because the same access transistors are used for both read and write operations, causing interference between the bit lines and the internal storage nodes.To overcome these limitations, the 8-Transistor (8T) SRAM cell introduces an improved architecture by separating

the read and write paths. This design includes additional transistors that create a dedicated read path, effectively isolating the internal storage nodes from the bit lines during read operations. As a result, read disturbance is minimized and stability is significantly improved. Furthermore, the 8T SRAM cell achieves a higher Static Noise Margin (SNM) compared to the conventional 6T design, since the read operation does not interfere with the stored data.In addition, separating the read and write operations reduces unnecessary switching activity on the bit lines, leading to lower dynamic power consumption. Although the 8T SRAM cell occupies slightly more area due to the extra transistors, the improvement in stability and power efficiency outweighs this disadvantage. This makes the 8T architecture suitable for modern applications where reliability and energy efficiency are more important than minimal area.With the increasing demand for low-power and high-performance memory systems, the 8T SRAM cell presents a promising solution for future VLSI designs. In this work, an 8T SRAM cell is designed using 45 nm CMOS technology and simulated using the Cadence Virtuoso tool. The performance of the proposed design is evaluated through transient analysis, focusing on parameters such as power consumption, delay, and stability. The results demonstrate improved read stability and reduced power consumption compared to conventional SRAM designs.

II. LITERATURE SURVEY

Several research works have focused on improving the performance of 8T SRAM cells using advanced device technologies and design techniques. One approach utilizes dual-threshold CNTFET-based 8T SRAM cells to achieve reduced power consumption along with faster operation, while also improving switchingcharacteristics and minimizing leakage effects compared to traditional CMOS implementations [1]. Another study explores a FinFET-based 8T SRAM design that emphasizes low power operation and enhanced stability, where the impact of process variations is reduced, leading to improved reliability and manufacturing yield [2].High- speed 8T SRAM designs have also been proposed for cache applications, particularly in L1 memory, where reduced access time and improved read/write performance are critical for high-performance processors [3]. In addition, comparative analyses have been conducted across different technology nodes such as 45 nm, 32 nm, and 22 nm to evaluate variations in performance metrics, including power consumption, delay, and scalability [4]. Further work investigates the implementation of 8T SRAM cells using advanced FinFET technologies at smaller nodes, such as 18 nm, demonstrating improvements in energy efficiency and device scaling advantages [5].Other contributions focus on enhancing stability and noise immunity. For example, Schmitt trigger-based 8T SRAM designs have been introduced to improve noise margins and ensure reliable operation under noisy environments [6]. Write-assist techniques have also been applied to improve write performance without compromising overall cell stability [7]. Additionally, low-leakage 8T SRAM designs have been proposed for energy-sensitive applications, offering improved standby power characteristics and better read stability [8].Specialized designs such as radiation-tolerant 8T SRAM cells have been developed for space applications, where reliability is improved by reducing the impact of radiation-induced faults [9]. Furthermore, single-ended 8T SRAM configurations have been introduced to support low-voltage operation while maintaining acceptable performance levels [10]. Techniques such as gated-VDD and noise reduction methods have also been explored to decrease power dissipation and improve overall efficiency [11]. Data- aware and power-gated SRAM designs further optimize energy usage by adapting power consumption based on stored data patterns [12].Finally, area optimization techniques have been investigated to reduce chip size while maintaining performance, addressing the trade-off between silicon area and efficiency in modern SRAM designs [13]. These studies collectively highlight the continuous advancements in 8T SRAM architectures aimed at achieving low power consumption, high stability, and improved scalability for next-generation VLSI systems.

III. STANDARD 6TSRAM CELL AND ITS LIMITATIONS

A. Structure of 6T SRAM Cell

The 6-transistor (6T) SRAM cell is a widely adopted memory configuration in contemporary digital circuits because of its compact layout and fast operation. The cell is built using six MOS transistors, where four transistors form two cross-coupled inverters that create a bistable storage element

capable of holding one bit of information. The remaining two transistors act as access devices, enabling communication between the internal storage nodes and the external bit lines, commonly denoted as BL and $B\bar{L}$. These access transistors are controlled by the word line (WL), which determines whether the cell is connected to the bit lines for read or write operations.

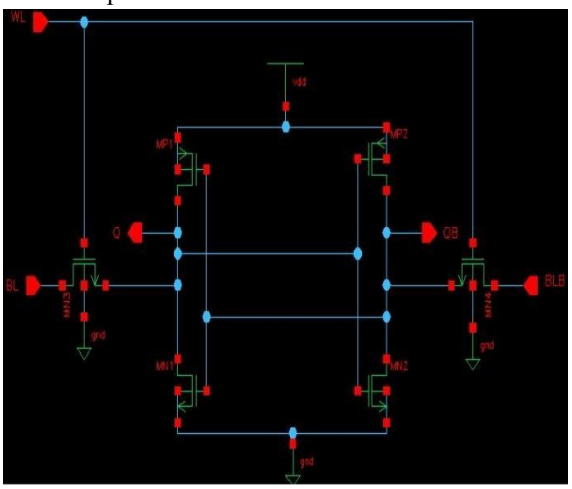

Fig . 1: Transistor-Level Circuit Diagram of the Conventional 6T SRAM Cell

B. Operation of 6T SRAM Cell

The 6T SRAM cell is a fundamental memory element that is widely utilized in modern digital systems. This is because it is very fast and works efficiently with CMOS technology. The 6T SRAM cell consists of six transistors arranged compactly to store a single bit of information. At the core of the 6T SRAM cell are two pairs of transistors forming inverters. These inverters are connected in a way that they can hold either of two stable states, namely logic 0 or logic 1. The 6T SRAM cell also has a pair of transistors that provide access to external circuitry. These transistors are connected through the bit lines, referred to as BL and $B\bar{L}$. The control signal known as the word line (WL) regulates these transistors.

The word line determines the operation of the 6T SRAM cell at any given time. The internal nodes of the inverters are connected such that when one node is at a high voltage, the other remains at a low voltage. This helps maintain the stored information within the 6T SRAM

1) Hold Operation

In the hold state, the word line is kept inactive, which turns OFF the access transistors and isolates the cell from the bit lines. The cross-coupled inverters maintain the stored value through positive feedback, ensuring that the data remains unchanged as long as the power supply is present. This state represents the idle condition of the SRAM cell where no read or write activity takes place.

2) Write Operation

During the write process, the word line is activated to enable the access transistors, allowing the internal nodes of the cell to connect with the bit lines. The input data is applied to BL and $B\bar{L}$ in complementary form. The bit line drivers are designed to overpower the existing state of the cell, forcing the internal nodes to switch to the new data value. Once the write operation is completed, the word line is deactivated, and the cross-coupled inverters retain the updated data.

3) Read Operation

For a read operation, both bit lines are initially precharged to a high voltage level. When the word line is enabled, the internal nodes are connected to the bit lines through the access transistors. Depending on the stored value, one of the bit lines discharges slightly through the pull-down transistor, while the other remains close to its precharged level. A sense amplifier detects this small voltage difference and determines the stored logic value. However, during this process, the internal node storing logic ‘0’ may experience a voltage rise, which can potentially disturb the stored data under certain conditions.

C. Limitations of 6T SRAM Cell

Despite its widespread usage, the 6T SRAM cell has several drawbacks, especially in scaled CMOS technologies. One major concern is the read disturbance problem, where the stored data may be unintentionally altered during a read operation due to the direct connection between internal nodes and bit lines. This issue becomes more severe at lower supply voltages and smaller technology nodes.Another important limitation is the reduction in Static Noise Margin (SNM), which indicates the ability of the cell to withstand noise without losing stored data. During read operations, SNM degrades significantly, making the cell more susceptible to errors caused by process variations, temperature changes, and supply fluctuations.Leakage current is also a critical issue in nanoscale designs. Even when the cell is not actively accessed, leakage paths contribute to power dissipation, which becomes substantial as the number of memory cells increases in large arrays. Additionally, the 6T SRAM cell uses the same path for both read and write

operations, leading to a design trade- off. Strengthening transistors to improve write ability can negatively impact read stability, and vice versa. This interdependence limits design flexibility and makes it challenging to optimize the cell for both performance and power efficiency simultaneously.To overcome these challenges, advanced SRAM architectures such as the 8T SRAM cell have been introduced. These cell while power is supplied. The 6T SRAM cell is very simple and occupies minimal area. This makes it suitable for storing large amounts of data in cache memory. The 6T SRAM cell is therefore preferred because it is compact and operates efficiently.
designs separate the read and write paths, improving stability, reducing read disturbance, and enhancing overall performance in nanoscale technologies.

IV. PROPOSED ARCHITECTURE

The proposed 8-Transistor (8T) SRAM cell is an enhanced version of the conventional 6T SRAM design, developed to improve stability and reliability in scaled CMOS technologies. The basic storage element of the cell remains similar to the 6T structure, consisting of cross-coupled inverters; however, two additional transistors are introduced to form a dedicated read path. This modification enables independent read and write operations, which is the key distinguishing feature of the 8T SRAM cell. By separating the read and write paths, the proposed architecture prevents direct interaction between the storage nodes and the bit lines during read access. This isolation significantly improves read stability and reduces the possibility of data disturbance. The additional transistors are specifically arranged to support this independent read mechanism, making the overall design more robust for low-voltage and nanoscale applications.

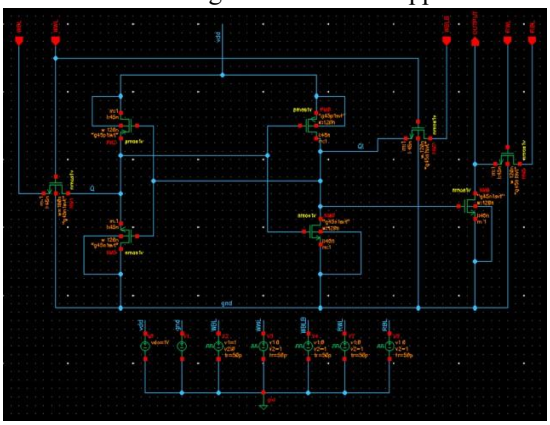

Fig. 2: Transistor-Level Schematic of the Proposed 8T SRAM Cell

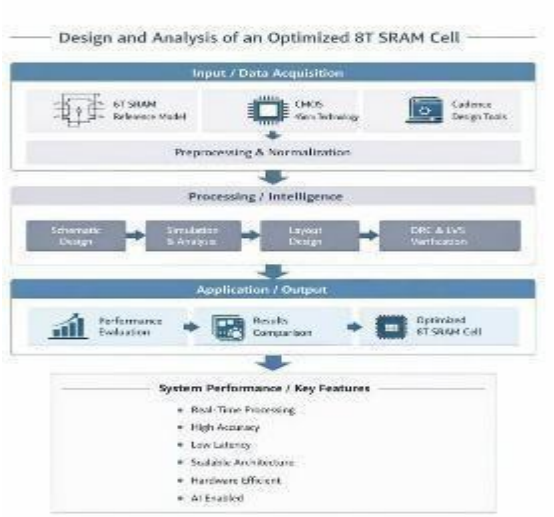

Fig. 3: Design Flow Block Diagram of the Proposed 8T SRAM Cell

A. Operation of 8T SRAM Cell

The design methodology of the proposed 8T SRAM cell is illustrated using a block diagram, which outlines the complete development flow from initial design to final performance evaluation. The process begins with understanding the limitations of the conventional 6T SRAM cell, followed by the formulation of an improved architecture. The design is implemented using 45 nm CMOS technology with the help of Cadence design tools.Initially, design parameters such as supply voltage, transistor sizing, and operating conditions are defined. The circuit is then modeled and simulated to verify its functional behavior. After successful validation at the schematic level, the layout is created while ensuring compliance with fabrication rules. Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification are performed to confirm the correctness of the layout.Finally, the proposed design is analyzed in terms of power consumption, delay, and stability. The obtained results are compared with the conventional 6T SRAM cell to evaluate performance improvements. This structured approach ensures that the design is optimized for reliability, efficiency, and scalability.

1. Hold Operation

During the hold state, both the write word line and read word line are kept at an inactive level, which turns off the associated transistors. As a result, the internal storage nodes are isolated from external connections, and the stored data is preserved through the feedback mechanism of the cross-coupled inverters. The cell remains stable in this condition, and only minimal power leakage occurs

while maintaining the stored information.

2. Write Operation

In the write operation, the write word line is enabled, allowing the internal nodes of the cell to connect with the write bit line pair. The input data to be stored is applied through these bit lines, forcing the internal nodes to switch to the desired logic state. Once the write process is completed, the word line is disabled, and the cross-coupled inverters retain the updated value.

3. Read Operation

For the read process, the read bit line is precharged before activation. When the read word line is enabled, the read path is established, and the stored value determines whether the read bit line discharges or remains at its initial level. Based on the stored value at internal node Q, the read bit line either maintains a high level or experiences a voltage drop. The sense amplifier detects this variation and identifies the stored data. Since the read path is isolated from the storage nodes, the read operation does not disturb the stored value, ensuring improved stability compared to conventional designs.

C. Advantages

The simulation results confirm that the proposed 8-transistor SRAM cell operates reliably under different input conditions. The use of separate control signals for read and write operations ensures accurate data storage and retrieval. One major advantage of this design is that the internal storage nodes remain unaffected during read access, which improves stability and prevents data corruption. Additionally, reduced switching activity leads to lower power consumption. The design also performs effectively under varying operating conditions, making it suitable for implementation in advanced CMOS technologies such as 45 nm.

VII. SIMULATION RESULTS AND WAVEFORM ANALYSIS

The transient analysis performance evaluation for the 8T SRAM cell is validated using transient analysis result s from Cadence simulations. In comparison to DC analysis, transient analysis provides a means of verifying dynamic behaviours such as switching delays and power consumption during read/write operations. Using the methodology described in the 6T SRAM paper as a reference, an analytical value has been developed for each of the 8T SRAM cell parameters

A.Delay Calculation

Propagation latency is among the key factors used to evaluate SRAM performance; it indicates how much time is required on average for the output (O) to react when the input (I) changes. For example, the delay for an 8T SRAM cell is measured from when the word lines are activated (WWL/RWL) until there is a variation at the internal storage nodes (Q and $\bar{Q}$) caused by a signal transition on the word line in the transient waveform.the data that we are writing. The special circuits then keep the data stable after the writing is finished. The fact that the reading path is means that the writing of data is not affected by the reading circuitry, which makes the memory more reliable and efficient.

The delay is calculated using the standard expression:

$$T_d = \frac{tPHL + tPLH}{2}$$

where

t_{PHL} = delay during high-to-low switching transition

t_{PLH} = delay during low-to-high switching transitionFig

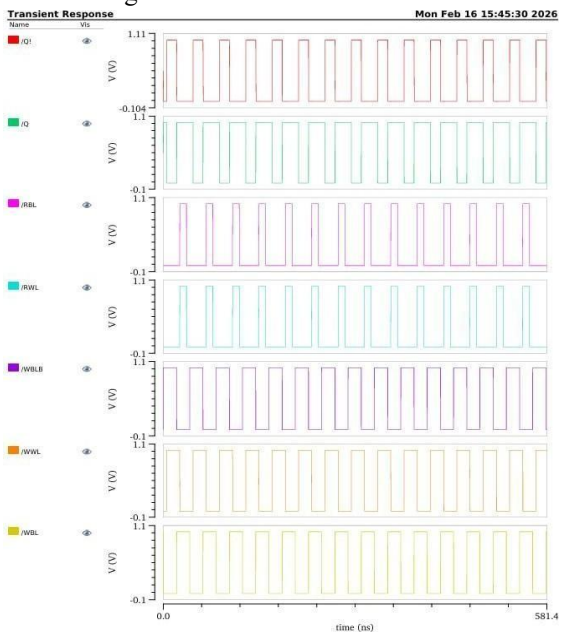

Fig.4 : Transient Response of 8T SRAM Cell

From the transient waveform, the following observations are made:

- Time at which input (word line) crosses 50% of V_{DD}: t_{in}
- Time at which output (Q or $\bar{Q}$) reaches 50% of final value: t_{out}

B.ANAVERAGE POWER CALCULATION:

The mean power dissipation of the SRAM cell is calculated over one complete switch cycle using transient waveform information (voltage and current). As discussed in the paper on 6T SRAM, the average power is defined by: P

$$P_{avg}=\frac{1}{T}\int_{0}^{T} V(t).I(t)dt$$

For CMOS circuits, dynamic power dominates and is approximated as:

$$P_{avg}= \alpha CLV_{DD}^{2} f$$

Where,

α = activity (switching) coefficient

CL = effective load capacitance

VDD = supply voltage level

f = switching frequency observed transient waveform:

Supply voltage VDD≈1.

Time period T≈581.4 ns⇒f≈1.72 MHz

The average instantaneous power is computed with simulation tools by extracting and performing the same calculations performed with an actual test. The comparison is based on computation of average power of 6T SRAM. Therefore, average power calculated from the average of instantaneous waveform based values:

Pavg≈420μW

Compared to 6T SRAM, notable improvement in power efficiency due to the following factors:

Independent read and write paths,Reduced switching activity on bit lines during read cycles,Significantly lower dynamic power consumption due to minimized disturbance through isolation of internal storage nodes during read and write operations.As demonstrated through transient analysis, the 8T SRAM cell outperforms the 6T design. The 8T cell is capable of maintaining an acceptable delay (~23 ns) while also consuming less power compared to the 6T design.

VIII. COMPARISION

The table I presents a comparison between the conventional 6T SRAM cell and the proposed 8T SRAM cell with respect to three major aspects: read stability, average power, and reliability. Each of these aspects shows noticeable enhancement in the proposed design. A key drawback of the conventional 6T SRAM cell is that the internal storage nodes along with their corresponding bit lines remain directly connected during read operations, which can introduce disturbances and degrade the stored data, particularly at lower voltage levels. The proposed 8T SRAM cell differs from the traditional 6T SRAM cell in that it incorporates a dedicated read path, which provides electrical isolation between the storage nodes and the read bit line, thereby eliminating read disturbance and improving overall cell stability. Consequently, the static noise margin of the 8T SRAM cell is significantly higher compared to the conventional 6T SRAM cell due to the separation of read and write operations, which reduces noise coupling and mitigates the effects of process variations. Therefore, the reliability of the 8T SRAM cell in deep submicron technologies such as 45 nm is considerably better than that of the conventional 6T SRAM cell. In addition, the dynamic power consumption of the 8T SRAM architecture is lower than that of the traditional 6T SRAM design because of reduced switching activity between internal storage nodes and external circuitry during read operations. This also helps in minimizing

Attributes	Conventional 6T Memory Cell	Proposed 8T Memory Cell
Cell Structure	The 6T SRAM cell consists of six transistors configured as two cross-coupled inverters and two access transistors used during both data access and write processes.	The proposed 8T SRAM cell consists of a 6T memory core along with two additional transistors that provide an independent sensing path for enhanced operation.
Read and Write Path	Within the 6T SRAM cell, both data access and write operations share the same access path, which leads to interference during operation.	Within the proposed 8T SRAM cell, data access and write operations are separated, which eliminates interference and improves reliability.
Read Stability	The data access stability is low due to the direct connection of storage nodes to the bit lines, which may disturb stored data.	The data access stability is high as the storage nodes are isolated from the sensing bit line, preventing disturbance during data retrieval.
	The write operation depends on the capability of	The write operation is more reliable due to the

Write Operation	access transistors to overcome the inverter feedback, which becomes challenging in scaled technologies.	absence of sensing path interference and improved transistor control.
Static Noise Margin (SNM)	The SNM is lower, especially during read operation, due to noise coupling from bit lines.	The SNM is higher because of improved isolation and reduced noise interference.
Power Consumption	The power consumption is higher due to simultaneous switching activity and leakage in shared paths.	The power consumption is reduced due to separate read path and minimized switching activity.
Leakage Current	Leakage current is relatively higher due to direct interaction between internal storage nodes and the bit lines.	Leakage current becomes lower due to reduced interaction between storage nodes and external nodes.
Area Requirement	The area requirement is smaller since fewer transistors are used.	The area requirement is slightly higher due to the addition of two transistors for read operation.
Performance	The overall performance is moderate due to limitations in stability and power efficiency.	The performance is improved with better stability, lower power consumption, and enhanced reliability.
Suitability	Suitable for applications where area is a constraint but stability is less critical.	Well-suited for energy-efficient and high-speed applications where stability and reliability are essential.

IX. CONCLUSION

In this project, an 8-Transistor SRAM cell was analyzed using CMOS technology with the support of Cadence Virtuoso tools. The proposed design outperforms the conventional 6-Transistor SRAM structure because it includes two additional transistors that create an independent read path. This modification helps separate read and write operations, thereby resolving issues present in traditional 6T SRAM cells, such as read disturbance and reduced stability at smaller technology nodes.A design of the 8-Transistor SRAM cell was implemented and tested with various input conditions to evaluate its functionality. The simulation results indicate that the 8T SRAM cell operates correctly during hold, read, and write modes. During write operation, the cell stores input data by allowing the write access transistors to control the feedback mechanism of the cross-coupled inverters. During read operation, the precharged read bit line discharges based on the stored value without disturbing the internal storage nodes. This demonstrates a key advantage of the 8T SRAM architecture, where the storage nodes remain fully isolated from the read path.Further analysis was carried out to evaluate the performance of the 8T SRAM cell in terms of power consumption, delay, and stability. The obtained results indicate that the proposed 8T SRAM design provides improved data retention during read operations, as the internal nodes are not directly connected to the bit lines. This leads to an increase in Static Noise Margin, making the cell more tolerant to noise and process variations.Additionally, dynamic power consumption is reduced because switching activity at the storage nodes is minimized during read operations. Although the 8T SRAM cell occupies slightly more area than the conventional 6T cell due to the additional transistors, this trade-off is justified by the significant improvements in performance and reliability. The reduction in leakage current and enhancement in stability make this design suitable for low-power and high-speed applications in modern VLSI systems.The overall process of designing, simulating, and verifying the 8T SRAM cell using Cadence tools provides valuable insight into practical VLSI design methodologies. The results clearly demonstrate that as technology scales down (e.g., 45 nm and below), advanced SRAM architectures such as the 8T design become essential for maintaining performance, stability, and power

efficiency.In conclusion, the proposed 8-Transistor SRAM cell shows superior performance compared to the conventional 6T SRAM cell in terms of read stability, energy efficiency, and reliability. Therefore, it can be considered a strong candidate for future memory designs in advanced CMOS technologies. Future work may focus on extending this design for large memory arrays, optimizing layout structures, and analyzing the effects of noise and process variations. Further improvements can also be explored for smaller technology nodes such as 32 nm and 22 nm to achieve enhanced performance in next-generation memory systems.

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