Implementation of PMOS Biased Sense Amplifier

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***Abstract*—Sense amplifiers are critical components in SRAM memory systems that detect and amplify small voltage variations developed on memory bit-lines during read operations. The sense amplifier's stability, power consumption, and sensing speed all have a significant impact on SRAM performance. This study used 180 nm CMOS technology in the Cadence Virtuoso environment to develop and execute two PMOS-biased sense amplifier circuits. The suggested circuits' sensing delay, waveform stability, and regenerative behavior were assessed in both standalone and SRAM-connected scenarios. The practical performance of the suggested architectures was investigated through transient and post-layout simulations. For high-speed and low-power SRAM applications, the results show enhanced sensing operation, dependable output production, and decreased sensing delay.**

I. INTRODUCTION

Modern digital systems frequently use static random-access memory (SRAM) due to its fast speed, low latency, and dependable operation. When quick data access is needed, SRAM is crucial for microprocessors, digital signal processors (DSPs), and cache memory. In contrast to DRAM, SRAM uses bistable-latching circuits to store data and does not need to be refreshed on a regular basis.

Very tiny voltage variations emerge on the SRAM cell's bit lines during memory read operations. Digital circuits are unable to immediately detect these tiny signals. For dependable data retrieval, sense amplifiers are employed to detect and magnify these minute fluctuations into full-logic levels.

Memory circuits encounter a number of difficulties when CMOS technology advances into deep submicron regions, including bit-line capacitance effects, higher power consumption, sensing delay, and leakage current. The SRAM system's total performance is lowered by these restrictions. As a result, creating a high-speed, low-power sense amplifier is now crucial for contemporary VLSI systems.

In this study, Cadence Virtuoso's 180 nm CMOS technology was used to implement and analyse two PMOS-biased sense amplifier circuits. Sensing delay, regenerative operation, waveform stability, and SRAM loading behaviour were used to assess the suggested circuits.

The bit lines are first precharged during operation. The sense amplifier produces complementary outputs by detecting the differential current produced by the SRAM cell and converting it into voltage when the enable signal is enabled.

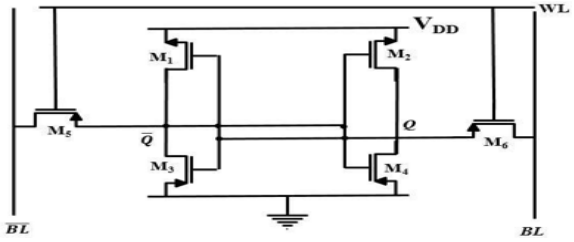


Figure 1 SRAM Architecture

II. PROPOSED SYSTEM

The proposed system consists of two PMOS-biased sense amplifier circuits designed for SRAM read operations. The objective of the proposed design is to reduce the sensing delay and improve the sensing reliability while maintaining low power consumption.

Proposed Circuit-1

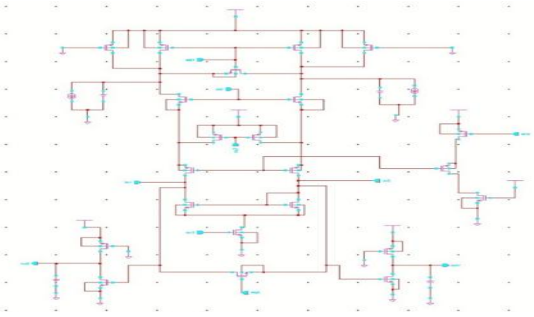


Figure 2 Schematic of current based sense amplifier circuit-1

Circuit 1 is a PMOS-biased sensing amplifier that operates on current. PMOS transistors are used in the circuit for differential current sensing and recharging. The inverter stages coupled across the load capacitance provides the outputs. The suggested design enhances signal amplification during the read operation and lowers the sensing delay.
The bit lines are first precharged during operation. The sense amplifier produces complementary outputs by detecting the differential current produced by the SRAM cell and converting it into voltage when the enable signal is enabled.

Proposed Circuit-2
Circuit-2 is a PMOS sensing amplifier with a latch that operates by regenerative positive feedback. The circuit combines the benefits of a latch-based sensor mechanism with a differential amplifier. The latch mechanism produces full-swing outputs by quickly amplifying the tiny voltage variations on the bit lines. When compared to traditional sensing circuits, the suggested latch-based topology enhances the waveform stability, sensing reliability, and SRAM loading tolerance.

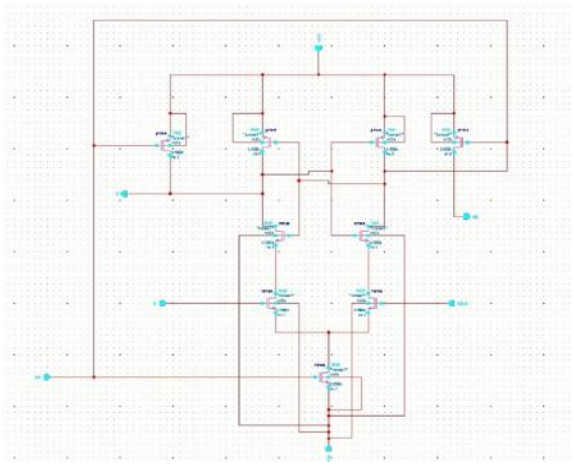


Figure 3 Schematic of latch-based sense amplifier circuit -2

III. METHODOLOGY

Using Cadence Virtuoso in 180 nm CMOS technology, the suggested sense amplifier circuits were created and simulated. Schematic design, transient simulation, layout design, parasitic extraction, and post-layout verification comprised the implementation procedure.

Initially, CMOS transistors with ideal transistor size were used in the schematic design of both sense amplifier circuits. The transistors' width/length (W/L) ratio was kept at 2µm/0.18µm for optimal sensing performance.
Transient simulations were used to study sensor delay, waveform stability, and regenerative functionality. Both solo and SRAM-connected setups were used to evaluate the effects of the memory loading conditions. The suggested circuits' layouts were created using the standard CMOS layout guidelines for practical verification. To make sure the layout was correct, Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks were carried out.
In order to decrease the sensing delay and enhance signal amplification during SRAM read operations, the suggested Circuit-1 is a PMOS-biased current-based sense amplifier. PMOS transistors are used in the circuit for differential current sensing and bit-line precharging. To assess the sensing performance and waveform stability, transient simulations were run in both standalone and SRAM-connected scenarios.

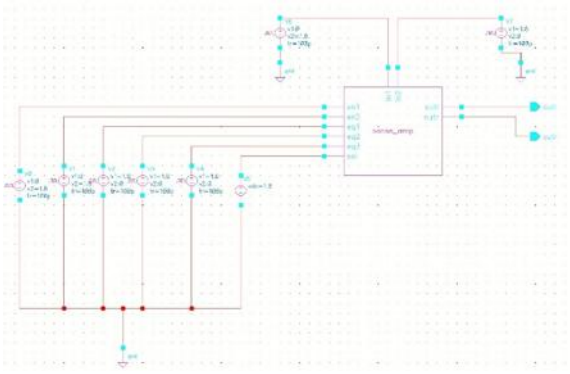


Figure 4 Test schematic of current based sense amplifier circuit-1 without memory

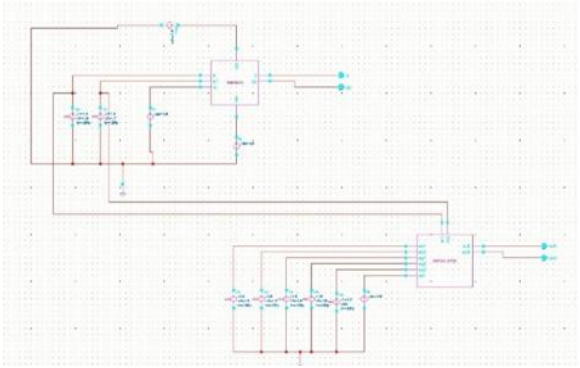


Figure 5 Test schematic of current based sense amplifier circuit-1with memory

Circuit-2 uses regenerative positive feedback operation in a latch-based PMOS sense amplifier architecture. The latch structure produces full-swing outputs by quickly amplifying tiny differential voltages formed on the bit-lines. In order to investigate sensing reliability and regeneration behavior, the circuit was examined both under memory-loaded and standalone situations. Under SRAM loaded situations, the latch-based topology increased sensor reliability and output voltage swing.

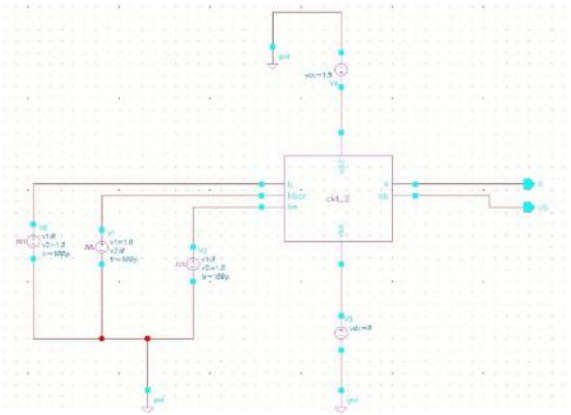


Figure 6 Test schematic of latch-based sense amplifier circuit-2 without memory

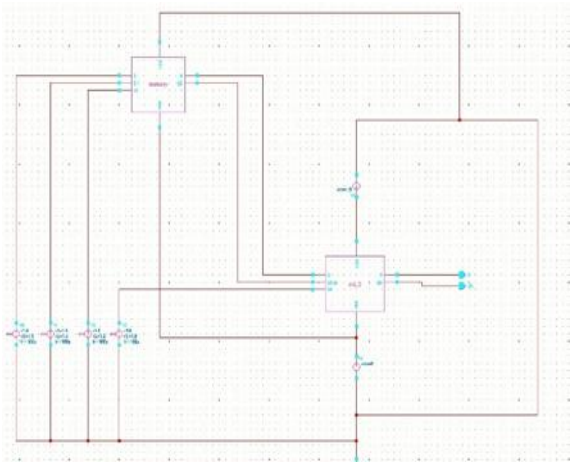


Figure 7 Test schematic of latch-based sense amplifier circuit-2 with memory

The layouts of the proposed circuits were designed using Cadence Virtuoso following standard 180nm CMOS design rules. Design Rule Check (DRC), Layout Versus Schematic (LVS), and parasitic extraction were performed to validate the physical implementation and analyze post-layout performance

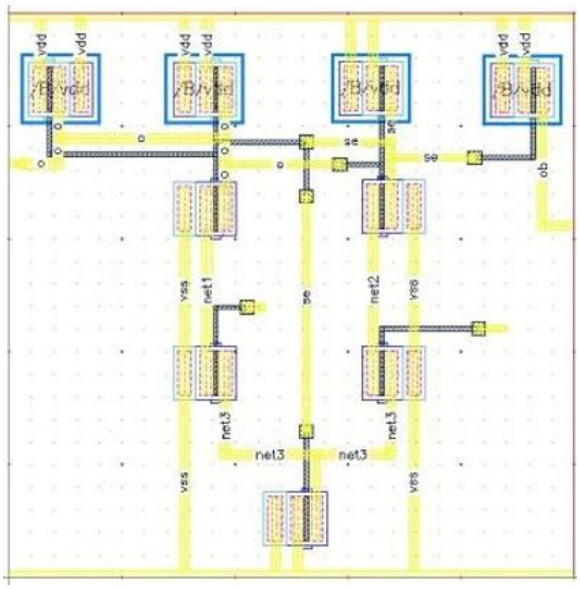


Figure 8 Layout of latch-based sense amplifier circuit-2

Both current based amplifier and latch-based amplifier were analyzed under these operating conditions, and the corresponding test schematics, waveforms, and delay measurements were obtained through transient simulation

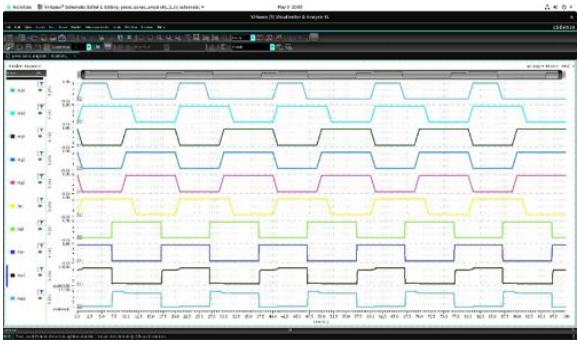


Figure 9 Waveform of Test schematic ofcurrent based sense amplifier circuit-1 without memory

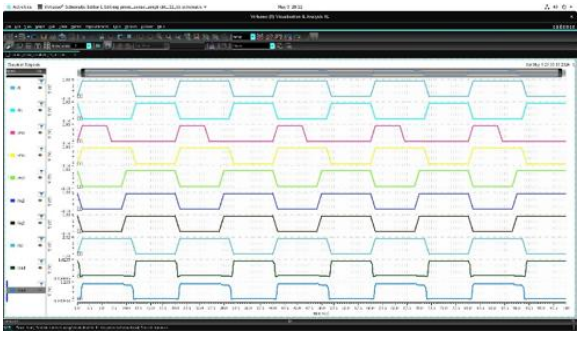
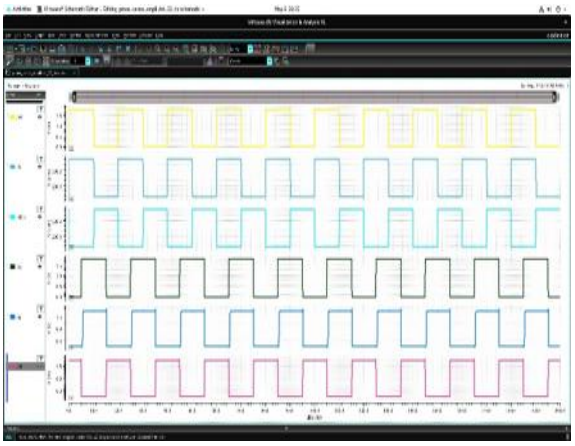


Figure 10 Waveform of Test schematic of current based sense amplifier circuit-1 with memory

Figure 11 Waveform of Test schematic of latch-based sense amplifier circuit-2 without memory



12 Waveform of Test schematic of latch-based sense amplifier circuit-2 with memory

IV. RESULTS

Cadence Virtuoso was used to model the suggested sense amplifier circuits utilizing 180nm CMOS technology. For both circuits, the transient responses verified steady output transitions and appropriate sensing functionality.

Circuit-1 current based sense amplifier displayed faster sensing operation due to lower capacitive loading and simpler form. For Circuit-1 with memory, the measured sensing latency was roughly 440.456 ps, whereas it was 551.87 ps without memory.

Circuit-2's latch-based positive feedback mechanism demonstrated enhanced regenerative operation and waveform stability. With memory, Circuit-2's sensing delay was roughly 10.428 ns; without memory, whereas 10.164 ns with memory.

Result Table

Circuit Configuration	Input Signal	Output Signal	Measured Delay
Current based sense amplifier without memory	EN1	OUTL	551.87 ps
Current based sense amplifier with memory	EN/SEL	OUTL	440.456 ps
Latch based sense amplifier without memory	SE	A	10.428 ns
Latch based sense amplifier with memory	SE	A	10.164 ns

Performance Comparison

Parameter	Current based sense amplifier	Latch based sense amplifier
Regenerative Operation	Moderate	Strong
Output Voltage Swing	Moderate	Full Swing
SRAM Loading Stability	Good	Better
Sensing Speed	Faster	Moderate
Positive Feedback	No	Yes

To evaluate the performance of the proposed circuits, two test cases were considered:

- Simulation with SRAM memory connection
- Simulation without SRAM memory connection

The memory-connected configuration was used to analyze practical sensing behavior under SRAM loading conditions and bit-line capacitance effects. The standalone configuration without memory was used to analyze the intrinsic sensing characteristics of the sense amplifier circuits without loading effects.

V. CONCLUSION

Using 180nm CMOS technology in Cadence Virtuoso, two PMOS biased sense amplifier circuits were successfully developed and built in this work. Both circuits' proper sensing operation was confirmed by the transient simulation and post-layout data.

While Circuit-2's latch-based sense amplifier offered superior regenerative operation, greater waveform consistency, and dependable sensing performance under SRAM loading situations, Circuit-1's current-based sense amplifier produced faster sensing speed

with less delay. Through positive feedback operation, Circuit-2's latch-based architecture improved output voltage swing and sensor reliability.

The suggested sense amplifier designs showed efficient low-power and high-performance features appropriate for high-speed memory and SRAM applications. The experiment demonstrates how crucial optimised sense amplifier design is for enhancing memory system performance as a whole.

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