Design and FPGA Implementation of a Parameterized Synchronous FIFO Using Verilog HDL and TCL-Based Automation in Xilinx Vivado

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***Abstract*—First-In First-Out (FIFO) memory structures play a vital role in modern digital systems by providing temporary data storage and synchronization between modules operating at different processing rates. This paper presents the design, implementation, and hardware validation of a parameterized synchronous FIFO using Verilog Hardware Description Language (HDL) on the EDGE Artix-7 FPGA development board. The proposed FIFO architecture supports configurable data width and memory depth, enabling scalability and flexibility for various FPGA-based applications. The FIFO design incorporates dedicated read and writes pointer management, full and empty status flag generation, and a Finite-State-Machine (FSM)-based debounce circuit for reliable push-button operation during hardware testing. The complete FPGA development workflow is automated using Tool Command Language (TCL) scripting in Xilinx Vivado, allowing project creation, source integration, synthesis, implementation, bitstream generation, report extraction, and FPGA programming through command-line execution. Functional verification is performed through simulation, while hardware validation is carried out using onboard switches, push buttons, and LEDs. Synthesis and implementation results demonstrate successful FIFO operation with efficient resource utilization and reliable data transfer.**

***Index Terms*—FIFO, FPGA, Verilog HDL, Xilinx Vivado, TCL Scripting, Artix-7, Synchronous FIFO, Hardware Automation, Digital Design, Memory Buffer.**

I. INTRODUCTION

Modern digital systems require efficient mechanisms for temporary data storage and transfer between pro-cessing modules operating at different speeds. The First-In First-Out (FIFO) memory structure is one of the most widely adopted buffering techniques. FIFO memories ensure that data is retrieved in the same order it is stored, making them essential in communication systems, embedded platforms, processors, digital signal processing, and FPGA-based designs.

Field Programmable Gate Arrays (FPGAs) have become the preferred platform for implementing digital sys-tems due to their reconfigurability, parallel processing capability, and reduced development time. Verilog HDL enables parameterized FIFO architectures customized to application requirements. Additionally, Xilinx Vivado supports Tool Command Language (TCL) scripting, which automates the complete design flow from project cre-ation to hardware deployment, improving reproducibility and reducing manual effort [1].

A. Background and Motivation

The increasing demand for high-speed data processing has created a need for reliable buffering mechanisms. FIFO memories serve as intermediate storage between data producers and consumers, ensuring smooth communi-cation. Traditional software-based buffering introduces additional latency and processing overhead. FPGA-based FIFO implementations overcome these limitations using dedicated hardware resources. The motivation behind this work is to develop a parameterized FIFO capable of efficient hardware implementation while demonstrating the advantages of TCL-based automation in Vivado.

B. Problem Statement

Designing reliable FIFO systems requires efficient management of memory locations, read and write pointers, and status indicators such as full and empty

flags. Incorrect pointer synchronization leads to data corruption, overflow, or underflow. Additionally, manual FPGA development through GUIs is repetitive and time-consuming, particularly when synthesis, implementation, and deployment must be repeated across iterations. There is there-fore a need for an automated, scalable FIFO design methodology that combines parameterized Verilog HDL with TCL-based automation.

C. Objectives

The primary objectives of this work are:

- Design and implement a parameterized synchronous FIFO using Verilog HDL.
- Develop configurable memory storage with programmable data width and address space.
- Implement read/write pointer management with full and empty status flag generation.
- Integrate an FSM-based debounce circuit for reliable push-button operation.
- Automate the complete FPGA development flow using TCL scripting in Xilinx Vivado.
- Verify functionality through simulation and validate on the EDGE Artix-7 board.
- Evaluate the practicality of combining Verilog design with TCL-driven automation.

D. Organization of the Paper

Section II presents the literature review. Section III discusses the system architecture and design methodol-ogy. Section IV explains the Verilog HDL implementation. Section V describes the TCL-based automation flow. Section VI presents simulation, synthesis, and hardware results. Section VII concludes the paper.

II. LITERATURE REVIEW

FIFO memories are fundamental components in digital systems, extensively used in communication interfaces, processor architectures, embedded systems, and FPGA-based designs. Their primary purpose is to provide tempo-rary data storage while preserving the order of information transfer between producer and consumer modules [6]. Early FIFO implementations relied on dedicated memory circuits with simple pointer-based control. These designs were efficient but lacked flexibility. With programmable logic devices, FIFO architectures began to be implemented using Verilog and VHDL, enabling configurable structures for various applications [5]. Synchronous FIFOs employ a common clock for both read and write operations, reducing synchronization complexity and minimizing timing issues making them widely adopted in real-time systems.

Parameterized FIFO designs improve reusability, allowing a single architecture to serve multiple applications. FPGA vendors such as Xilinx and Intel provide dedicated memory resources and optimization techniques (e.g., distributed RAM inference) that facilitate efficient FIFO implementation [4]. TCL scripting has emerged as an effective solution for automating FPGA workflows, improving productivity and ensuring consistent results [3]. FSM-based debounce circuits provide robust noise filtering for reliable hardware interaction with mechanical switches [2].

Although numerous FIFO implementations have been reported, limited work combines parameterized FIFO design, FSM-based debouncing, FPGA hardware validation, and TCL-based automation within a single unified framework. The present work addresses this gap by integrating all these aspects using Verilog HDL and Xilinx Vivado 2022.2.

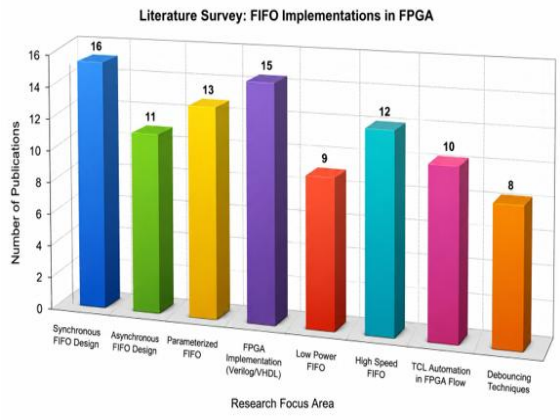

Figure 1: graph of the literature survey

III. PROPOSED SYSTEM ARCHITECTURE

The proposed system implements a parameterized synchronous FIFO on the EDGE Artix-7 FPGA (xc7a35tftg256-1) using Verilog HDL with TCL-based automation. The design hierarchy consists of three modules:

- fifo test Top-level integration module.
- debounce explicit ×2 FSM-based button debounce

for write (wr) and read (rd).

- fifo Parameterized circular buffer (DATA SIZE=3, ADDR SPACE EXP=2, depth=4)

A. FIFO Architecture

The FIFO controller implements synchronous read and write operations controlled by a common 100 MHz system clock. The architecture consists of: a parameterized memory array (inferred as distributed RAM); a write pointer (current write addr) that advances on each valid write; a read pointer (current read addr) that advances on each valid read; and full/empty status flags driven by pointer comparison logic.

The prototype uses DATASIZE = 3(3-bit data width) and ADDRSPACEEXP = 2(4 memory locations).

Input data is supplied via FPGA slide switches.

B. Pointer and Status Logic

The write pointer advances when the FIFO is not full and a write request is asserted. The read pointer advances on a valid read operation. The Empty flag asserts after reset and when the read pointer catches up to the write pointer following a read. The Full flag asserts when the write pointer catches up to the read pointer following a write. These flags prevent overflow and underflow while maintaining data integrity.

C. Debounce Circuit

The FSM-based debounce module implements a 4-state FSMD: zero → wait1 → one → wait0. A 22-bit decrement counter (N = 22) provides approximately 42 ms settling time at 100 MHz, ensuring exactly one clean db tick pulse per button press regardless of mechanical bounce duration.

D. Hardware Platform

The EDGE Artix-7 FPGA development board provides: three slide switches (sw [2:0]) for 3-bit data input; push buttons btnC (reset), btnU (write), btnD (read); and on-board LEDs for data out [2:0], full (LED15), and empty (LED0). All I/O standards are LVCMOS33.

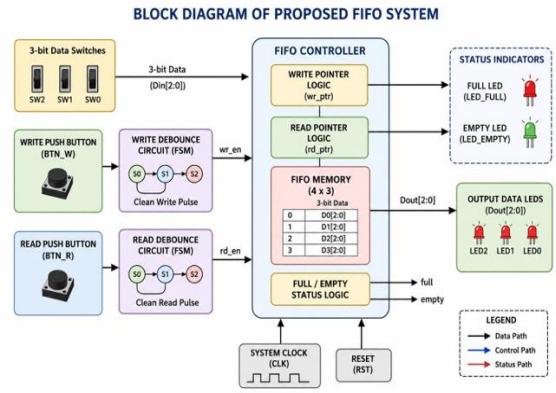

Figure 2: Block Diagram of the FIFO Memory). FULL=0 and EMPTY=1 persist until debounce tick fires.

IV. VERILOG HDL IMPLEMENTATION

a. FIFO Module (fifo.v)

The parameterized FIFO module is coded with DATA SIZE and ADDR SPACE EXP parameters. The memory array is inferred as distributed RAM (RAM32M primitive) by Vivado. Read is combinational (zero-latency);

write is clocked and gated by the writeenabledsignal. The control logic uses caseon {writetofifo, read from fifo} to handle all four input combinations.

```
module fifo
  #(parameter DATA_SIZE      = 8,
              ADDR_SPACE_EXP = 4)
   (input  clk, reset,
    input  write_to_fifo, read_from_fifo,
    input  [DATA_SIZE-1:0] write_data_in,
    output [DATA_SIZE-1:0] read_data_out,
    output empty, full);

  reg [DATA_SIZE-1:0] memory [2**ADDR_SPACE_EXP-1:0];

  // Combinational read      zero latency
  assign read_data_out = memory[current_read_addr];

  // Write only when FIFO is not full
  assign write_enabled = write_to_fifo & ~fifo_full;

  always @(posedge clk)
    if (write_enabled)
      memory[current_write_addr] <= write_data_in;
```

Listing 1: FIFO Module Port Declaration and Key Logic

b. Debounce Module (debounce explicit.v)

```
parameter [1:0]
  zero  = 2'b00, wait1 = 2'b01,
  one   = 2'b10, wait0 = 2'b11;

// N=22 gives ~42 ms debounce at 100 MHz
parameter N = 22;
reg [N-1:0] q_reg;    // countdown counter
```

Listing 2: Debounce FSM State and Counter Declaration

The dbtickoutput pulses high for exactly one clock cycle on confirmed button press, triggering precisely one FIFO transaction.

c. Top-Level Module (fifo test.v)

```
fifo #(.DATA_SIZE(3), .ADDR_SPACE_EXP(2))
  fifo_unit(
    .clk(clk_100MHz), .reset(reset),
    .write_to_fifo(write),
    .read_from_fifo(read),
    .write_data_in(sw),
    .read_data_out(data_out),
    .full(full), .empty(empty));
```

Listing 3: Top-Level Instantiation

d. XDC Constraint File

Table 1 summarizes key pin assignments for the xc7a35tftg256-1 device.

Signal	Pin	Signal	Pin
clk_ 100MHz	W5	reset (btnC)	U18
sw[0]	V17	wr (btnU)	T18
sw[1]	V16	rd (btnD)	U17
sw[2]	W16	empty (LED0)	U16
data_out[0]	U15	data out[1]	U14
data_out[2]	V14	full (LED15)	L1

Table 1: Key XDC Pin Assignments

V. TCL-BASED DESIGN AUTOMATION

TCL scripting automates the entire FPGA design flow in Xilinx Vivado, replacing repetitive GUI operations with command-line execution. This improves reproducibility, reduces development time, and enables batch-mode compilation.

A. Project Creation and Source Integration

```
create_project fifo_project ./fifo_project \
  -part xc7a35tcpg236-1

add_files fifo.v add_files
fifo_test.v
add_files debounce_explicit.v add_files
-fileset constrs_1 fifo.xdc

set_property top fifo_test [current_fileset]
update_compile order -fileset sources 1
```

Listing 4: Project Creation and Source Import

B. Synthesis, Implementation, and Bitstream

```
# Run synthesis
launch_runs synth_1
wait_on_run synth_1

# Run implementation
launch_runs impl_1
wait_on_run impl_1

# Generate bitstream
launch_runs impl_1 -to_step write_bitstream
wait_on_run impl_1
write_bitstream -force fifo.bit
```

Listing 5: Synthesis and Implementation Commands

C. Hardware Programming via TCL

```
open_hw_manager
connect_hw_server
open_hw_target
current_hw_device [lindex [get_hw_devices] 0]
set_property PROGRAM.FILE fifo.bit \
  [current_hw_device]
program_hw_devices [current_hw_device]
```

Listing 6: FPGA Programming Through Vivado Hardware Manager

D. Report Generation

```
report_utilization -file utilization_report.rpt
report_timing_summary -file timing_report.rpt
```

Listing 7: Automated Report Generation

E. Advantages of TCL Automation

i. Eliminates repetitive manual GUI operations.
ii. Ensures reproducible implementation results.
iii. Accelerates FPGA development cycles.
iv. Enables automated report generation and analysis.
v. Simplifies project migration across different systems.
vi. Supports batch-mode and scripted FPGA compilation.

VI. SIMULATION, SYNTHESIS AND HARDWARE RESULTS

A. Functional Simulation

Behavioral simulation was performed in Xilinx Vivado 2022.2 using the fifo test tb testbench. The simulation runs for 1000 ns at 1 ps resolution, applying sequential write operations (values 0–4) followed by reads.

Fig. 3 shows the Vivado waveform. The simulation confirms:

vii. Empty flag (value 1) deasserts upon the first writes operation.
viii. Full flag asserts when all four memory locations are occupied.
ix. dataoutreflects the first-written value upon read.
x. Empty flag reasserts after all entries are drained.
xi. Switch data values 0, 1, 2, 3 are correctly captured in sequence.

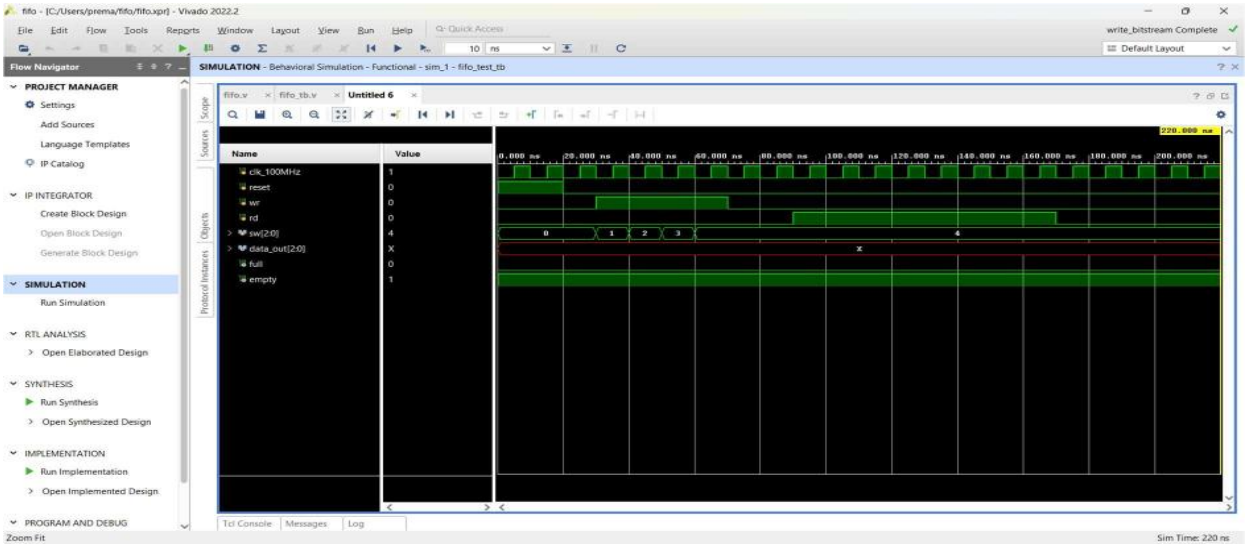

Figure 3: Vivado Behavioral Simulation Waveform FIFO Read/Write Transactions (clk, reset, wr, rd, sw[2:0], data out [2:0], full, empty)

Fig. 4 shows the TCL simulation console output confirming correct signal transitions at each timestep.

```
#     add_wave /
#     set_property needs_save false [current_wave_config]
#   } else {
#     send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File
->New Waveform Configuration' or type 'create_wave_config' in the TCL console."
#   }
# }
# run 1000ns
Time=0 WR=0 RD=0 SW=000 DATA_OUT=xxx FULL=0 EMPTY=1
Time=30000 WR=1 RD=0 SW=001 DATA_OUT=xxx FULL=0 EMPTY=1
Time=40000 WR=1 RD=0 SW=010 DATA_OUT=xxx FULL=0 EMPTY=1
Time=50000 WR=1 RD=0 SW=011 DATA_OUT=xxx FULL=0 EMPTY=1
Time=60000 WR=1 RD=0 SW=100 DATA_OUT=xxx FULL=0 EMPTY=1
Time=70000 WR=0 RD=0 SW=100 DATA_OUT=xxx FULL=0 EMPTY=1
Time=90000 WR=0 RD=1 SW=100 DATA_OUT=xxx FULL=0 EMPTY=1
Time=170000 WR=0 RD=0 SW=100 DATA_OUT=xxx FULL=0 EMPTY=1
$stop called at time : 220 ns : File "C:/Users/prema/AppData/Roaming/Xilinx/Vivado/fifo2/tb/fifo2_tb.v" Line 1
INFO: [USF-XSim-96] XSim completed. Design snapshot 'fifo_test_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:00 ; elapsed = 00:00:19 . Memory (MB): peak = 429.062 ; gain = 8.129
Vivado%
```

Figure 4: TCL Simulation Console Output Signal Values at Each Timestep (0–170000 ns). FULL=0 and EMPTY=1 persist until debounce tick fires.

B. RTL Synthesis Results

RTL synthesis targeted the xc7a35tftg256-1 device. Fig. 5 shows the detailed RTL component statistics from the Vivado TCL console.

```
Vivado 2022.2 Tcl Shell - C:\Xi
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
         2 Input   22 Bit       Adders := 2
         2 Input    2 Bit       Adders := 2
+---Registers :
                    1 Bit    Registers := 2
+---RAMs :
                   12 Bit   (4 X 3 bit)          RAMs := 1
+---Muxes :
         2 Input   22 Bit        Muxes := 2
         3 Input    2 Bit        Muxes := 2
         2 Input    2 Bit        Muxes := 6
         2 Input    1 Bit        Muxes := 4
         3 Input    1 Bit        Muxes := 12
         4 Input    1 Bit        Muxes := 6
---------------------------------------------------------------------------------
Finished RTL Component Statistics
```

Figure 5: RTL Component Statistics from Vivado Synthesis FIFO Module (Adders, Registers, Distributed RAM, Multiplexers)

Table 2 summarizes the RTL components. The FIFO memory is inferred as a single RAM32M (4×3-bit distributed RAM), confirming efficient mapping with no DSP slices or block RAMs required.

Table 2: RTL Component Statistics FIFO Module

Resource	Type	Detail	Count
Adders	2-Input	22-bit	2
Adders	2-Input	2-bit	2
Registers	1-bit		2
RAM (Dist.)	12-bit	4×3 bit	1
Muxes	2-Input	22-bit	2
Muxes	3-Input	2-bit	6
Muxes	2-Input	1-bit	4
Muxes	3-Input	1-bit	12
Muxes	4-Input	1-bit	6

Fig. 6 shows the Distributed RAM Final Mapping Report from Vivado, confirming the RAM32M inference for the fifo unit/memory regobject.

```
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:16 ; elapsed = 00:00:16 . Memory (MB): peak = 1345.641 ; gain = 548.652
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:16 ; elapsed = 00:00:16 . Memory (MB): peak = 1345.641 ; gain = 548.652
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start ROM, RAM, DSP, Shift Register and Retiming Reporting
---------------------------------------------------------------------------------

Distributed RAM: Final Mapping Report
+------------+-----------------------+-----------+----------------------+-------------+
|Module Name | RTL Object            | Inference | Size (Depth x Width) | Primitives  |
+------------+-----------------------+-----------+----------------------+-------------+
|fifo_test   | fifo_unit/memory_reg | Implied   | 4 x 3                | RAM32M x 1  |
+------------+-----------------------+-----------+----------------------+-------------+

---------------------------------------------------------------------------------
Finished ROM, RAM, DSP, Shift Register and Retiming Reporting
```

Figure 6: Vivado Distributed RAM Final Mapping Report RAM32M (4×3, Implied) Inference for fifo unit/memory reg

C. Cell Utilization After Implementation

Table 3 presents the complete post-implementation cell utilization report.

Table 3: Cell Utilization Complete fifo test Design

#	Cell	Count
1	BUFG	1
2	CARRY4	24
3	LUT1	42
4	LUT2	1
5	LUT3	48
6	LUT4	63
7	LUT5	5
8	LUT6	5
9	RAM32M	1
10	FDCE	1
11	FDPE	1
12	IBUF	7
13	OBUF	5

D. Timing and Routing Results

The implementation achieves:

i. Total routed nets: 147, Failed nets: 0, Unrouted: 0.
ii. Global Vertical Routing Utilization: 0.0163%.
iii. Global Horizontal Routing Utilization: 0.0349%.
iv. Node overlaps: 0. Congested regions: None (all four directions).
v. Timing: 0 errors, 0 critical warnings, synthesis completed in ~12 s.

E. Hardware Validation on FPGA Board

The bitstream was programmed onto the EDGE Artix-7 board via JTAG using the Vivado Hardware Manager (TCL-automated). Hardware validation proceeded as follows:

1. Reset (btnC): LED0 (empty) illuminates; all data LEDs off.
2. Write (btnU): Data set via switches; LED0 extinguishes after first write.
3. Full condition: After four writes, LED15 (full) illuminates.
4. Read (btnD): data out LEDs display FIFO-ordered data correctly.
5. Empty condition: After four reads, LED0 reasserts.

Fig. 7 shows the board during the initial empty state. LED0 is illuminated confirming the FIFO is empty after reset.

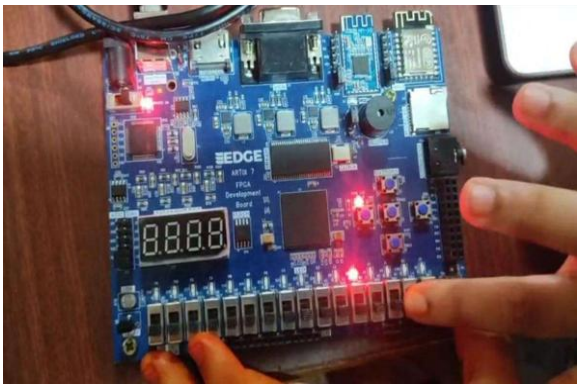

Figure 7: EDGE Artix-7 FPGA Board FIFO Empty State: LED0 (empty flag) illuminated, data output LEDs inactive

Fig. 8 shows the board during active write operations with data LEDs reflecting the written values.

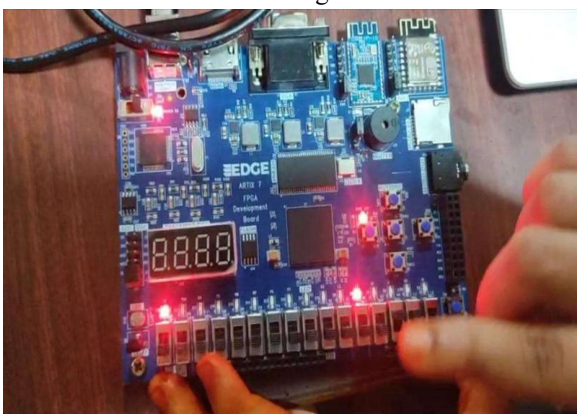

Figure 8: EDGE Artix-7 FPGA Board Write Operations in Progress: data out LEDs displaying output values; empty flag deasserted

Fig. 9 shows the FIFO in the full state, with multiple data LEDs and the full flag LED active simultaneously.

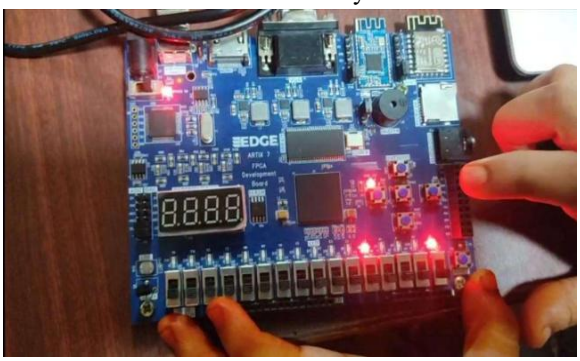

Figure 9: EDGE Artix-7 FPGA Board FIFO Full State: Multiple data LEDs illuminated, full flag LED active

The debounce circuit ensures each button press triggers exactly one FIFO transaction, confirmed by consistent single-step LED changes during testing.

VII. CONCLUSION

This paper has presented the complete design, simulation, synthesis, and FPGA hardware implementation of a parameterized synchronous FIFO memory using Verilog HDL on a Xilinx Artix-7 FPGA. The FIFO employs a circular buffer architecture with read/write address pointers and full/empty status flag logic. An FSM-based debounce module eliminates button bounce to ensure clean single-pulse control. The entire FPGA development workflow was fully automated using TCL scripting in Xilinx Vivado 2022.2.

Functional simulation confirmed correct data ordering and flag behavior. Synthesis results demonstrated compact resource utilization with the FIFO memory mapped to a single RAM32M distributed RAM primitive. Imple-mentation achieved zero timing violations, zero routing failures, and extremely low routing utilization (<0.035%). Physical hardware demonstration on the EDGE Artix-7 board validated correct FIFO operation through LED-based observation. The TCL-driven automation methodology significantly reduces development effort and im-proves reproducibility, making it readily applicable to larger FPGA design projects.

Future work includes: (i) extending to an asynchronous FIFO with Gray-code pointer synchronization for clock domain crossing; (ii) adding programmable almost-full/almost-empty threshold flags; and (iii) integrating the FIFO as a data buffer in a UART or SPI communication subsystem.

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