A Review of Monolithic 3D Acceleration of SRAM using Planar MOSFETs for Low Power and Reliability

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***Abstract*—This review paper presents a comprehensive survey of Monolithic 3D (M3D) integration techniques applied to 8-transistor (8T) SRAM cells designed with planar MOSFETs, with a focus on achieving low power consumption and high reliability [1]. Conventional 6T SRAM architectures face significant stability limitations—most notably the read disturb phenomenon—during high-speed memory operations. This paper examines the existing body of literature concerning 8T SRAM bit-cell topologies implemented in 90 nm planar CMOS technology, wherein the read path is effectively decoupled from the internal storage nodes. The review synthesizes key findings related to Static Noise Margin (SNM) enhancement, Power-Delay Product (PDP) reduction, and the advantages conferred by monolithic 3D stacking compared to traditional through-silicon via (TSV)-based 3D integration [2]. This work establishes the theoretical benchmarks and design considerations that will inform subsequent simulation-based validation of the proposed 8T SRAM architecture.**

***Index Terms*—Monolithic 3D (M3D), 8T SRAM, Planar MOSFET, Low Power, Reliability, 90nm CMOS.**

I. INTRODUCTION

Static Random Access Memory (SRAM) constitutes a fundamental building block of modern digital systems, particularly within System-on-Chip (SoC) architectures where it occupies a substantial portion of the total die area and contributes significantly to overall power dissipation [3]. As semiconductor technology continues to scale into the deep sub-micron regime, traditional two-dimensional (2D) planar CMOS implementations encounter severe constraints related to power density, leakage current, and operational reliability.

In response to these scaling challenges, Monolithic 3D (M3D) integration has emerged as a promising alternative to conventional device scaling. Unlike TSV-based 3D integration, M3D technology enables sequential fabrication of multiple device tiers with nanoscale inter-tier vias, thereby offering substantial improvements in interconnect density, latency, and energy efficiency. This review paper specifically examines the application of M3D techniques to accelerate 8T SRAM performance while maintaining the compatibility and cost advantages of planar MOSFET technology at the 90 nm node.

II. PROBLEM STATEMENT

The widespread adoption of conventional 6T SRAM cells in high-performance memory arrays is hindered by an inherent design limitation: the read disturb vulnerability. During a read operation, the access transistors and the pull-down transistors of the cross-coupled inverter pair form a resistive voltage divider [1]. This condition temporarily elevates the voltage at the low storage node, potentially causing an unintended bit-flip and consequent loss of stored data. This stability degradation becomes increasingly severe as supply voltages are reduced to meet low-power design objectives and as process variations introduce mismatch between neighbouring transistors.

The central problem addressed by this review is the identification and analysis of alternative SRAM topologies and integration methodologies that can simultaneously satisfy the following design requirements:

- Read Stability: Elimination or significant mitigation of read disturb effects.

- Low Power Operation: Maintenance of low static and dynamic power consumption.
- Area Efficiency: Minimal increase in bit-cell footprint relative to the 6T baseline.
- Technology Compatibility: Feasibility of implementation using established planar MOSFET fabrication processes.

This review specifically investigates how an 8-transistor SRAM architecture, augmented by Monolithic 3D integration, addresses these conflicting design constraints.

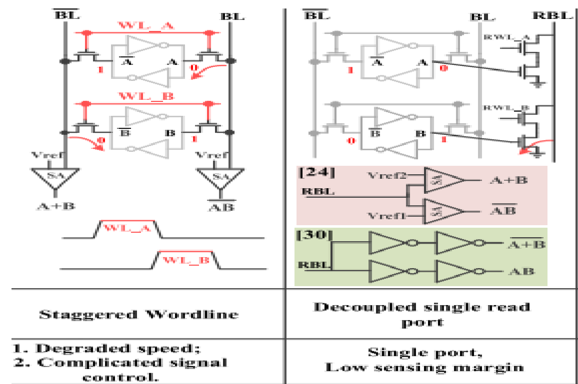

Fig 1. 6T vs 8T Read Path Comparison Diagram

III. LITERATURE SURVEY

The survey of existing literature reveals a definitive trajectory from 2D planar integration toward 3D monolithic stacking for advanced memory applications. The following subsections synthesize key contributions from recent research.

3.1 Evolution from 6T to 8T SRAM Architectures

The fundamental distinction between 6T and 8T SRAM topologies lies in the access mechanism for read operations. In a 6T cell, a single pair of access transistors serves both read and write operations, thereby coupling the read current path directly to the sensitive storage nodes. The 8T configuration introduces a dedicated read buffer comprising two additional transistors that form an isolated read port. This decoupling ensures that the read current does not perturb the voltage levels at the internal storage nodes, effectively eliminating the read disturb phenomenon [1], [5].

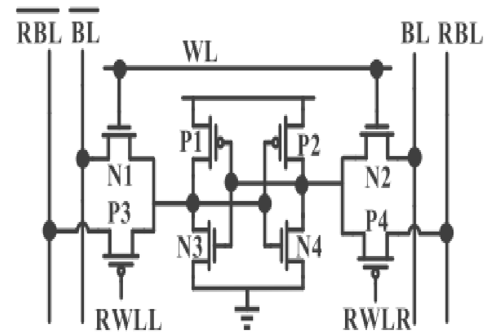

Fig 2. Schematic of 8T SRAM cell

Table 1: Literature Review of SRAM Performance Metrics

Metric	6T SRAM (Baseline)	Proposed 8T SRAM
Transistor Count	6	8
Read Mechanism	Shared Access Path	Dedicated, decoupled read port
Read Stability (SNM)	Low—susceptible to disturb	High—immune to read disturb
Write Margin	Moderate	Comparable to 6T
Leakage Current	Baseline	Slightly elevated (2 additional transistors)
Nominal Supply Voltage	1.2V	1.2V
Technology Node	90 nm planar CMOS	90 nm planar CMOS

3.2 Monolithic 3D Integration for SRAM Acceleration

Monolithic 3D integration distinguishes itself from traditional TSV-based 3D stacking through its sequential fabrication process. In M3D, upper device layers are fabricated directly atop lower layers at low thermal budgets, enabling inter-tier via dimensions on the order of tens of nanometers—orders of magnitude smaller than TSV diameters. This fine-grained vertical interconnectivity is particularly advantageous for SRAM arrays, where dense routing and minimal parasitic capacitance are essential for high-speed, low-energy operation [3], [4].

Guler and Jha [4] demonstrated that M3D stacking of FinFET-based 8T SRAM cells yields significant

improvements in read access time and leakage power compared to 2D implementations. While their work focuses on FinFET technology, the underlying M3D principles are equally applicable to planar MOSFET designs, offering a migration path that leverages existing fabrication infrastructure.

3.3 Planar MOSFETs in the 90 nm Node
Despite the industry's transition toward FinFET and fully depleted SOI technologies at advanced nodes, planar MOSFETs fabricated in the 90 nm node (e.g., gpdk090 process design kit) remain relevant for numerous applications due to their mature yield, lower mask costs, and well-characterized reliability mechanisms. The literature indicates that planar devices at this node exhibit acceptable short-channel effects when operated at nominal supply voltages near 1.2 V. However, to remain competitive with more advanced transistor architectures in terms of Power-Delay Product (PDP), innovative circuit topologies and integration schemes—such as the 8T cell with M3D stacking—are required [2], [5].

3.4 Performance Metrics: Static Noise Margin and Power-Delay Product
The Static Noise Margin (SNM) serves as the primary quantitative metric for assessing SRAM cell stability. It is defined as the maximum DC noise voltage that can be tolerated by the cross-coupled inverters before the stored state is corrupted. Theoretical analysis and prior simulation studies consistently indicate that 8T SRAM cells achieve significantly higher read SNM values compared to 6T cells, attributable to the isolation of storage nodes from the read bit-line [1], [4].

The Power-Delay Product (PDP) provides a composite figure of merit that balances energy consumption against switching speed. While the addition of two transistors in the 8T configuration marginally increases leakage power, the elimination of read disturb enables reliable operation at reduced supply voltages, thereby potentially lowering dynamic power. M3D integration further contributes to PDP reduction by minimizing interconnect capacitance and resistance [3].

PDP = Pavg \ Tdelay

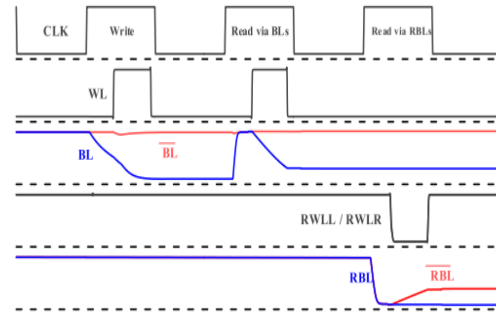

Fig.3 Timing diagram for different operation cycles

IV. PROPOSED THEORETICAL FRAMEWORK AND DESIGN METHODOLOGY

In preparation for the subsequent simulation phase of this research, we establish the theoretical boundaries and methodological approach that will guide experimental validation.

4.1 Static Noise Margin (SNM) Expectation
The 8T SRAM cell is theoretically expected to exhibit a read SNM substantially superior to that of the 6T baseline. This expectation derives from the isolation provided by the dedicated read buffer transistors, which prevents the read current from influencing the voltage state of the internal storage nodes.

4.2 Design Methodology Overview
The forthcoming simulation phase will employ Cadence Virtuoso for schematic entry and Spectre for transient, DC, and noise margin analyses. The design will be implemented using the gpdk090 90 nm planar CMOS process design kit. Based on the literature surveyed, a 1.2 V supply voltage is anticipated to provide an optimal balance between leakage current suppression and switching speed for this technology node.

4.3 Anticipated Advantages of M3D Integration
The literature strongly suggests that M3D integration of the proposed 8T SRAM design will yield the following benefits:

- Reduced Interconnect Delay: Shorter vertical connections between stacked tiers minimize RC delay.
- Lower Dynamic Power: Decreased wiring capacitance reduces energy per switching event.

- Enhanced Bit-Cell Density: Vertical stacking enables greater memory capacity within a given footprint.
- Improved Noise Immunity: Compact 3D routing minimizes coupling between adjacent signal lines.

V. CONCLUSION

This review paper has systematically examined the existing literature concerning Monolithic 3D acceleration of 8T SRAM cells implemented with planar MOSFET technology for low-power, high-reliability memory applications. The principal findings of this survey are summarized as follows:

- 8T SRAM Architecture: The addition of a dedicated read port effectively decouples the read path from the storage nodes, rendering the cell immune to read disturb and significantly enhancing read Static Noise Margin (SNM).
- Monolithic 3D Integration: M3D technology offers substantial advantages over conventional TSV-based 3D stacking, including finer inter-tier via pitch, reduced parasitic capacitance, and improved energy-delay characteristics—all of which are critical for memory acceleration.
- Planar MOSFET Viability: While FinFET technologies dominate at advanced nodes, planar MOSFETs at the 90 nm node remain a practical and cost-effective platform for SRAM implementation, particularly when augmented by innovative circuit topologies and M3D stacking.

This review establishes the theoretical foundation and performance benchmarks that will inform the subsequent simulation-based validation phase of this research. The anticipated simulation results will quantify the improvements in SNM, PDP, and access time achievable through the proposed M3D-accelerated 8T SRAM design.

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