Design and Implementation of BIST Architecture for low power VLSI Applications using Verilog

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Abstract—**Modern VLSI systems contain highly complex logic and memory components, making fault detection using traditional external testing methods difficult, expensive, and time-consuming. This paper presents the design and implementation of a low-power Built-In Self-Test (BIST) architecture for a RISC-V processor using Verilog HDL. The proposed architecture integrates scan chain, Logic Built-In Self-Test (LBIST), and Memory Built-In Self-Test (MBIST) techniques to improve testability and fault coverage. The scan chain enhances controllability and observability of internal registers, while LBIST uses LFSR and MISR structures for automatic logic fault detection. MBIST employs a March-based algorithm to detect memory faults efficiently. The proposed system enables automatic PASS/FAIL generation without external testing equipment. Experimental results show improved reliability, reduced testing cost, faster fault detection, and optimized power, area, and delay performance for low-power VLSI applications.**

Index Terms—**BIST, LBIST, MBIST, RISC-V Processor, Scan Chain, DFT, Verilog HDL, LFSR, MISR, Fault Detection, Low Power VLSI, Embedded Systems, Memory Testing, Logic Testing.**

I. INTRODUCTION

The continuous advancement in Very Large-Scale Integration (VLSI) technology has led to the development of highly complex digital systems containing millions of transistors, embedded memories, and high-speed processing units. As circuit complexity increases, ensuring the reliability and correctness of these systems becomes a major challenge. Traditional external testing techniques require expensive Automatic Test Equipment (ATE), large testing time, and complex debugging procedures, making them less suitable for modern System-on-Chip (SoC) and processor-based applications. Therefore, efficient Design for Testability (DFT) techniques are essential to improve fault detection and simplify the testing process.

Built-In Self-Test (BIST) is one of the most effective DFT methodologies used in modern VLSI systems. BIST enables the circuit to test itself internally without depending heavily on external testing hardware. It automatically generates test patterns, applies them to the circuit under test (CUT), analyzes the output responses, and finally produces a PASS or FAIL result. This self-testing capability significantly reduces testing cost, minimizes testing time, improves fault coverage, and enhances system reliability.

In processor-based systems such as RISC-V architectures, both logic circuits and embedded memories are highly vulnerable to manufacturing defects, stuck-at faults, transition faults, and memory-related failures. Detecting these faults using conventional methods becomes difficult because of limited internal visibility and controllability. To overcome these challenges, scan chain testing, Logic Built-In Self-Test (LBIST), and Memory Built-In Self-Test (MBIST) techniques are widely used.

The scan chain technique improves the controllability and observability of internal processor registers by connecting them as shift registers during test mode. This allows easy shifting of test data into the processor and observation of internal outputs. LBIST is mainly used for testing processor logic automatically. It utilizes a Linear Feedback Shift Register (LFSR) to generate pseudo-random test patterns and a Multiple Input Signature Register (MISR) to compress and analyze output responses. By comparing the generated signature with the expected signature, logic faults inside the processor can be detected efficiently.

Similarly, MBIST is used for testing embedded memories such as instruction memory (IMEM) and

data memory (DMEM). MBIST performs memory fault detection using March-based algorithms that involve writing and reading different test patterns such as logic '0' and logic '1'. This technique helps identify common memory faults including stuck-at faults, coupling faults, and address faults with high accuracy. This paper presents the design and implementation of a low-power BIST architecture for a RISC-V processor using Verilog HDL. The proposed architecture integrates scan chain, LBIST, and MBIST techniques into a single testing framework. During normal functional mode, the processor operates as a standard RISC-V system. During test mode, the architecture automatically performs logic and memory testing without external testing equipment. The proposed system improves internal observability, increases fault coverage, reduces testing complexity, and enhances processor reliability.

The complete architecture is designed and implemented using Verilog HDL and verified through simulation and synthesis results. Experimental analysis shows that the proposed BIST system achieves efficient fault detection with optimized area, power consumption, and delay performance. Therefore, the proposed methodology is highly suitable for modern low-power VLSI and embedded processor applications where reliable and cost-effective testing is required.

II. LITERATURE SURVEY

Mehta and Singh (2025) proposed a Hybrid Scan-BIST architecture for VLSI applications by combining scan chain testing with Built-In Self-Test techniques to improve fault detection and internal controllability. The methodology integrated scan registers with pseudo-random test pattern generation to enhance testing efficiency in digital circuits. The results showed improved fault coverage and better observability of internal signals; however, the architecture increased overall design complexity and hardware overhead due to additional scan logic and control circuitry [1].

Patel et al. (2025) developed a low-power BIST architecture for VLSI systems using optimized Linear Feedback Shift Register (LFSR) and Multiple Input Signature Register (MISR) structures implemented in Verilog HDL. The proposed method reduced switching activity during test pattern generation to minimize dynamic power consumption during testing operations. Simulation results demonstrated lower power dissipation and efficient fault detection capability, although the design introduced additional hardware area overhead because of the integrated BIST components [2].

Sharma and Reddy (2025) presented an energy-efficient BIST architecture using Verilog HDL for reducing power consumption in VLSI circuits. The methodology focused on controlling unnecessary transitions during pseudo-random pattern generation and output response analysis [3].

Kumar et al. (2025) implemented an FPGA-based low-power BIST design using pseudo-random testing techniques in Verilog HDL. The architecture employed LFSR-generated test patterns and response compression techniques to detect logic faults efficiently in FPGA-based digital systems. Experimental results showed improved testing performance, reduced testing time, and lower power consumption on FPGA platforms. However, the obtained results may not accurately represent actual ASIC performance because FPGA The proposed design achieved reduced switching activity and improved energy efficiency during test mode operation. However, the technique provided limited fault coverage for certain complex faults, which affected overall testing efficiency architectures differ significantly from ASIC implementations [4].

Verma and Gupta (2024) proposed a scan chain-based Design for Testability (DFT) architecture for RISC-V processors to improve internal observability and controllability of processor registers. The methodology connected internal registers as shift chains during test mode, allowing efficient shifting of test patterns and observation of internal outputs. The proposed design improved debugging capability and fault detection efficiency in processor systems. However, the scan shifting process increased overall testing time and introduced additional timing overhead [5].

Kim et al. (2025) introduced an integrated LBIST and MBIST architecture for embedded processor systems to perform automatic logic and memory fault detection simultaneously. The proposed system utilized LFSR-based pseudo-random test generation for logic testing and March-based algorithms for memory testing. Experimental analysis showed improved reliability, enhanced fault coverage, and efficient self-testing

capability for embedded systems. However, additional power consumption was observed during test mode because both logic and memory testing modules operated simultaneously [6].

III. PROPOSED WORK

The proposed work presents a low-power Built-In Self-Test (BIST) architecture integrated with a RISC-V processor for efficient fault detection and testing in VLSI systems. The proposed design combines Scan Chain Testing, Logic Built-In Self-Test (LBIST), and Memory Built-In Self-Test (MBIST) within a single testing framework using Verilog HDL. Unlike conventional external testing methods, the proposed architecture enables automatic internal testing without requiring expensive Automatic Test Equipment (ATE).

The proposed BIST system consists of a RISC-V Core, Instruction Memory (IMEM), Data Memory (DMEM), Scan Multiplexer, scan chain registers, LBIST module, MBIST module, Linear Feedback Shift Register (LFSR), Multiple Input Signature Register (MISR), and BIST controller. The scan chain improves observability and controllability of internal processor registers by connecting them serially during test mode operation.

The LBIST module performs automatic logic testing using pseudo-random test patterns generated through the LFSR, while the MISR compresses output responses and generates a signature for fault detection. The MBIST module performs memory testing using a March-based algorithm to detect faults in instruction and data memories. The architecture operates in two modes: Functional Mode and Test Mode. During Functional Mode, the processor executes normal operations, whereas in Test Mode, the architecture performs automatic self-testing of logic and memory components.

A. Top Level BIST System

The proposed BIST_RISCV_TOP architecture serves as the top-level control module for managing functional and test operations in the RISC-V processor. The architecture consists of two multiplexers, namely the Test Mode Multiplexer and the Reset Multiplexer, which are controlled by dedicated selection signals. The Test Mode Multiplexer selects between the normal functional input and the test input based on the value of the test_mode signal. During normal operation, the functional path is enabled, allowing the processor to execute instructions and perform regular computations.

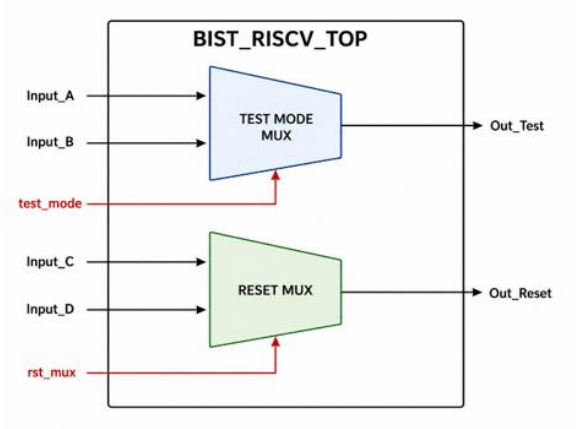

Fig.1. Top Level Module

When the test mode is activated, the multiplexer switches the system to the test path, enabling Built-In Self-Test (BIST) operations such as LBIST and MBIST. Similarly, the Reset Multiplexer selects the appropriate reset source for either functional operation or testing. This architecture provides a flexible mechanism for switching between normal and test modes without modifying the processor hardware. By integrating multiplexing-based control logic, the proposed design improves test accessibility, simplifies fault detection, and enables efficient self-testing of the processor, thereby enhancing the reliability and testability of low-power VLSI systems.

B. BIST Architecture

The proposed BIST architecture integrates a Scan Multiplexer, RISC-V Core, Instruction Memory, Data Memory, Logic Built-In Self-Test (LBIST), and Memory Built-In Self-Test (MBIST) into a unified testing framework for low-power VLSI applications. The Scan MUX serves as the interface between normal operation and test operation by controlling the flow of test patterns to the processor. The RISC-V Core acts as the Circuit Under Test (CUT) and performs normal instruction execution during functional mode. The Instruction Memory stores program instructions, while the Data Memory stores data required for processor operations. To ensure reliable operation, the MBIST module performs memory fault detection by testing both instruction and data memories using a March-based testing algorithm. The LBIST module is responsible for automatic logic testing of the RISC-V core using pseudo-random test patterns generated through an LFSR and response analysis performed by a MISR.

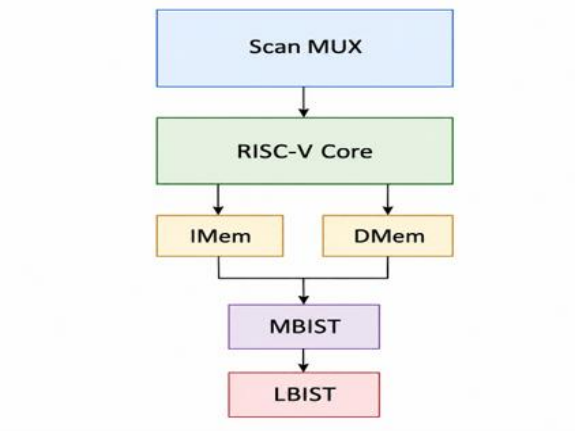

Fig.2. BIST Architecture

During test mode, the architecture enables comprehensive testing of both logic and memory components, improving fault coverage, observability, controllability, and system reliability. The integration of scan-based testing, LBIST, and MBIST reduces dependence on external testing equipment while providing an efficient and cost-effective self-test solution for modern VLSI systems

C. RISC-V CUT Operation

The RISC-V Core functions as the Circuit Under Test (CUT) in the proposed BIST architecture. During Functional Mode, the Program Counter (PC) generates instruction addresses, and instructions are fetched from the Instruction Memory (IMEM). The fetched instructions are stored in the Instruction Register and processed through the Accumulator (ACC) register. Based on the execution results, data addresses are generated and data is written to the Data Memory (DMEM). Thus, the processor performs normal instruction execution and memory operations.

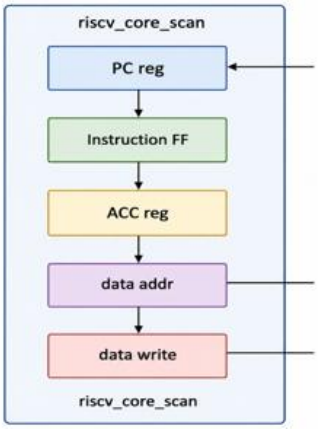

Fig.3. RISC-V CUT

During Scan Mode, the internal registers such as the PC register, Instruction Register, ACC register, Data Address register, and Data Write register are connected as a scan chain. Test patterns are shifted through these registers to observe and control internal states of the processor. This scan-based structure improves fault detection, controllability, and observability, enabling efficient testing of the RISC-V processor logic.

D. Logic BIST

The Logic Built-In Self-Test (LBIST) module is integrated into the proposed BIST architecture to perform automatic testing of the RISC-V processor logic.

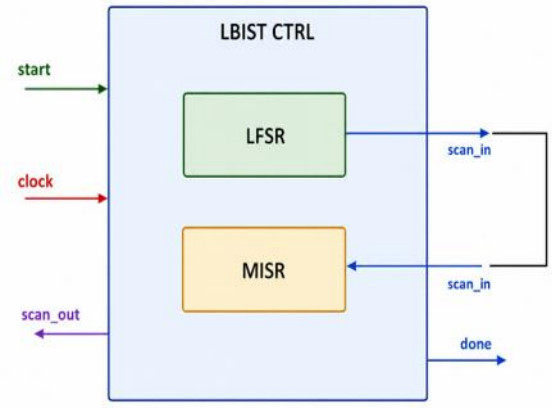

Fig.4. Logic BIST

As shown in the functional diagram, the LBIST controller manages the complete testing process using a Linear Feedback Shift Register (LFSR) and a Multiple Input Signature Register (MISR). When the start signal is activated, the LFSR generates pseudo-random test patterns and applies them to the RISC-V Core through the scan_in path. The internal logic of the processor evaluates these test patterns, and the resulting responses are shifted out through the scan_out path. The MISR captures and compresses the output responses into a compact signature, which is compared with a reference signature to determine the presence of faults. The entire testing operation is synchronized using the system clock, and a done signal is generated upon completion of the test sequence. By integrating the LFSR, MISR, and scan-chain mechanism, the proposed LBIST architecture improves fault coverage, reduces testing time, and enables efficient self-testing of the RISC-V processor without requiring external testing equipment.

E. Memory BIST

The Memory Built-In Self-Test (MBIST) module is designed to perform automatic testing of the Instruction Memory (IMEM) and Data Memory (DMEM) within the proposed RISC-V processor architecture. As shown in the functional diagram, the MBIST Controller manages the entire memory testing process using an Address Counter, Pattern Generator, Compare Logic, and Fail

Flag unit. When the Start signal is activated, the Address Counter sequentially generates memory addresses, while the Pattern Generator produces predefined test patterns that are written into the memory through the mem_addr and mem_wdata signals. The memory responses, received through the imem_rdata interface, are compared with the expected values by the Compare Logic block.

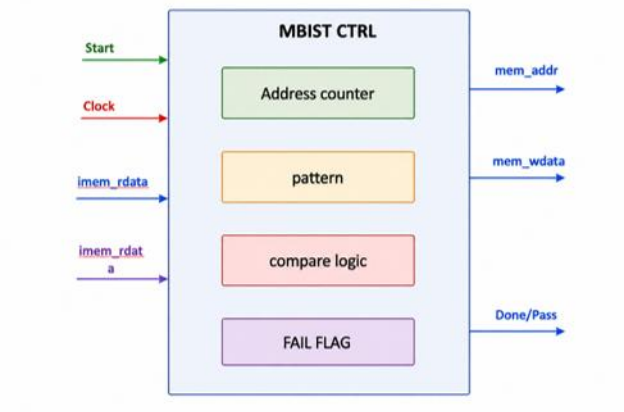

Fig.5. Memory BIST

Any mismatch detected during the comparison process activates the Fail Flag, indicating the presence of a memory fault. The testing operation is synchronized using the system Clock, and upon successful completion, the controller generates a Done/Pass signal. The proposed MBIST architecture enables efficient detection of memory faults such as stuck-at faults, address faults, and data retention faults, thereby improving memory reliability, fault coverage, and overall system testability without requiring external testing equipment.

IV. RESULTS

A. RTL Schematic

Figure 6 shows the RTL schematic of the proposed BIST-enabled RISC-V processor designed using Verilog HDL. The architecture integrates the RISC-V core with Scan Chain, Logic Built-In Self-Test (LBIST), and Memory Built-In Self-Test (MBIST) modules to provide efficient fault detection and self-testing capabilities. The RTL view illustrates the complete hardware connectivity between processor registers, memory blocks, multiplexers, control logic, and test modules.

During normal operation, the RISC-V processor executes instructions from the instruction memory and performs data operations through the data memory.

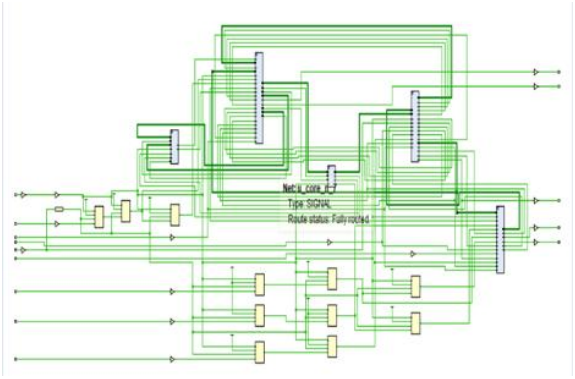

Fig.6. RTL Schematic

When test mode is enabled, the scan chain provides access to internal registers, while the LBIST and MBIST modules perform automatic testing of logic and memory components. The LBIST module generates test patterns and analyzes responses to detect logic faults, whereas the MBIST module verifies the correctness of memory operations using dedicated test patterns and comparison logic. The RTL schematic confirms the successful integration of all functional and test modules within a single architecture. This implementation improves fault coverage, enhances system reliability, and reduces dependence on external testing equipment, making it suitable for modern low-power VLSI and embedded processor applications.

B. Simulation Results and Verification

The proposed BIST-enabled RISC-V processor was verified using Xilinx Vivado simulation under both fault-free and fault-injected conditions. Figure 7 shows the simulation waveform of the system operating without any introduced faults. In this case, the logic and memory modules function correctly, and the generated outputs match the expected values. The LBIST and MBIST modules complete the testing process successfully, indicating normal operation of the processor.

Figure 8 shows the simulation waveform after introducing faults into the design. The injected faults cause mismatches between the expected and actual responses, which are detected by the BIST architecture. The LBIST and MBIST controllers identify the faulty condition through signature comparison and memory verification mechanisms, thereby demonstrating the effectiveness of the proposed self-test approach.

Fig.7. Fault-free simulation waveform

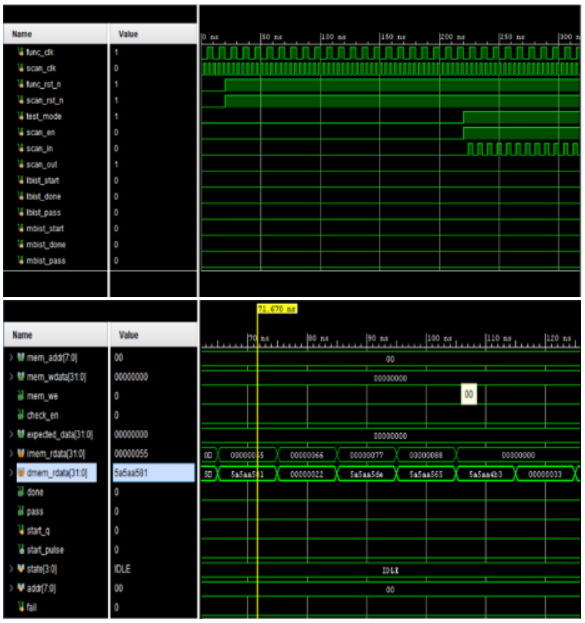

Fig.8. Fault-injected simulation waveform.

The simulation results demonstrate the effectiveness of the proposed BIST architecture in verifying both logic and memory components of the RISC-V processor. The integration of scan chain, LBIST, and MBIST modules enables comprehensive testing without the need for external testing equipment. The scan chain improves internal controllability and observability, allowing efficient application of test patterns and monitoring of internal processor states.

Furthermore, the fault-injection analysis confirms the capability of the proposed architecture to detect faults accurately and distinguish between normal and faulty operating conditions. The LBIST module effectively identifies logic-related faults through signature analysis, while the MBIST module detects memory faults using automated read and write verification operations. This combined testing approach improves fault coverage and enhances the reliability of the overall system.

The successful simulation and verification results validate the functionality of the proposed design and demonstrate its suitability for low-power VLSI applications. The architecture provides a cost-effective and scalable testing solution for modern RISC-V based embedded systems, reducing testing time while maintaining high fault detection efficiency.

C. Performance Analysis and Resource Utilization of the Proposed BIST Architecture

Table I. Performance Analysis and Resource Utilization of the Proposed BIST Architecture:

Parameter	Proposed
Power	8.3mW
Delay	3.096ns
Area(mm²)	0.277
Slice Registers	277
LUTs	272

V. CONCLUSION

The proposed BIST architecture for the RISC-V processor was successfully designed and verified using Verilog HDL. By integrating Scan Chain Testing, Logic Built-In Self-Test (LBIST), and Memory Built-In Self-Test (MBIST), the architecture provides an effective solution for detecting faults in both processor logic and memory modules. The simulation results demonstrated correct operation under normal as well as fault-injected conditions,

confirming the ability of the system to identify and isolate faults accurately. The implementation results showed low power consumption, acceptable delay, and efficient resource utilization, making the design suitable for low-power VLSI applications. The scan chain improved the observability and controllability of internal registers, while the LBIST and MBIST modules enabled automatic self-testing without relying on external test equipment.

Overall, the proposed architecture enhances system reliability, reduces testing complexity, and offers a practical and cost-effective testing solution for modern RISC-V based embedded systems.

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