Design and Implementation of a Micro-Blaze Based Ethernet Lite Using FPGA IP Cores

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Abstract— **Design and implementation of a MicroBlaze-based Ethernet Lite communication system using FPGA IP cores on the Artix-7 Arty A7-35T platform. The proposed system integrates the MicroBlaze soft-core processor, AXI Ethernet Lite IP, AXI UART Lite, AXI Timer, AXI Interrupt Controller, and AXI Interconnect using Xilinx Vivado and Vitis tools. The lwIP lightweight TCP/IP stack is incorporated to support Ethernet communication and packet transmission between the FPGA board and host computer through static IP configuration. Experimental results confirm successful 10/100 Mbps Ethernet communication, ping response, TCP/IP packet transfer, and UART-based debugging. Comparative analysis with the existing Virtex-5 TEMAC-based system shows significant improvements in FPGA resource utilization, power efficiency, scalability, and debugging support. The proposed system achieved optimized FPGA resource utilization with 11,847 LUT usage and 22 BRAM utilization. The power consumption was also reduced from 12.27 W to 0.892 W, improving energy efficiency. The AXI-based architecture and Vivado/Vitis tool flow also improved system flexibility, reduced latency, and simplified hardware-software integration. The implemented system demonstrates a low-cost, lightweight, and efficient FPGA-based Ethernet communication solution suitable for embedded networking and industrial applications.**

Index Terms— **vivado, Arty-A7, Microblaze, Ethernet lite**

I. INTRODUCTION

Ethernet communication is an essential technology in modern embedded systems used for industrial automation, IoT, robotics, networking, and real-time monitoring applications [9], [14]. It provides reliable, scalable, and high-speed data transfer between connected devices [14]. Due to its low cost and widespread adoption, Ethernet has become a preferred communication standard in embedded applications [9].

FPGA-based systems are increasingly used for implementing Ethernet-enabled solutions because they offer flexibility, parallel processing, and hardware acceleration [1], [2], [6]. A Field Programmable Gate Array (FPGA) is a reconfigurable hardware platform that allows customized digital system design according to application requirements [2]. Unlike conventional microcontrollers, FPGAs can execute multiple operations simultaneously, improving overall system.

performance. Modern FPGA devices support embedded processors, memory controllers, communication interfaces, and custom hardware modules within a single chip [6].

The MicroBlaze processor, developed by AMD Xilinx, is a 32-bit soft-core RISC processor widely used in FPGA-based embedded systems [10]. It provides configurable architecture, interrupt support, cache memory, and seamless integration with AXI-based peripherals [10].

Ethernet communication in FPGA systems is commonly implemented using Ethernet Media Access Controller (MAC) IP cores [1], [6]. In this project, the AXI Ethernet Lite IP core is utilized because it offers a lightweight and resource-efficient Ethernet solution supporting 10/100 Mbps communication [11]. The AXI protocol simplifies communication between the processor and peripherals while improving system scalability [11].

The hardware platform used is the Arty A7-35T development board based on the Artix-7 FPGA architecture. Compared to older high-end FPGA devices such as Virtex-5, the Artix-7 platform offers reduced cost and power consumption while maintaining adequate performance for embedded networking applications [2], [4].

The hardware design is developed using Vivado Design Suite [12], while software development is carried out using the Vitis Unified Software Platform [13]. To enable TCP/IP networking functionality, the lightweight IP (lwIP) stack is integrated into the system [8]. The lwIP stack is specifically designed for embedded applications with limited memory and processing resources [8]. It provides efficient implementation of TCP/IP protocols required for Ethernet communication [8], [14].

The developed system demonstrates a cost-effective and resource-efficient FPGA-based Ethernet communication platform suitable for networking and embedded communication applications [5], [7].

AXI Interconnect is used to connect the processor with Ethernet and memory peripherals efficiently [10], [11]. The Ethernet Lite IP handles Ethernet frame formatting, transmission, and reception functions [11]. The lwIP stack provides support for TCP, UDP, IP, ARP, and ICMP protocols required for network communication [8], [14].

II. METHODOLOGY

The existing Virtex-5 FPGA based soft-core processor Ethernet communication system was designed for Ethernet data transfer between the FPGA and host computer. The architecture mainly consisted of the Virtex-5 FPGA platform, Micro Blaze soft-core processor, Ethernet MAC controller, Ethernet PHY interface, UART modules, memory modules, and communication peripherals. The Ethernet MAC controller handled Ethernet frame transmission and reception, while the Ethernet PHY interfaced with the host computer through Ethernet communication. UART communication and memory buffering modules were used for debugging, packet handling, and data storage. The system verified Ethernet communication using network utilities such as ping testing and packet monitoring. However, the traditional Ethernet communication architecture and the use of Virtex-5 FPGA increased hardware complexity, FPGA resource utilization, power consumption, and implementation overhead.

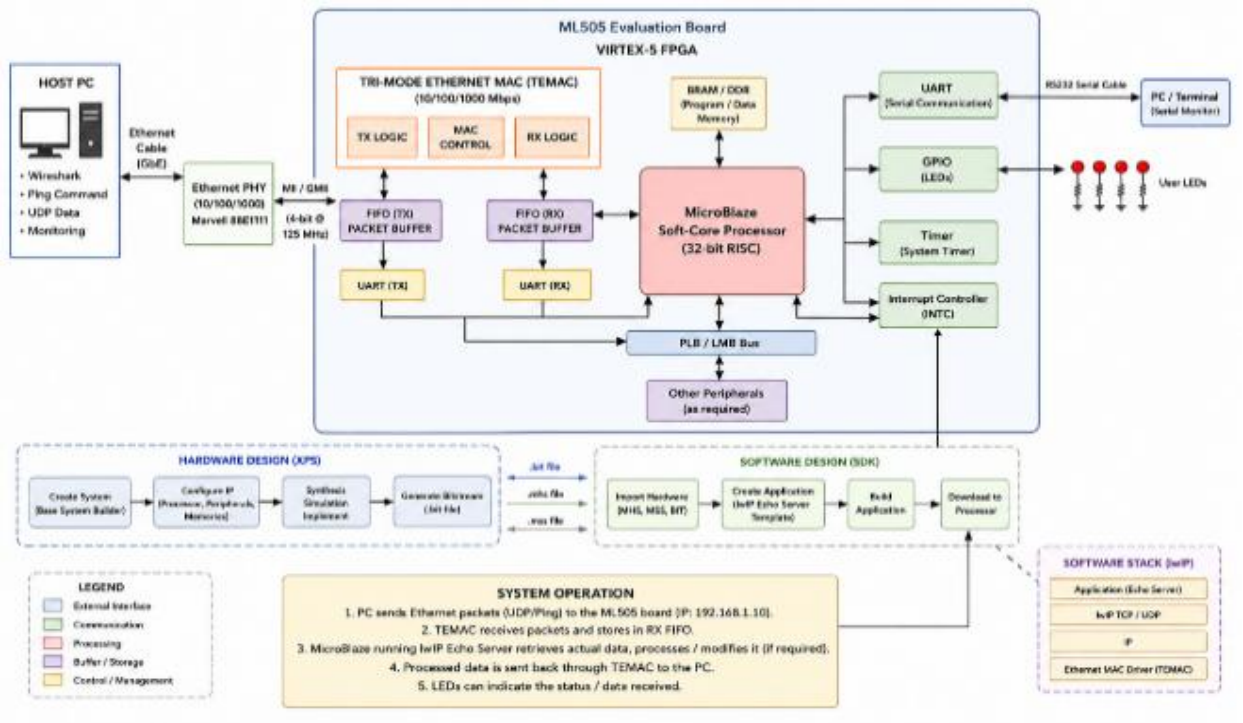

Figure 1: Virtex-5 FPGA Based Ethernet Data Transfer System

Figure.1 illustrates an Ethernet communication system implemented on the ML505 board using a Virtex-5 FPGA and the MicroBlaze soft-core processor. The architecture includes MicroBlaze, Tri-Mode Ethernet MAC (TEMAC), Ethernet PHY, FIFO buffers, BRAM/DDR memory, UART, GPIO LEDs, timer,

and interrupt controller. The host PC communicates with the FPGA through a Gigabit Ethernet connection. The Ethernet PHY interfaces with the TEMAC core via the MII/GMII interface operating at 125 MHz. TEMAC supports 10/100/1000 Mbps Ethernet communication and handles packet transmission and reception. Received packets are stored in FIFO buffers and processed by the MicroBlaze processor running the lwIP Echo Server application. BRAM/DDR memory is used for program execution and packet storage. UART provides serial debugging, while GPIO LEDs indicate system activity.

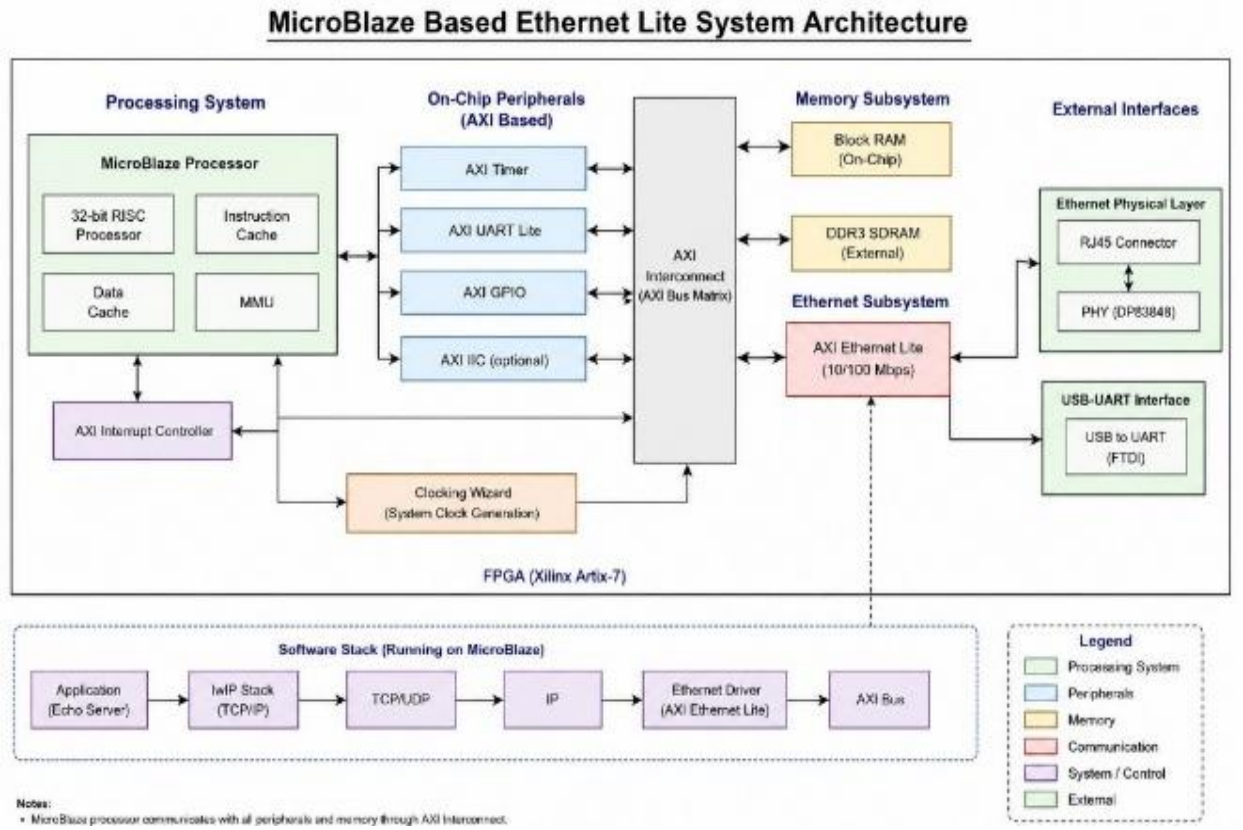

Figure.2: Proposed MicroBlaze-Based Ethernet Lite System Architecture

The MicroBlaze processor acts as the central processing unit responsible for executing the embedded software application. The Ethernet Lite IP core performs Ethernet frame transmission and reception. Communication between different peripherals is achieved through the AXI bus architecture.

The lwIP stack provides TCP/IP communication support and enables packet-based Ethernet communication between the FPGA board and the host computer. UART communication is used for debugging and displaying system information such as IP address and communication status. The proposed architecture provides a lightweight and modular embedded communication system suitable for low-cost FPGA implementation.

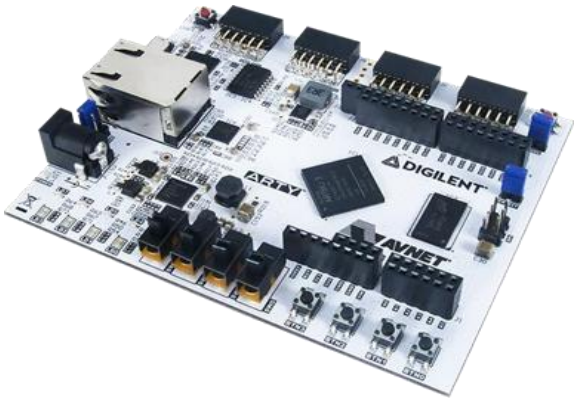

Figure.3: Artix-7 FPGA Board

The proposed Ethernet communication system is implemented on the Artix-7 FPGA available on the Arty A7-35T development board. The Artix-7 FPGA

is chosen because of its low cost, low power consumption, and compatibility with AXI-based embedded system design. Compared to the Virtex-5 FPGA used in the reference implementation, it provides a more economical and efficient solution while maintaining reliable performance.

- Instruction cache
- Data cache
- AXI communication interface
- Interrupt handling
- Memory access

The MicroBlaze processor provides a flexible architectural solution which allows the designer to turn off and on features of the processor as required by their applications. All peripherals communicate with the MicroBlaze processor using the AXI interconnect architecture, providing flexibility in the development of embedded applications and enabling the use of a soft-core processor within an FPGA.

The AXI architecture provides several advantages such as:

- Modular architecture
- Easy IP integration
- Reduced communication latency
- Simplified debugging
- High-speed communication
- Parallel data transfer

The AXI interconnect is the core of the embedded system architecture outlined earlier in this section. It provides interconnectivity between the processor and the Ethernet controller, UART, timer, memory controller, interrupt controller and other peripherals, when present.

The UART terminal displays important information such as:

- FPGA boot messages
- Ethernet initialization status
- IP address configuration
- Packet transmission status
- Error and debugging messages

The host computer communicates with the FPGA via a USB-UART interface. Tera Term serial terminal program is used to monitor UART output. Debugging using a UART connection is critical for verifying the performance of an embedded Ethernet system and for determining whether or not there were any communication errors during an execution of the embedded Ethernet system.

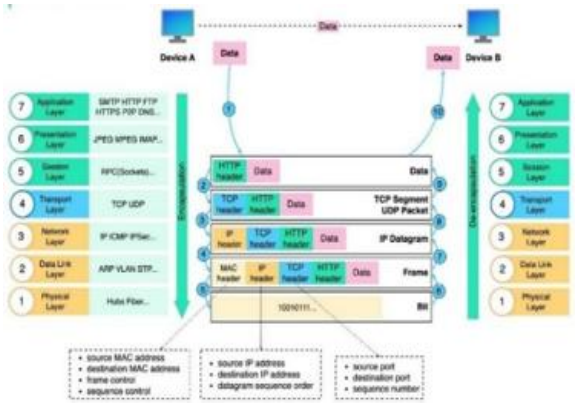

Fig.4 TCP/IP data encapsulation process

For TCP/IP communication within the proposed system, the lightweight IP (lwIP) stack will be incorporated to provide TCP/IP communications in an embedded system with limited memory and processing capabilities.

- TCP protocol
- UDP protocol
- IP addressing
- Ethernet frame handling
- Packet buffering

As lwIP is small and lightweight, it has a reduced memory consumption and is less resource-intensive than traditional TCP/IP stacks, and is therefore suited to FPGA based embedded applications. The lwIP stack will run on the MicroBlaze CPU and will be communicating with the Ethernet Lite IP core to send and receive packets, while also managing the network communication between the FPGA board and the host computer.The lwIP stack runs on the MicroBlaze processor and communicates with the Ethernet Lite IP core for packet transmission and reception. It manages network communication between.

The software application performs:

- Ethernet controller initialization
- lwIP stack initialization
- IP address configuration
- Packet processing
- UART communication
- Communication testing

The proposed system is based upon the co-design methodology of hardware and software working cooperatively within the FPGA hardware platform. The co-design methodology enables improvements in flexibility, debugability and system optimization. Hardware acceleration is to be incorporated into future work to further enhance communication performance.

The hardware implementation of the proposed system is carried out using Xilinx Vivado Design Suite on the Arty A7-35T. The complete architecture is designed using Vivado IP Integrator by integrating various FPGA IP cores.

The major hardware components used in the design are:

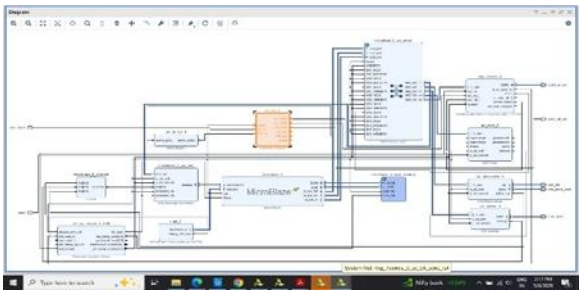

Figure 5: Vivado Block Design of MicroBlaze-Based Ethernet Lite System

- MicroBlaze soft-core processor
- AXI Ethernet Lite IP core
- AXI UART Lite
- AXI Timer
- AXI Interrupt Controller
- AXI Interconnect
- Clocking Wizard

The MicroBlaze processor acts as the central processing unit and controls all Ethernet communication operations within the system. The AXI Interconnect enables communication between the processor and peripherals through the AXI bus architecture. The AXI Ethernet Lite IP core provides 10/100 Mbps Ethernet communication and handles Ethernet frame transmission and reception via the onboard PHY interface. AXI UART Lite is used for serial communication, debugging, and displaying network-related information. The AXI Timer performs timing and delay generation functions, while the AXI Interrupt Controller manages interrupts from Ethernet and UART peripherals. After integrating all IP cores, address mapping and AXI connections are configured and verified. Finally, the design is synthesized, implemented, and programmed onto the Artix-7 FPGA using the generated bitstream file.

The software implementation is developed using the Xilinx Vitis platform after exporting the hardware design from Vivado. The application is written in Embedded C and executed on the MicroBlaze processor. A Board Support Package (BSP) is configured to support peripherals such as Ethernet Lite, UART, timer, and interrupt controller. The lwIP (Lightweight IP) stack is integrated to enable TCP/IP networking functionality. It manages packet transmission, IP addressing, Ethernet frame processing, and network communication. The lightweight architecture of lwIP ensures efficient operation with low memory and resource utilization

The software implementation mainly performs:

- Ethernet controller initialization
- lwIP stack initialization
- Static IP configuration
- Packet transmission and reception
- UART debugging and monitoring

The FPGA board is connected to the host computer using an Ethernet cable. Static IP addresses are configured for both systems to establish communication. During execution, the MicroBlaze processor initializes the Ethernet Lite IP and lwIP stack. Ethernet packets received from the host computer are processed by the lwIP stack and transmitted back through the Ethernet interface.

Figure 6: BSP Configuration with lwIP Library in Vitis

UART terminal output is used to verify successful communication by displaying IP address information, packet status, and debugging messages.

III. RESULTS

The complete hardware architecture was successfully implemented using Vivado IP Integrator. The block design included MicroBlaze processor, AXI Ethernet Lite IP, AXI UART Lite, AXI Timer, AXI Interconnect, DDR memory controller, and interrupt controller.

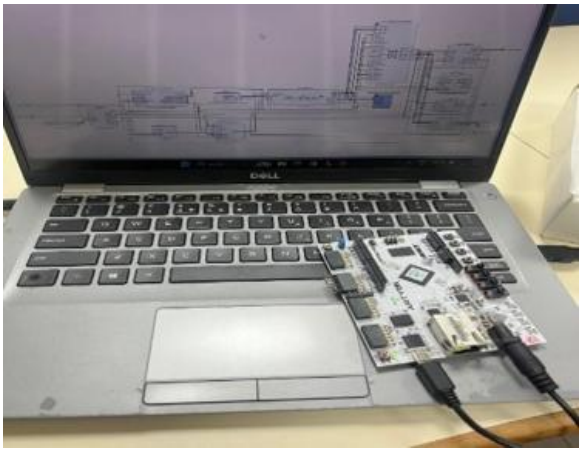

Figure.7 Vivado Block Design of Proposed Ethernet Lite System

The FPGA resource utilization report was generated using the Vivado implementation tool after successful synthesis and implementation of the proposed Ethernet Lite system. The report shows the utilization of major FPGA resources such as LUTs, Flip-Flops, BRAMs, DSP slices, and IO pins. The proposed MicroBlaze-based Ethernet Lite architecture utilized 11,847 LUTs and 22 BRAMs on the Artix-7 FPGA device. This flexibility enhances the adaptability of the system for various industrial and IoT applications. Furthermore, the implementation confirms that reliable Ethernet communication can be achieved with low hardware overhead and efficient resource management.

Site Type	Used	Fixed	Available	Util%
Slice LUTs	11847	0	20800	56.96
LUT as Logic	10465	0	20800	50.31
LUT as Memory	1382	0	9600	14.40
LUT as Distributed RAM	928	0		
LUT as Shift Register	454	0		
Slice Registers	11472	0	41600	27.58
Register as Flip Flop	11468	0	41600	27.57
Register as Latch	0	0	41600	0.00
Register as AND/OR	4	0	41600	<0.01
F7 Muxes	198	0	16300	1.21
F8 Muxes	0	0	8150	0.00

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	22	0	50	44.00
RAMB36/FIFO*	18	0	50	36.00
RAMB36E1 only	18			
RAMB18	8	0	100	8.00
RAMB18E1 only	8			

Figure.8: Memory Resource Utilization

Power analysis of the proposed system was performed using the Vivado power analysis tool after hardware implementation. The generated report estimated the total on-chip power consumption of the Artix-7 FPGA-based Ethernet Lite system. The proposed architecture consumed approximately 0.892 W of total power, which is lower compared to traditional Virtex-5 TEMAC-based Ethernet systems.

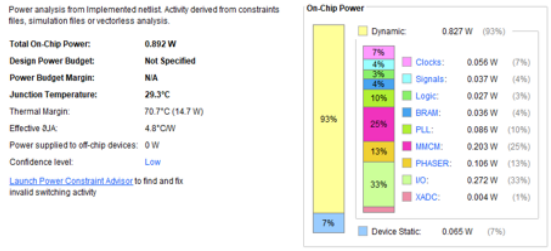

Figure .9: Power report.

The reduction in power consumption was achieved by using the lightweight AXI Ethernet Lite IP core and optimized AXI-based embedded architecture. The lower power requirement makes the proposed system suitable for low-cost and energy-efficient embedded networking applications.

The timing summary report generated after implementation verified that the proposed Ethernet Lite design met the required FPGA timing constraints. Timing analysis showed a small negative slack of -3.383 ns, indicating minor timing violations that can be improved through further optimization. Despite this, the system successfully performed Ethernet communication without functional issues. The results confirm reliable operation of the MicroBlaze processor, AXI interconnect, and Ethernet Lite architecture on the Artix-7 FPGA platform.

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)
-3.383	-3.383	1	37377	0.052	0.000

THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
0	37319	0.251	0.000	0	14149

Figure.10: Timing Summary Report

The software platform was successfully developed using Xilinx Vitis. The Board Support Package (BSP) was configured with lwIP TCP/IP library support.
The lwIP stack initialization was completed successfully, enabling Ethernet communication support for the MicroBlaze processor.

The software implementation verified successful integration of:

- lwIP TCP/IP stack
- Ethernet drivers
- UART drivers
- Interrupt support

The embedded application was compiled and executed successfully on the MicroBlaze processor. The host PC was configured with Ethernet settings that are in the same subnet as the board allowing for communication to be established.

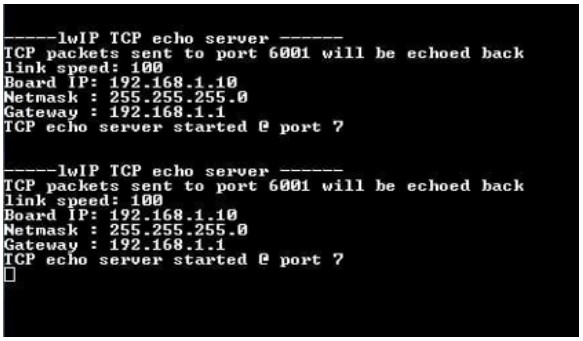

Figure 11 static IP address Configuration

The configured network parameters enabled successful communication between FPGA and host PC through Ethernet interface.

- TCP/IP communication
- Ethernet frame processing

The lwIP stack successfully handled incoming and outgoing Ethernet packets.

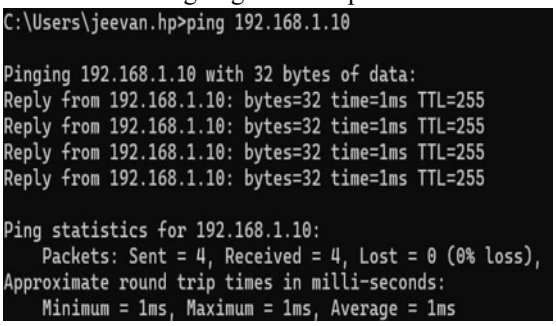

Figure .12 Static IP Ping result

The throughput and latency performance of the proposed MicroBlaze-based Ethernet Lite system were evaluated after establishing Ethernet communication between the FPGA board and the host computer. The AXI Ethernet Lite IP core successfully achieved stable 100 Mbps communication using static IP configuration and the lwIP TCP/IP stack.

Table.1: Throughput and Latency Analysis

Parameter	Measured Value
Ethernet Communication Speed	100 Mbps
Ethernet Communication Speed	100 Mbps
Average Ping Response Time	1 ms
Packet Loss	0%

The obtained results confirm that the proposed lightweight Ethernet communication architecture provides stable and efficient packet-based communication suitable for embedded networking applications.

Table.2: Comparative Analysis

Parameter	Existing System [13] [	Proposed System
FPGA Platform	Virtex-5	Artix-7
Ethernet Interface	TEMAC	AXI Ethernet Lite
Cost	High	Low
Power Consumption	12.27 W	0.892 W
Flexibility	Moderate	High
Design Tool Flow	EDK/XPS	Vivado/Vitis
Architecture	Traditional Bus-Based	AXI-Based
Resource Utilization	More LUT Usage	11,847 LUT Usage
Performance Optimization	Limited	Enhanced
Debugging Support	Basic	AXI ILA & UART
Communication Speed	1 Gbps	10/100 Mbps
BRAM Utilization	>35	22 BRAMs
Latency	Higher	Lower
Scalability	Moderate	High

The use of AXI Ethernet Lite, AXI-based architecture, and Vivado/Vitis design flow enhances system flexibility, debugging capability, and resource efficiency. Overall, the proposed system provides a cost-effective and optimized solution for FPGA-based Ethernet communication while maintaining reliable networking performance.

IV. CONCLUSION

A MicroBlaze-based Ethernet Lite communication system was successfully implemented on the Artix-7 Arty A7-35T FPGA using Xilinx Vivado and Vitis tools. The proposed system integrated AXI Ethernet Lite, MicroBlaze processor, AXI UART Lite, AXI Timer, AXI Interrupt Controller, and lwIP TCP/IP stack for embedded Ethernet communication. The implemented design achieved reliable 10/100 Mbps Ethernet communication between the FPGA board and host computer through static IP configuration. Experimental results verified successful packet transmission, packet reception, TCP/IP communication, ping response, and UART debugging. Compared to the existing TEMAC-based architecture, The proposed system achieved optimized FPGA resource utilization with 11,847 LUT usage and 22 BRAM utilization. The power consumption was also reduced from 12.27 W to 0.892 W, improving energy efficiency. The AXI-based architecture simplified hardware integration and improved scalability and debugging support. The use of AXI Ethernet Lite IP reduced overall hardware complexity and development cost. The proposed system demonstrates an efficient and lightweight FPGA-based embedded networking solution suitable for industrial automation, IoT, and real-time communication applications.

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