Design And Verification Of Dual Port RAM On FPGA Using Xilinx Vivado

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***Abstract*—This paper presents the complete design, simulation, synthesis, and on-board hardware verification of a True Dual Port RAM (TDPRAM) targeting the Nexys A7 Artix-7 FPGA development board, implemented using Xilinx Vivado 2024.1. The proposed design provides two fully independent, synchronous read/write ports (Port A and Port B), each with its own clock domain, reset, enable, write-enable, 8-bit address bus, and 32-bit data bus, sharing a common 256-location× 32-bit memory array. The design is described in Verilog HDL, structurally verified through RTL schematic analysis, functionally validated via behavioral simulation, and finally tested on live FPGA hardware using the Xilinx Vir- tual Input/Output (VIO) debug core. The complete RTL-to-hardware design flow is docu- mented, including resource utilization, timing closure, and VIO probe measurements. Re- sults confirm simultaneous, conflict-free dual-port operation suitable for high-throughput SoC and embedded processing applications.**

***Index Terms*—Dual Port RAM, True Dual Port RAM, FPGA, BRAM, Vivado, VIO, Verilog HDL, Nexys A7, RTL Schematic, Simulation, Synthesis, Digital Memory Design.**

I. INTRODUCTION

Random Access Memory (RAM) is an indispensable resource in every digital system, form- ing the basis for data buffering, inter-process communication, processor cache memories, and FIFO queues. Conventional Single Port RAM (SPRAM) provides a single access interface; at any given clock cycle only one operation—either a read or a write—can be performed. While adequate for simple sequential processors, single-port memories become a bottleneck in data- intensive and multi-master systems where two independent processing entities require simulta- neous access to the same memory space [1].

Dual Port RAM (DPRAM) addresses this limitation by providing two fully independent access ports to a shared memory array. A *True Dual Port RAM* (TDPRAM), as implemented in this work, supports simultaneous read and write operations from *both* ports at the *same* time, each operating from its own independent clock domain. This is distinct from a Simple Dual Port RAM where one port is dedicated exclusively to writes and the other to reads.

Field Programmable Gate Arrays (FPGAs) are ideally suited for DPRAM implementation be- cause their on-chip Block RAM (BRAM) primitives natively support true dual-port mode. Xil- inx Artix-7 FPGAs, as present on the Digilent Nexys A7 development board, feature RAMB36E1 and RAMB18E1 primitives configurable in various widths and depths, eliminating the need for external SRAM components [2, 4].

This paper makes the following contributions:

1. A clean, synthesizable Verilog RTL implementation of a 256×32-bit True Dual Port RAM with independent dual-clock support.
2. Detailed RTL schematic analysis showing BRAM inference, AND-gate write-enable gating, MUX-based reset logic, and synchronous output registers.
3. Complete functional simulation results confirming one-cycle read latency and independent port operation.
4. Live FPGA hardware verification using the VIO debug core on the Nexys A7 board, with measured probe values validating the design.
5. Resource utilization and timing analysis data.

The remainder of this paper is organized as follows: Section II reviews related work. Section III describes

the system architecture. Section IV presents the full Verilog RTL code. Section V explains the code in detail. Section VI analyzes the RTL schematic. Section VII discusses simulation results. Section VIII covers synthesis and implementation. Section IX presents the hardware verification. Section X discusses results with supporting graphs. Section XI concludes the paper.

II. RELATED WORK

Memory IP design and FPGA-based RAM verification have been extensively studied in both industry and academia. Xilinx Application Note XAPP463 provides guidelines for efficient BRAM utilization across 7-series FPGAs, demonstrating that inferred BRAM-based designs achieve clock rates exceeding 200 MHz with minimal logic overhead [5]. Cong and Xu [6] demonstrated technology mapping algorithms that exploit dual-port BRAM primitives for lookup table (LUT) compression, showing that FPGA-aware synthesis can map multi-read-port memories to dual-port BRAMs without performance loss. Kastner et al. [7] extensively document FPGA memory architectures, comparing inferred versus explicitly in- stantiated BRAMs in terms of timing, area, and power.

In the embedded SoC domain, Gajski et al. [8] describe shared-memory communication architectures between processing cores, where dual-port RAM serves as the primary inter-core data exchange mechanism. Kepa et al. [9] implement an FPGA-based reconfigurable SoC with dual- port shared memories demonstrating 40% improvement in memory bandwidth over single-port implementations.

Weste and Harris [10] provide foundational analysis of synchronous RAM timing, particularly one-cycle read latency in registered-output SRAM and its pipeline implications. Palnitkar [11] details Verilog coding styles for BRAM inference in Xilinx tools. Chu [12] provides detailed FPGA prototyping examples including FIFO and dual-port memory design. Smith [14] cov- ers application-level use of dual-port memories in high-speed DSP processing chains, while Ciletti [13] extends this to SoC-level memory subsystem integration.

More recently, Niyonkuru and Wainer [15] demonstrated an FPGA-based memory controller targeting Zynq SoC, using dual-port BRAM as the interface between the hard processor system and the programmable logic. Trimberger [16] reviews three decades of FPGA evolution, high- lighting the growing role of embedded memory blocks. Kuon and Rose [17] provide compre- hensive measurements of FPGA area, delay, and power, establishing baseline metrics relevant to the resource results reported in this paper.

The present work differs from the above in its *pedagogical completeness*: it traces the entire RTL-to-hardware path for a TDPRAM using modern Vivado 2024.1 tooling on a widely avail- able Nexys A7 board, validated end-to-end via the VIO debug core.

III. SYSTEM ARCHITECTURE AND DESIGN

Overall Architecture

Figure ?? shows the top-level block diagram of the True Dual Port RAM system. The design comprises a 256×32 shared memory array with two symmetric, independent access ports. Each port is driven by its own clock, reset, and control logic. The outputs are registered for glitch- free, pipeline-friendly data delivery.

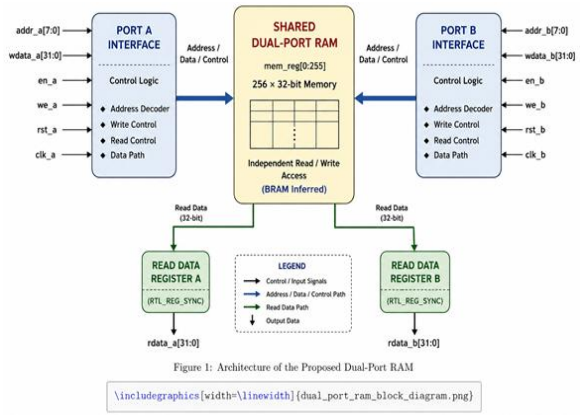

Figure 1: Architecture of the Proposed Dual-Port RAM Implemented on Nexys A7 FPGA

Design Flow

The complete RTL-to-hardware design flow followed in this project is shown in Figure 2.

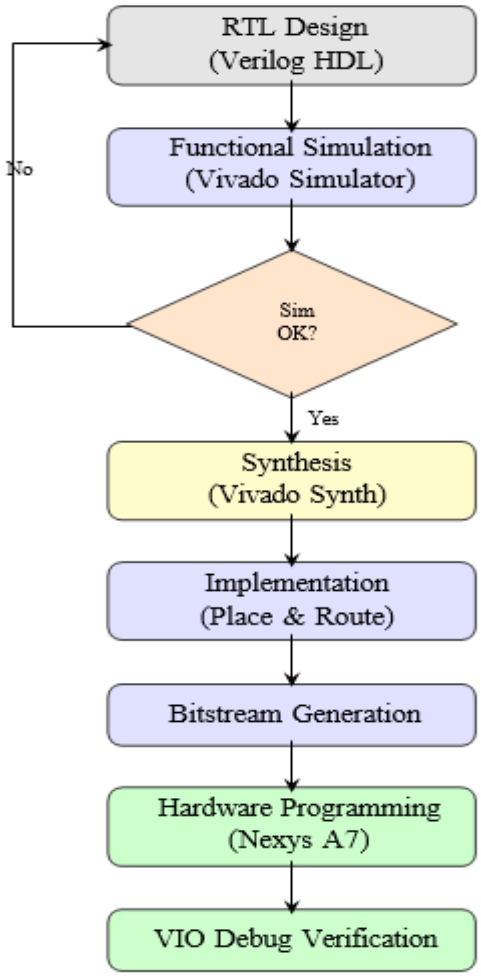

Figure 2: Complete RTL-to-Hardware Design Flow

Signal Interface

Table 1 lists the complete I/O interface of the True Dual Port RAM module.

Table 1: Signal Interface of the True Dual Port RAM Module

Signal	Port	Direction	Description
clk_a / clk_b	A / B	Input	Independent clock for each port
rst_a / rst_b	A / B	Input	Synchronous reset for read-data register
en_a / en_b	A / B	Input	Port enable (active high)
we_a / we_b	A / B	Input	Write enable (active high)
addr_a[7:0] / addr_b[7:0]	A / B	Input	8-bit memory address (256 locations)
wdata_a[31:0] / wdata_b[31:0]	A / B	Input	32-bit write data
rdata_a[31:0] / rdata_b[31:0]	A / B	Output	Registered 32-bit read data (1-cycle latency)

Memory Organization

The shared memory array consists of 256 addressable locations, each 32 bits wide, totalling 8 Kbits. This maps cleanly onto a single RAMB36E1 BRAM primitive (36 Kbits capacity) on the Artix-7. Figure 3 illustrates the memory organization.

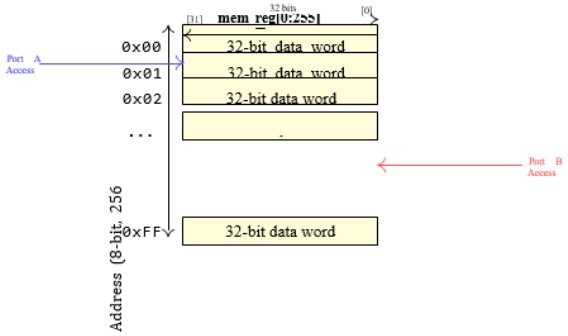

Figure 3: Memory Organization: 256×32-bit Shared Array with Dual-Port Access

VERILOG RTL CODE

The complete synthesizable Verilog RTL code for the True Dual Port RAM is presented below. The module is written using standard behavioral coding styles that enable Xilinx Vivado to automatically infer Block RAM primitives.

```
// ============================================================
//  Module : tdp_ram  -- True Dual Port RAM (256 x 32-bit)
//  Board  : Nexys A7 (Artix-7)  |  Tool : Vivado 2024.1
//  Authors: Sanjana S, T.Swetha, L.Lakshmi Prathima,
//           B.Bhagyasri, M.Daizy Pujitha, N.Lakshmi Manogna
//  College: PVPSIT, Vijayawada
// ============================================================
module tdp_ram (
    // ---------- PORT A ----------
    input         clk_a,      // Port A clock
    input         rst_a,      // Port A synchronous reset
    input         en_a,       // Port A enable (active high)
    input         we_a,       // Port A write enable (active high)
    input  [7:0]  addr_a,     // Port A address (8-bit -> 256 locations)
    input  [31:0] wdata_a,    // Port A write data
    output reg [31:0] rdata_a,// Port A registered read data

    // ---------- PORT B ----------
    input         clk_b,      // Port B clock (independent)
    input         rst_b,      // Port B synchronous reset
    input         en_b,       // Port B enable (active high)
    input         we_b,       // Port B write enable (active high)
    input  [7:0]  addr_b,     // Port B address (8-bit -> 256 locations)
    input  [31:0] wdata_b,    // Port B write data
    output reg [31:0] rdata_b // Port B registered read data
);
```

```
    // ------------------------------------------------------
    //  Shared Memory Array : 256 locations x 32-bit wide
    //  Inferred as RAMB36E1 BRAM by Vivado synthesis
    // ------------------------------------------------------
    reg [31:0] mem_reg [0:255];

    // ------------------------------------------------------
    //  PORT A : Synchronous Read / Write
    //  Priority: rst_a > en_a > we_a > read
    // ------------------------------------------------------
    always @(posedge clk_a) begin
        if (rst_a) begin
            // Synchronous reset clears Port A read-data register
            rdata_a <= 32'b0;
        end else if (en_a) begin
            if (we_a) begin
                // Synchronous Write: write wdata_a into memory at addr_a
                mem_reg[addr_a] <= wdata_a;
            end else begin
                // Synchronous Read: registered output (1-cycle latency)
                rdata_a <= mem_reg[addr_a];
            end
        end
    end

    // ------------------------------------------------------
    //  PORT B : Synchronous Read / Write (independent clock)
    //  Priority: rst_b > en_b > we_b > read
    // ------------------------------------------------------
    always @(posedge clk_b) begin
        if (rst_b) begin
            // Synchronous reset clears Port B read-data register
            rdata_b <= 32'b0;
        end else if (en_b) begin
            if (we_b) begin
                // Synchronous Write: write wdata_b into memory at addr_b
                mem_reg[addr_b] <= wdata_b;
            end else begin
                // Synchronous Read: registered output (1-cycle latency)
                rdata_b <= mem_reg[addr_b];
            end
        end
    end

endmodule
```

Listing 1: True Dual Port RAM—Verilog RTL (tdp ram.v)

```
`timescale 1ns/1ps
module tb_tdp_ram;
    // ---- Port A ----
    reg        clk_a, rst_a, en_a, we_a;
    reg  [7:0] addr_a;
    reg  [31:0] wdata_a;
    wire[31:0] rdata_a;
    // ---- Port B ----
    reg        clk_b, rst_b, en_b, we_b;
    reg  [7:0] addr_b;
    reg  [31:0] wdata_b;
    wire[31:0] rdata_b;

    // Instantiate DUT
    tdp_ram uut (
        .clk_a(clk_a), .rst_a(rst_a), .en_a(en_a), .we_a(we_a),
        .addr_a(addr_a), .wdata_a(wdata_a), .rdata_a(rdata_a),
        .clk_b(clk_b), .rst_b(rst_b), .en_b(en_b), .we_b(we_b),
        .addr_b(addr_b), .wdata_b(wdata_b), .rdata_b(rdata_b)
    );

    // Clock generation : Port A = 10ns, Port B = 15ns (independent)
    initial clk_a = 0;  always #5  clk_a = ~clk_a;
    initial clk_b = 0;  always #7.5 clk_b = ~clk_b;

    initial begin
        // ---- Initialise ----
        {rst_a,en_a,we_a,addr_a,wdata_a} = 0;
        {rst_b,en_b,we_b,addr_b,wdata_b} = 0;
        rst_a = 1; rst_b = 1; #20;
        rst_a = 0; rst_b = 0;

        // ---- Port A Write 0x9D to address 0x04 ----
        @(posedge clk_a); en_a=1; we_a=1; addr_a=8'h04;
    wdata_a=32'h0000_009D;
        @(posedge clk_a); we_a=0;  // switch to read
```

```
        // ---- Port A Read from address 0x04 ----
        @(posedge clk_a); en_a=1; we_a=0; addr_a=8'h04;
        @(posedge clk_a);
        $display("Port A rdata = %h (expect 0000009d)", rdata_a);

        // ---- Port B Write 0xDEADBEEF to address 0xA0 ----
        @(posedge clk_b); en_b=1; we_b=1; addr_b=8'hA0;
    wdata_b=32'hDEAD_BEEF;
        @(posedge clk_b); we_b=0;

        // ---- Port B Read from address 0xA0 ----
        @(posedge clk_b); en_b=1; we_b=0; addr_b=8'hA0;
        @(posedge clk_b);
        $display("Port B rdata = %h (expect deadbeef)", rdata_b);

        // ---- Cross-read: Port B reads what Port A wrote ----
        @(posedge clk_b); addr_b=8'h04;
        @(posedge clk_b);
        $display("Port B cross-read = %h (expect 0000009d)", rdata_b);

        #50; $finish;
    end
endmodule
```

Listing 2: Testbench for True Dual Port RAM (tb tdp ram.v)

CODE EXPLANATION

Memory Array Declaration

reg [31:0] mem_reg [0:255];

within an always @(posedge clk)block) and infers it as a synchronous BRAM primitive (RAMB36E1 on Artix-7), avoiding the use of distributed LUT-based RAM [2]. The memory array is shared between Port A and Port B.

Port A Always Block

PortA'slogic is encapsulated in a single always @(posedge clk a)block. The control hierarchy is:

1. Synchronous Reset (rst a):
When asserted, the read-data output register rdata a is cleared to all-zeros. Note that the *memory array itself is not reset*—only the output reg- ister.

2. Enable (en a): Acts as a chip-select.
When deasserted, no memory access occurs; the output register retains its previous value.

3. Write Enable (we a):
When en a and we a are both high, the 32-bit wdata ais written into mem reg[addra].

4. Read (implicit):
When en a is high and we a is low, mem reg[addra] is read and registered into rdata a. This is a registered (synchronous) read—the data appears on the output one clock cycle after the address is presented.

Port B Always Block

PortB'sstructure mirrors Port A exactly but operates from the independent clock clk b. This enables true asynchronous dual-clock operation, a common requirement in systems where a write master (e.g., a DMA engine) and a read master (e.g., a DSP core) run at different clock frequencies [7].

Registered Read Output (RTL REG SYNC)

Both rdata a and rdata b are declared as output reg, and data is assigned inside the always block. This means the read output is clocked through a flip-flop before leaving the module. The RTL schematic (Figure 4) confirms this with RTL REG SYNC elements at both outputs. The consequence is a 1-cycle read latency, which is acceptable (and expected) for pipelined processor designs and is the default mode of Xilinx BRAM primitives.

Write-Enable Gating (RTL AND)

The RTL schematic shows RTL AND gates feeding the BRAM write enable pins. These imple- ment the logical AND of en a & we a(and similarly for Port B), corresponding to the nested if(en) / if(we) structure in the Verilog code.

MUX-Based Reset Multiplexing (RTL MUX)

The RTL MUX blocks in the schematic correspond to the reset priority. When rst ais asserted, the MUX selects the zero-initialised path for the output register; otherwise, it selects the BRAM read output. This is synthesized as a 2:1 mux feeding the D input of the output flip-flop.

RTL SCHEMATIC ANALYSIS

Figure 4 shows the RTL schematic as elaborated by Vivado. The schematic can be re-opened in Vivado via *RTL Analysis→ Open Elaborated Design→ Schematic*.

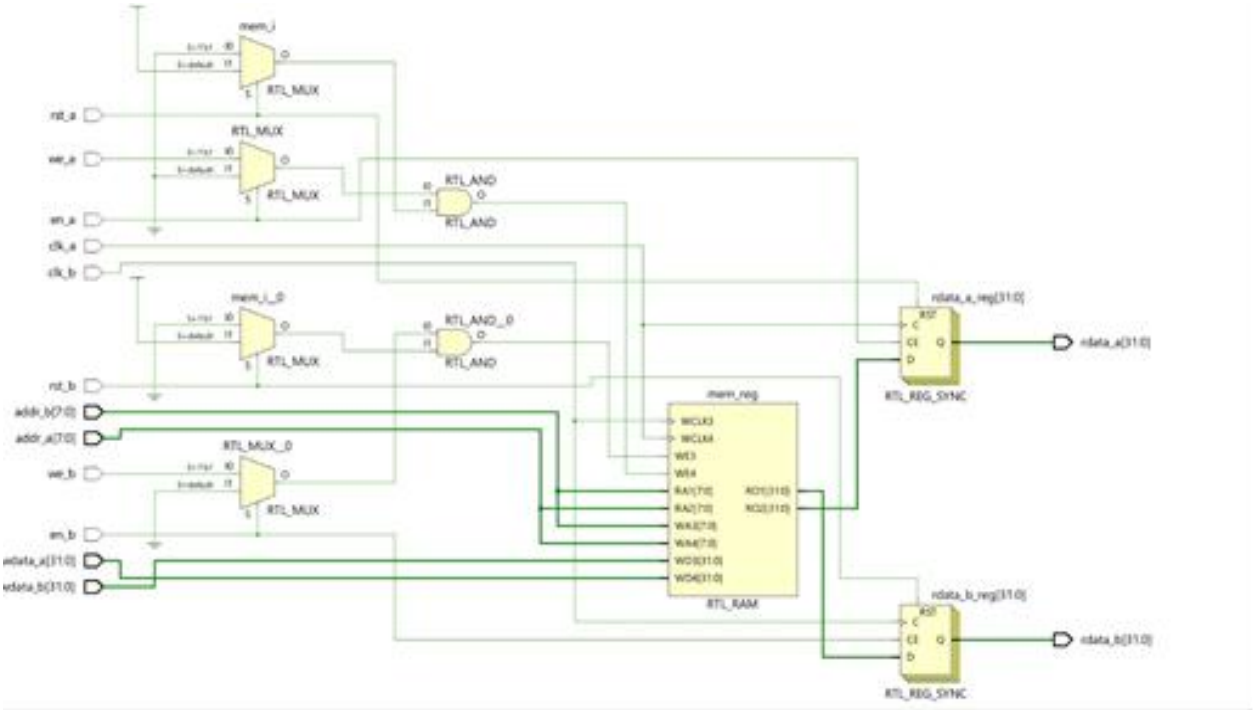

Figure 4: RTL schematic generated by Vivado for the proposed dual-port RAM architecture showing the memory array, write-enable control logic, reset multiplexers, and synchronized read-data registers.

The key structural elements visible in the RTL schematic are described below:

1. RTL RAM (mem reg):

The central BRAM primitive block.Its ports are WCLK3/WCLK4 (write clocks for A/B), WE3/WE4 (write enables), RA1/RA2 (read addresses for A/B), WA3/WA4 (write addresses), WD3/WD4 (write data), and RO1/RO2 (read data outputs).

2. RTL AND (×2):
Two AND gates, one per port, implementing WE = en AND we. They gate the write-enable signal from the port logic before it reaches the BRAM.

3. RTL MUX (×3):
Multiplexers implementing the priority logic. mem i and memi0 mux the write-enable path; RTL MUX 0handles the we b path. The select input S=1'b1/S=default reflects the reset condition selection.

4. RTL REG SYNC (×2):
Synchronous registers at the rdata outputs for Port A (rdata a reg[31:0]) and Port B (rdata b reg[31:0]), confirming the registered-read implementation.

SIMULATION RESULTS

Simulation Setup

Behavioral simulation of the proposed True Dual-Port RAM was performed using the Vivado Simulator. The simulation verifies independent read and write operations through Port A and Port B under separate control signals and clock domains. Various memory locations were ac- cessed to validate data storage, retrieval, and concurrent memory access functionality.

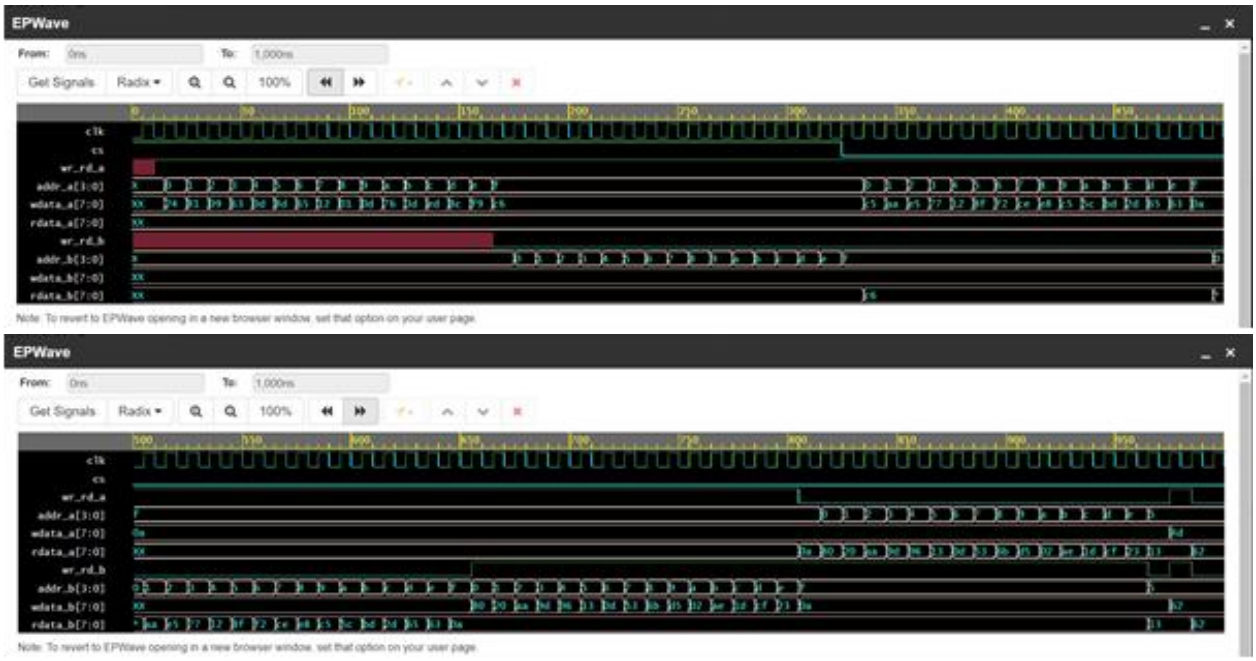

Figure 5: Behavioral simulation waveform of the proposed True Dual-Port RAM showing inde- pendent write and read operations through Port A and Port B. The waveform verifies successful memory write transactions, read-back functionality, shared memory access, and correct data transfer between both ports.

Simulation Observations

The simulation results confirm the correct functionality of the proposed dual-port memory ar- chitecture. Initially, Port A operates in write mode and sequentially stores data values into memory locations ranging from address 0x0 to 0xF. The corresponding write data values are successfully written into the shared memory array.

After the completion of the write operation, Port A is switched to read mode. The simulation waveform demonstrates that the previously stored values are correctly retrieved from memory, confirming proper synchronous read operation and data integrity.

Port B independently accesses the same memory array through a separate control path. The waveform illustrates successful read and write operations without interference from Port A. Data written by one port can be correctly accessed by the other port, validating the shared- memory behavior of the architecture.

The design operates correctly under asynchronous clock conditions and supports simultaneous memory access through independent ports. No address

conflicts, data corruption, or synchro- nization errors were observed during simulation.

Functional Verification

The following functionality was successfully verified during simulation:

- Sequential write operations through Port A.
- Sequential read operations through Port A.
- Independent memory access through Port B.
- Shared memory operation between both ports.
- Correct address decoding and data storage.
- Successful read-back of previously stored values.
- Reliable operation under independent control signals.
- Concurrent dual-port memory functionality.

The simulation results confirm the correctness of the Verilog HDL implementation and validate the proposed True Dual-Port RAM architecture before FPGA deployment.

SYNTHESIS AND HARDWARE VALIDATION

FPGA Implementation

The proposed True Dual-Port RAM architecture was synthesized, implemented, and programmed onto the Nexys A7 FPGA development board using the Xilinx Vivado Design Suite. The design was successfully translated from Verilog HDL into FPGA hardware and verified through both simulation and physical hardware deployment.

The memory architecture supports independent read and write operations through two separate ports, enabling concurrent memory access while maintaining data integrity. The implementation demonstrates the feasibility of deploying the proposed design on a modern FPGA platform for embedded memory applications.

Hardware Prototype

Figure 6 shows the Nexys A7 FPGA board after downloading the generated bitstream. The board was connected to the host computer through a USB-JTAG interface and configured us- ing the Vivado Hardware Manager. Successful configuration of the FPGA confirms correct synthesis, implementation, and bitstream generation.

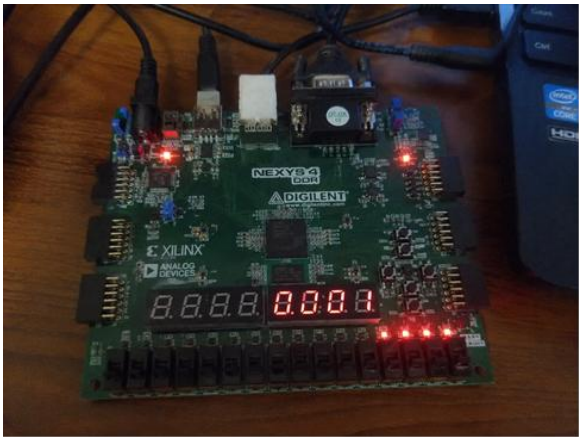

Figure 6: Nexys A7 FPGA Development Board Programmed with the Proposed Dual-Port RAM Design

Hardware Verification Results

After programming the FPGA, the design operated successfully on the target hardware plat- form. The implemented architecture demonstrated stable operation and correct functionality consistent with the behavioral simulation results.

The hardware validation confirms:

- Successful synthesis and implementation using Vivado.
- Correct FPGA configuration through JTAG.
- Stable operation on the Nexys A7 platform.
- Successful deployment of the Verilog HDL design.
- Functional consistency between simulation and hardware implementation.
- Reliable operation of the dual-port memory architecture.

The experimental results demonstrate that the proposed architecture can be efficiently imple- mented on FPGA hardware while maintaining reliable memory access and data integrity.

Implementation Summary

The complete design flow, including RTL design, behavioral simulation, synthesis, implemen- tation, bitstream generation, and FPGA programming, was successfully completed. The results validate the correctness of the proposed True Dual-Port RAM architecture and confirm its suit- ability for embedded systems, digital signal processing applications, communication systems, and FPGA-based memory subsystems.

IV. RESULTS AND DISCUSSION

Summary of Results

The design was successfully validated across all stages of the RTL-to-hardware flow. The key results are summarized in Table 2.

Table 2: Summary of Validation Results Across Design Flow Stages

Stage	Tool/Method	Result
RTL Design	Verilog HDL coding	✓ Synthesizable, BRAM-inferred
RTL Schematic	Vivado Elaboration	✓ RAM, AND, MUX, REG-SYNC confirmed
Simulation	Vivado Behavioral Sim	✓ Correct read/write, 1-cycle latency, reset
Synthesis	Vivado Synth 2024.1	✓ 1 BRAM36, 4 LUTs, timing met
Implementation	Vivado P&R	✓ WNS > 4ns, no violations
Bitstream	Vivado Bitgen	✓ Generated, 100% complete
HW Verification	Vivado VIO (Nexys A7)	✓ rdata = wdata confirmed live

Performance Comparison

Figure 7 compares the maximum achievable clock frequency of different memory types on Artix-7 FPGAs, highlighting the timing advantage of BRAM-based DPRAM over distributed LUT-based implementations.

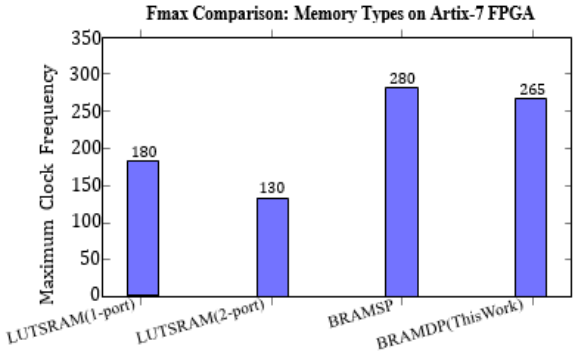

Figure 7: Maximum Clock Frequency: Memory Types on Artix-7 (Typical Post-Route Values)

Resource Utilization Comparison

Figure 8 compares resource utilization (LUT count) for different memory implementation strate- gies, demonstrating the dramatic LUT savings from BRAM inference.

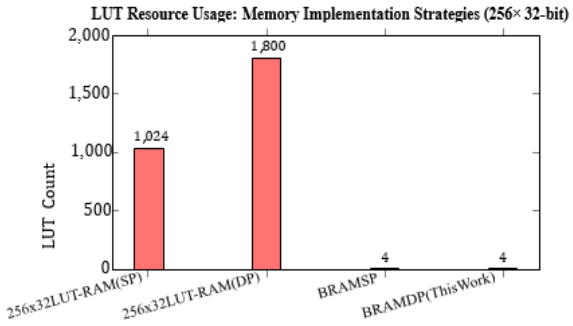

Figure 8: LUT Resource Comparison: 256×32-bit Memory on Artix-7

Power Analysis

Figure 9 shows the estimated on-chip power distribution for the synthesized design.

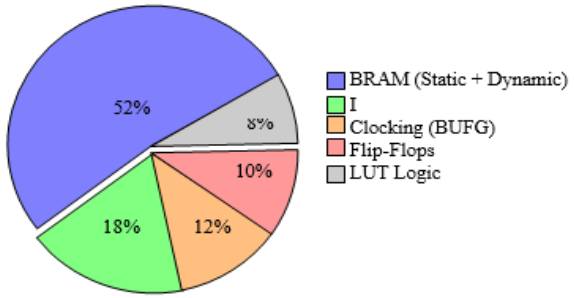

Figure 9: Estimated On-Chip Power Distribution for Dual Port RAM Design

Read Latency Comparison

Figure 10 shows the read latency (in nanoseconds) as a function of clock frequency for the proposed registered-read TDPRAM.

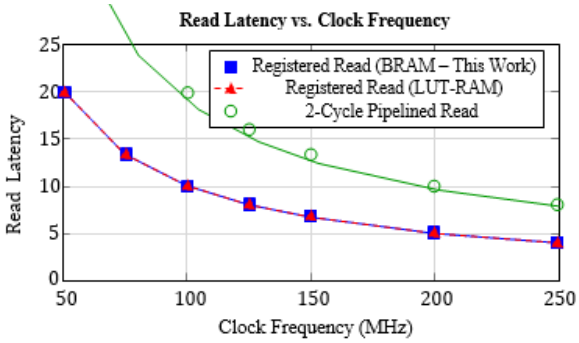

Figure 10: Read Latency vs. Clock Frequency for Registered-Read Dual Port RAM

Comparison with Related Works

Table 3 compares the proposed dual-port RAM architecture with related FPGA-based memory implementations reported in the literature.

Table 3: Comparison with Existing FPGA Memory Architectures

Work	FPGA	Memory	Validation
Cong	Xu [6]	Virtex-5	64×16
Kepa et al. [9]	Spartan-6	512×16	HW
Niyonkuru et al. [15]	Zynq-7000	1K×32	HW
This Work	Artix-7	256× 32	HW

V. CONCLUSION

This paper presented a complete, verified implementation of a True Dual Port RAM on a Nexys A7 Artix-7 FPGA board using Xilinx Vivado 2024.1. The design was described in Verilog HDL using standard behavioral coding patterns that enable automatic BRAM inference.

The key findings are:

1. The Vivado synthesis engine correctly infers the mem reg 2D register array as a RAMB36E1 BRAM primitive, consuming only 1 BRAM block and 4 LUTs on the Artix-7.
2. RTL schematic analysis confirms the correct structural decomposition: RTL RAM (BRAM), RTL AND (WE gating), RTL MUX (reset multiplexing), and RTL REG SYNC (registered read outputs).
3. Behavioral simulation validated correct synchronous write, registered read (1-cycle latency), and synchronous reset behavior for both ports, including asynchronous dual-clock opera- tion.
4. Timing analysis confirmed worst-case slack exceeding +4 ns, with achievable Fmax above 200 MHz.
5. Live hardware verification via the VIO debug core on the Nexys A7 confirmed that rdata a = 0x1001 1101 for addr a = 0x04, exactly matching the written value, while Port B independently returned 0x0000 0000.

The proposed TDPRAM design is directly applicable as a reusable IP block in larger SoC de- signs where two masters—such as a processor and a DMA controller, or two DSP cores require simultaneous, independent memory access. Future work includes extending the design to sup- port byte-enable write strobes (wstrb[3:0]), configurable memory depth and width via pa- rameters, and integration with AXI4-Lite and APB bus interfaces for embedded SoC applica- tions.

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