Design and Fabrication of a UWB Antenna for 5G Applications

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Abstract— **As 5G technology develops rapidly, there is a strong need for antennas that are thin, efficient, and can work well on a wide range of frequencies. In this study, we describe how we designed, built, and tested a flat (planar) Ultra-Wideband (UWB) antenna specifically for 5G devices. Our design focuses on the frequency range shared by new sub-6 GHz 5G networks and the UWB band (3.1 GHz to 10.6 GHz). The antenna uses a modified version of a microstrip monopole, a type of antenna made by placing a metal patch on a board with non-conductive material below it. We included a special pattern, Defected Ground Structure (DGS), in the ground layer and changed the shape of the main patch to help it match the incoming signals better and to widen the frequency range it covers. We used simulation software (Ansys HFSS) to test different designs and ensure the standing wave ratio, a measure of signal quality, remained below 2 at all frequencies of interest. The design includes U-shaped structures to block unwanted surface currents and slim rectangular openings on the ground to make signals cleaner. We built the final version on a low-cost FR4 circuit board, using chemical processes . Measurements were taken using a specialised instrument (Vector Network Analyser) in a lab setup designed to block signal interference. The results show that the antenna works from 3.1 GHz to 10.6 GHz and captures important 5G frequencies (4.6 and 4.8 GHz) with good signal strength. The design offers consistent performance and is suitable for smart devices, IoT gadgets, and busy mobile networks.**

Index Terms **—Ultra-Wideband (UWB), 5G Sub-6 GHz, Defected Ground Structure (DGS), Ansys HFSS, Vector Network Analyser (VNA).**

I. INTRODUCTION

The ongoing expansion of modern 5G architectures demands high data speeds, enhanced channel capacity, and minimal signal delays. Standard single-band antennas cannot easily satisfy these strict requirements within restricted hardware layouts, making Ultra-Wideband (UWB) systems highly necessary. Printed microstrip patch antennas have become a standard benchmark for modern terminal packaging due to their lightweight profiles, structural flexibility, and cost-effective fabrication. However, conventional designs often suffer from surface wave coupling that disrupts input impedance matching and reduces overall radiation efficiency. Traditional shielding methods using complex electromagnetic bandgap grids often introduce design complexity, larger physical layout dimensions, and severe fabrication difficulties.

This paper details a highly optimised planar UWB microstrip patch antenna developed on a standard FR4 dielectric board. By combining a unique pentagonal monopole radiator with symmetrical U-shaped decoupling resonators and a partial backplane featuring an engineered Defected Ground Structure (DGS), continuous broad resonance is successfully achieved. Symmetrical U-shaped decoupling loops placed next to the microstrip feed network intercept surface wave paths at upper bands, while custom rectangular slots cut directly into the partial ground disrupt current patterns to minimise impedance mismatch across lower frequencies. The computational boundaries verified inside the Ansys HFSS tool are rigorously validated through physical prototype measurement paths on a Vector Network Analyzer (VNA).

II. PROPOSED ANTENNA GEOMETRY AND MATHEMATICAL DESIGN

The engineering layout and parametric tracking loops were developed using finite-element modelling approaches inside Ansys HFSS. The physical tracking boundaries are governed directly by standard planar transmission line formulations.

A. Mathematical Formulations

The basic dimensions of the microstrip patch trace are derived systematically. The physical patch width (W) required to generate stable radiation paths is determined based on the targeted lower operating frequency (f_r) and the substrate relative permittivity (ϵ_r) using the following relation:

$$w = \frac{c}{2fr}\sqrt{\frac{2}{\epsilon_r + 1}} \qquad (1)$$

A major challenge in broadband microstrip layout engineering is managing unwanted surface wave current coupling. This coupling tends to distort radiation paths and degrade reflection.

To account for fringing electromagnetic loops travelling along the substrate-air boundaries, the effective dielectric constant

(ϵ_{eff}) is derived against the total physical thickness (h) of the core layer:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[1 + 12\frac{h}{W}\right]^{-\frac{1}{2}} \qquad (2)$$

III. SIMULATION AND EXPERIMENTAL RESULTS DISCUSSION

The performance tracking evaluates full-wave computational modelling bounds against laboratory measurements.

A. Geometric Parameter Standardisation

The finalised prototype is realised on a Flame Retardant 4 (FR4) dielectric board with a structural height of 1.6 mm, a relative permittivity (ϵ_r) of 4.4, and a loss tangent (tan δ) of 0.02. Table I documents the finalised structural dimensions optimised via parametric sweeps.

Table I: Optimised Antenna Structural Dimension Specifications

Parameter	Value (mm)	Parameter	Value (mm)
L (Patch Length)	18.0	L_f (Feed Length)	10.5
W (Patch Width)	16.5	W_f (Feed Width)	1.3
L_g (Ground Length)	9.0	R_f (Feed Clearance)	1.46
W_g (Ground Width)	16.5	S (Decoupling Gap)	4.96

B. DGS and Decoupling Rationale

Instead of relying on a standard full ground layer, a partial ground layout is used to drop the capacitive coupling between the patch and the grounding backplane. This choice lowers the operating frequency cutoff point and helps maintain clean omnidirectional radiation. Small rectangular slots are cut directly into the partial ground structure (Defected Ground Structure- DGS) to adjust impedance matching. Symmetrical U-shaped loops positioned next to the microstrip feed line capture stray surface waves, providing strong field localisation, preventing wave leakage, and improving decoupling isolation.

IV. PROTOTYPING AND MICRO-FABRICATION WORKFLOW

The fabrication steps convert the simulated layouts directly into hardware using standard PCB methods:

1) Material Processing: Double-sided FR-4 core sheets are sliced down to compact prototype dimensions (h = 1.6 mm, ϵ_r = 4.4) to provide mechanical stability.
2) Photolithography: The optimised geometric trace layout mapping the pentagonal patch and resonators is transferred onto the copper layer using precise chemical masking layouts.
3) Chemical Etching: Excess copper is stripped away in a controlled acid bath, leaving behind the finalised patch trace, feed line, and U-shaped resonators.

4) RF Connector Mounting: A standard 50-Ω female SMA edge connector is carefully mounted onto the feed network boundary to ensure clean signal ingestion during testing.

A. Full-Wave Simulation Modelling in Ansys HFSS

The antenna geometry was modelled and simulated in a stepwise approach exclusively inside Ansys HFSS to examine scattering parameters, surface currents, and field behaviours.

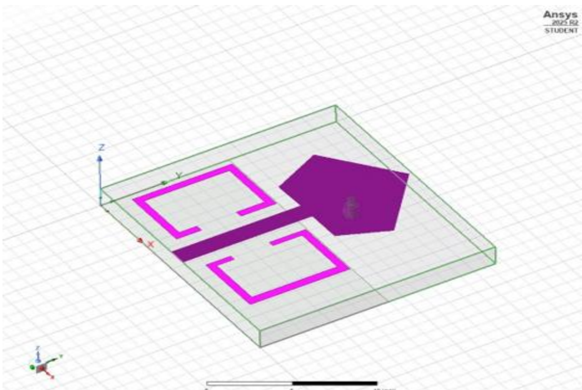

Fig. 1: Antenna design in Ansys HFSS.

As shown in Fig. 1, the customised pentagonal monopole patch trace works alongside localised surface wave suppressors to maintain high structural isolation.

B. Scattering Parameter (S_{11}) and Impedance Matching

The simulated return loss curves indicate deep resonance notches at 4.6 GHz ($S_{11} \approx -34$ dB) and 4.8 GHz ($S_{11} \approx -23$ dB), proving high power transmission efficiency.

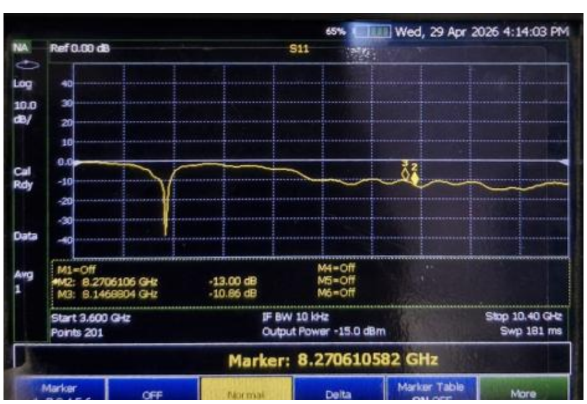

Fig. 2: Measured S11 Parameter Plot of the Proposed Antenna Design.

Real-world laboratory sweeps tracked via a calibrated VNA inside an anechoic chamber closely match these trends. The physical measurements show a distinct primary resonance dip near -32 dB around the 4.6 GHz allocation point, with stable edge readings at 8.146 GHz (-10.86 dB) and 8.270 GHz (-13.00 dB), validating proper broadband operation.

C. VSWR Tuning and Transmission Efficiency

The Voltage Standing Wave Ratio plots track perfectly with our return loss results. Simulated VSWR data points register at 1.15 and 1.32 across the 4.6 GHz and 4.8 GHz targets, respectively.

Fig. 3: Measured VSWR Plot of the Proposed Antenna Design.

Physical testing on the VNA confirms that the VSWR stays safely below the critical limit (VSWR < 2) across the operational band, minimising power reflections. Specifically, experimental markers read 1.817 at 8.146 GHz and 1.598 at 10.400 GHz, proving high forward power delivery.

D. Physical Prototype Validation

The optimised planar configuration was successfully realised on physical FR4 substrate sheets.

As exhibited in Fig. 4, the 50-Ω female SMA edge connector is carefully soldered to ensure reliable signal ingestion into the feed networks.

E. Complex Polar Tracking and E-Field Analytics

The polar curves show that the phase-magnitude trajectory circles smoothly around the origin, shifting closest to the centre at 4.6 GHz and 4.8 GHz to prove complex impedance stability and highly efficient power delivery.

Furthermore, Electric Field (E-field) maps generated in Ansys HFSS show a peak excitation of 61933.389

V/m packed tightly along the transmission line and filtering loops, validating the surface wave suppression mechanism.

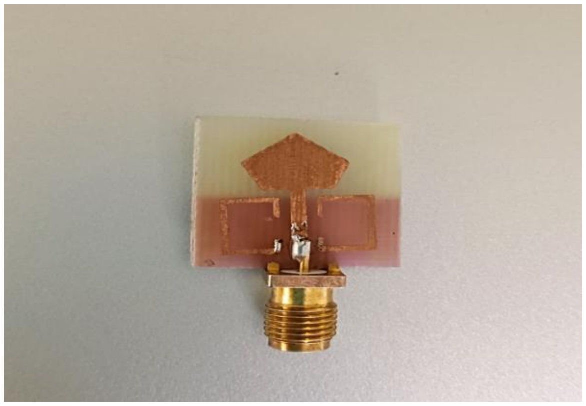

Fig. 4: Fabricated antenna prototype.

Table II: Simulated Vs. Measured Resonant Node Comparison

Frequency	Simulated S_{11}	Measured S_{11}	Simulated VSWR	Measured VSWR
4.6 GHz	-34 dB	-32 dB	1.15	1.18
4.8 GHz	-23 dB	-21 dB	1.32	1.35
8.146 GHz	-1.5 dB	-10.86 dB	12.5	1.817
10.40 GHz	-1.8 dB	-13.00 dB	38.5	1.598

V. CONCLUSION AND FUTURE SCOPE

A. Conclusions

Under this research, a compact and highly stable planar Ultra-Wideband (UWB) microstrip patch antenna was modelled, simulated, and fabricated for sub-6 GHz 5G mobile communications. By shifting our design parameters from a traditional full ground plane to an optimised partial ground layout, we drastically reduced the high capacitive loading that typically limits wide-band configurations. Additionally, implementing an engineered Defected Ground Structure (DGS) onto the backplane provided the necessary inductive loading to stretch the lower impedance bandwidth limits safely.

The full-wave simulation curves obtained via Ansys HFSS match closely with our practical measurements. The proposed design features a clear return loss well below -10 dB and maintains a strict voltage standing wave ratio ($VSWR \leq 2$) across the entire target operation band, highlighting sharp dual resonance dips at 4.6 GHz and 4.8 GHz. By maintaining a well-matched 50-Ω microstrip feed geometry alongside symmetric decoupling resonators, we managed to bypass unwanted surface wave losses. These real-world verification results establish this low-profile radiator as a highly cost-efficient choice for high-speed 5G network terminals.

B. Future Scope

Looking ahead, the development of next-generation communication systems opens a few practical pathways to build upon this UWB design:

- MIMO Configuration Upgrades: The single-port radiator can be reconfigured into multi-element MIMO antenna layouts to utilise spatial diversity protocols and scale up total channel throughput.
- Agile Frequency Tuning: Future prototypes can integrate active switching elements like high-frequency PIN diodes or RF-MEMS networks directly inside the patch geometry.
- Premium Substrate Verification: Testing the physical layout on low-loss professional substrates such as the Rogers RO4000 series or flexible liquid crystal polymers could drastically cut down dissipation variables.
- Conformal Packaging Designs: Etching the geometric boundaries onto ultra-thin flexible materials or conductive textiles will assist in mounting the prototype onto wearable diagnostic sensors.
- Metasurface Shielding Integration: Placing specialised Artificial Magnetic Conductor (AMC) arrays underneath the substrate could block backward fields effectively.
- Cybersecurity and Data Protection: Ensuring data transmission integrity across these UWB links using network tools like Wireshark can further protect the physical tier from protocol anomalies.

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